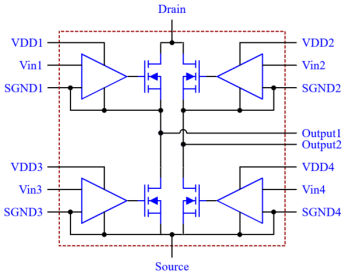
500 V, 30 MHz, 4500 W RF Power MOSFET-Driver Hybrid

DRF1510

Product Overview

500 V RF Power MOSFET-Driver Full-Bridge Hybrid: 4500 W at 13.56 MHz



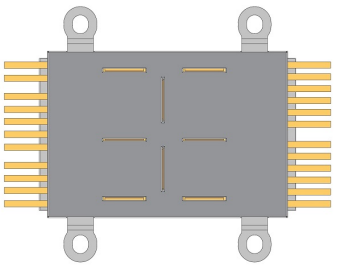


Table 1. Ordering Information

Catalog Part Number (CPN)	Package	Packing Media	Qualification
DRF1510	T102	Box	Industrial

Features

- Switching frequency: DC to 30 MHz
- Low pulse width distortion
- 1 V CMOS Schmitt trigger input with 1 V hysteresis
- Isolated backside to 1000 V
- RoHS compliant

Applications

- Class-D, Class-E RF generators
- Switch-mode power amplifiers
- Plasma
- Pulse generators
- CO_2 Lasers
- Semiconductor capital equipment
- Flat-panel displays, industrial glass, photovoltaic
- Induction heating, defrosting, drying
- Hazardous or toxic gas, waste treatment
- Lighting
- Ignition
- Ultrasonic cavitation

Benefits

- High efficiency
- Lower cost, more compact system than non-integrated driver and MOSFET
- Excellent thermal performance for high power density

DRF1510 Reference Design

DRF1510-CLASS-D learning tool and development platform enables minimal time-to-market, including:

- Detailed application note
- Circuit schematics
- Bill of materials
- Circuit board layout
- Theory of operation
- Performance data

1. Device Specifications

This section shows the specifications of this device.

1.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of this device. T_C = 25 °C unless otherwise specified.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
I_{DD}	Maximum driver supply current	15	A
V_{DD}	Driver power supply voltage	15	V
V_{in}	Input voltage	–5.0 to V_{DD} + 0.3	
V_{DSS}	Drain-source voltage	500	
I_D	Continuous drain current	30	A
I_{D_PK}	Peak drain current[1]	34	A
f	Maximum operating frequency	30	MHz

Note:

1. Repetitive rating: pulse width and case temperature are limited by the maximum junction temperature.

1.2 Thermal and Mechanical Characteristics

The following table shows the thermal and mechanical characteristics of this device.

Table 1-2. Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
$R_{\theta JC}$	Junction-to-case thermal resistance (per MOSFET)		0.137		°C/W
Q	Heat dissipation (per MOSFET)			1095	W
T_J	Operating junction temperature	–55		175	°C
T_A	Operating ambient temperature			125	
T_{STG}	Storage temperature	–40		125	
Wt	Package weight		28.8		g

ESD practices should comply with JESD-625.

1.3 Electrical Performance (per Driver-MOSFET Section)

The following table shows the static characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-3. Static Characteristics

Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{DD} = 12 V, V_{in} = 0 V, I_{DS} = 250 µA	500			V
$R_{DS(on)}$	Drain-source on-resistance	V_{DD} = 12 V, I_{DS} = 2 A			330	mΩ
V_{DD}	Driver power supply voltage		10		15	V
V_{in}	Input voltage		–5.0		V_{DD} + 0.3	
I_{DSS}	Zero-gate voltage drain current	V_{DS} = 500 V, V_{in} = 0 V			25	µA

.....continued						
Symbol	Characteristic	Test Conditions	Min.	Typ.	Max.	Unit
I_O	Output current	HV_{DC} = 400 V, P_{out} = 4500 W, Frequency = 13.56 MHz, Duty cycle = 50%			12.5	A

The following table shows the dynamic characteristics of this device. T_C = 25 °C unless otherwise specified.

Table 1-4. Dynamic Characteristics

Symbol	Characteristic	Test Conditions	Min	Typ	Max	Unit
C_{in}	Input capacitance	V_{DD} = 12 V, V_{DS} = 0 V, V_{in} = 0 V, ƒ = 1 MHz		35		pF
C_{oss}	Output capacitance	V_{in} = 0 V, V_{DS} = 150 V, ƒ = 1 MHz		210		
$t_{d(on)}$	Turn-on delay time (50% to 50%)	V_{DD} = 12 V, V_{in} = 0 V to 5 V, R_L = 16.6 Ω, C_L = 0.4 nF		24.8		ns
t_r	Voltage rise time (10% to 90%)			6.5		
$t_{d(off)}$	Turn-off delay time (50% to 50%)			31.6		
t_f	Voltage fall time (90% to 10%)			5.2		
$V_{T(on)}$	Turn-on threshold voltage	V_{DD} = 12 V, V_{in} = 0 V to 5 V ramp	2.20		2.70	V
$V_{T(off)}$	Turn-off threshold voltage	V_{DD} = 12 V, V_{in} = 5 V to 0 V ramp	0.95		1.35	
R_{in}	Input resistance			1		MΩ

1.4 Typical Performance Curves

This section shows the typical performance curves of this device. Data for performance curves are characterized, not 100% tested.

Figure 1-1. $R_{DS(on)}$ vs. Junction Temperature

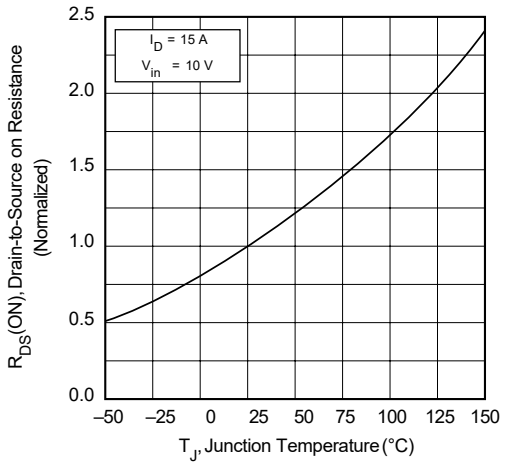


Figure 1-2. Capacitance vs. Drain-to-Source Voltage

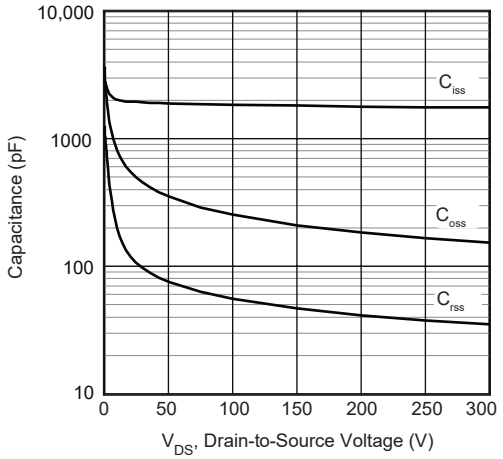


Figure 1-3. Forward Safe Operating Area

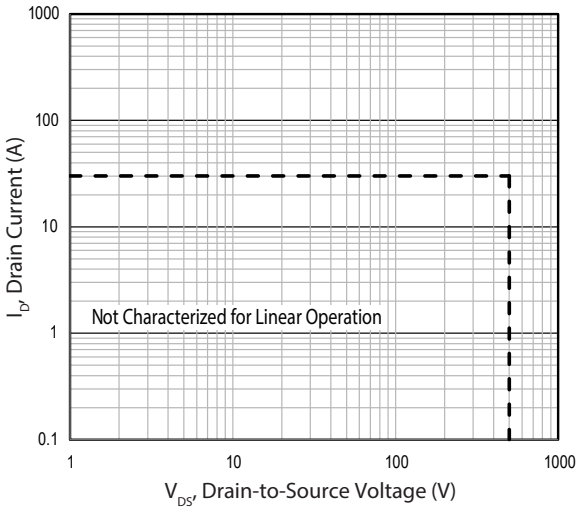


Figure 1-4. Output Power and Efficiency vs. HV_{DC}

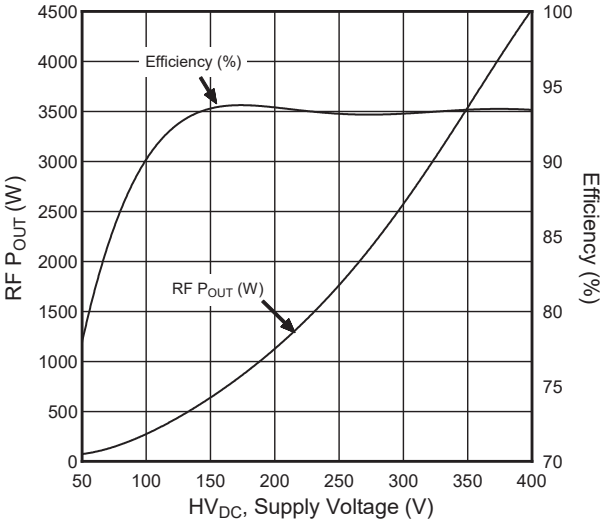
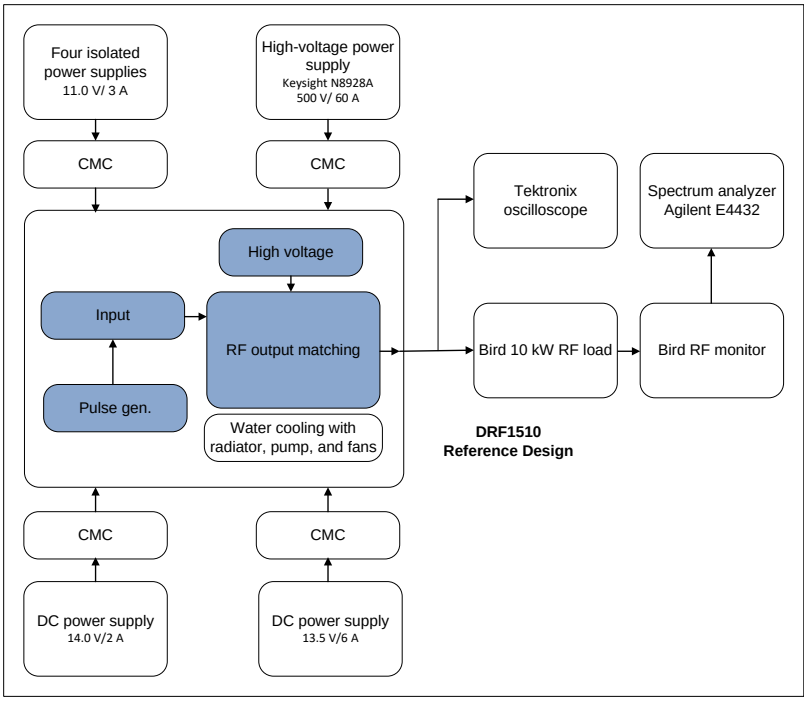


Figure 1-5. Test Setup Diagram



Note: See application note DRF1510 Class-D Full-Bridge RF Generator with Internal Cooling System.

Figure 1-6. Maximum Transient Thermal Impedance

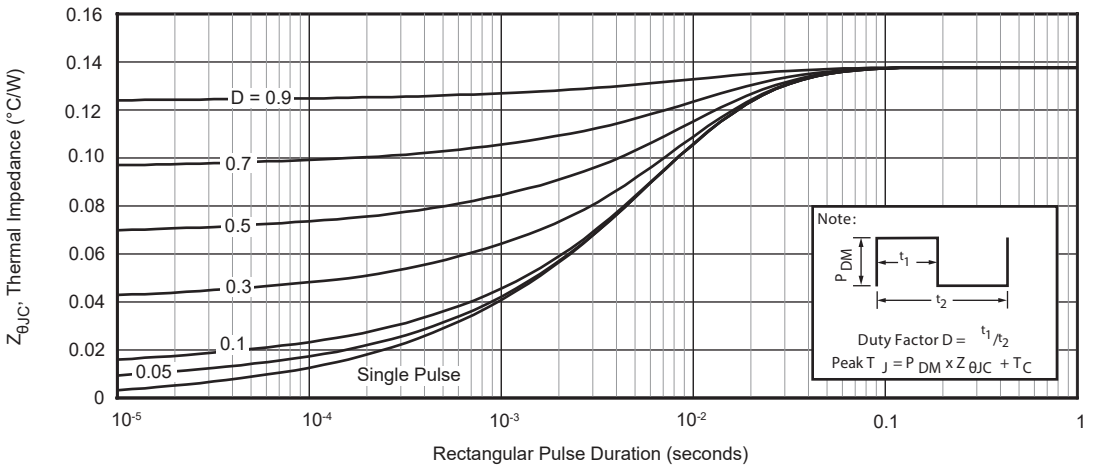
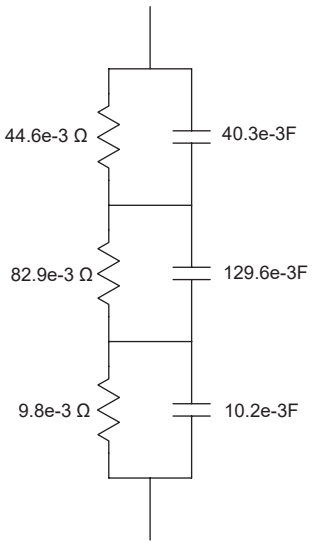


Figure 1-7. Transient Thermal Impedance Model



2. Test Circuits

The following figure shows the test circuits for each driver-MOSFET section of this device.

Figure 2-1. Simplified Circuit Diagram

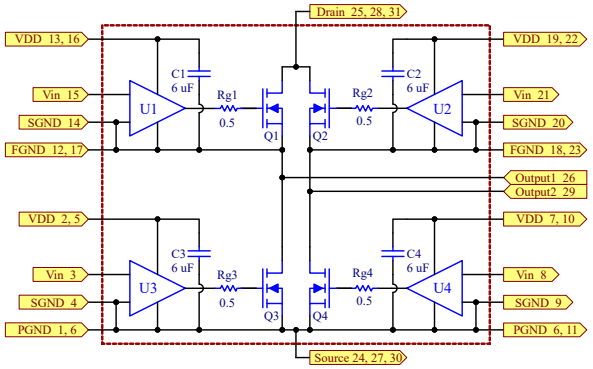
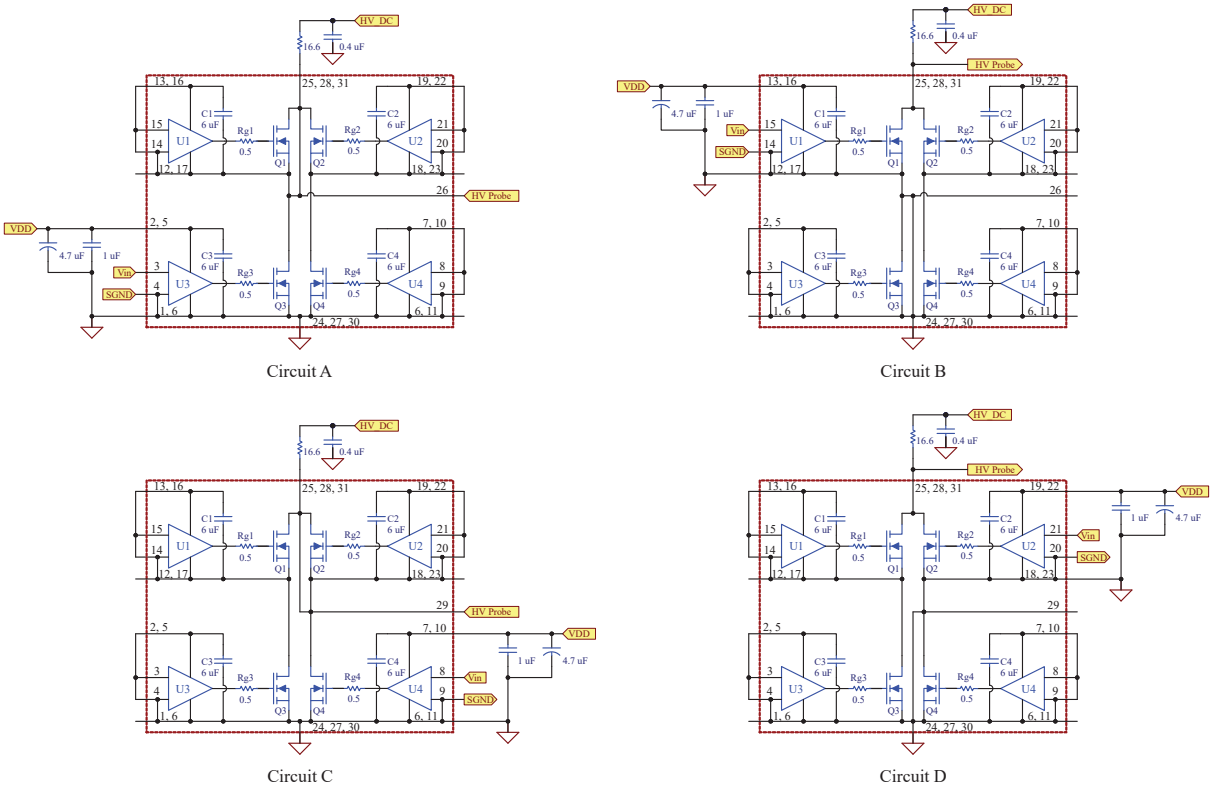


Figure 2-2. Test Configurations



Note: The DRF1510 Test Circuits illustrated are for reference only. These four circuits allow each of the sections in the Full Bridge to be tested independently. Circuits A, C are configured to test the lower or negative supply section of the DRF1510, and Circuits B, D are configured to test the upper or positive supply section. This method ties all pins of the unused section to the output Circuits A, C or the ground Circuits B, D.

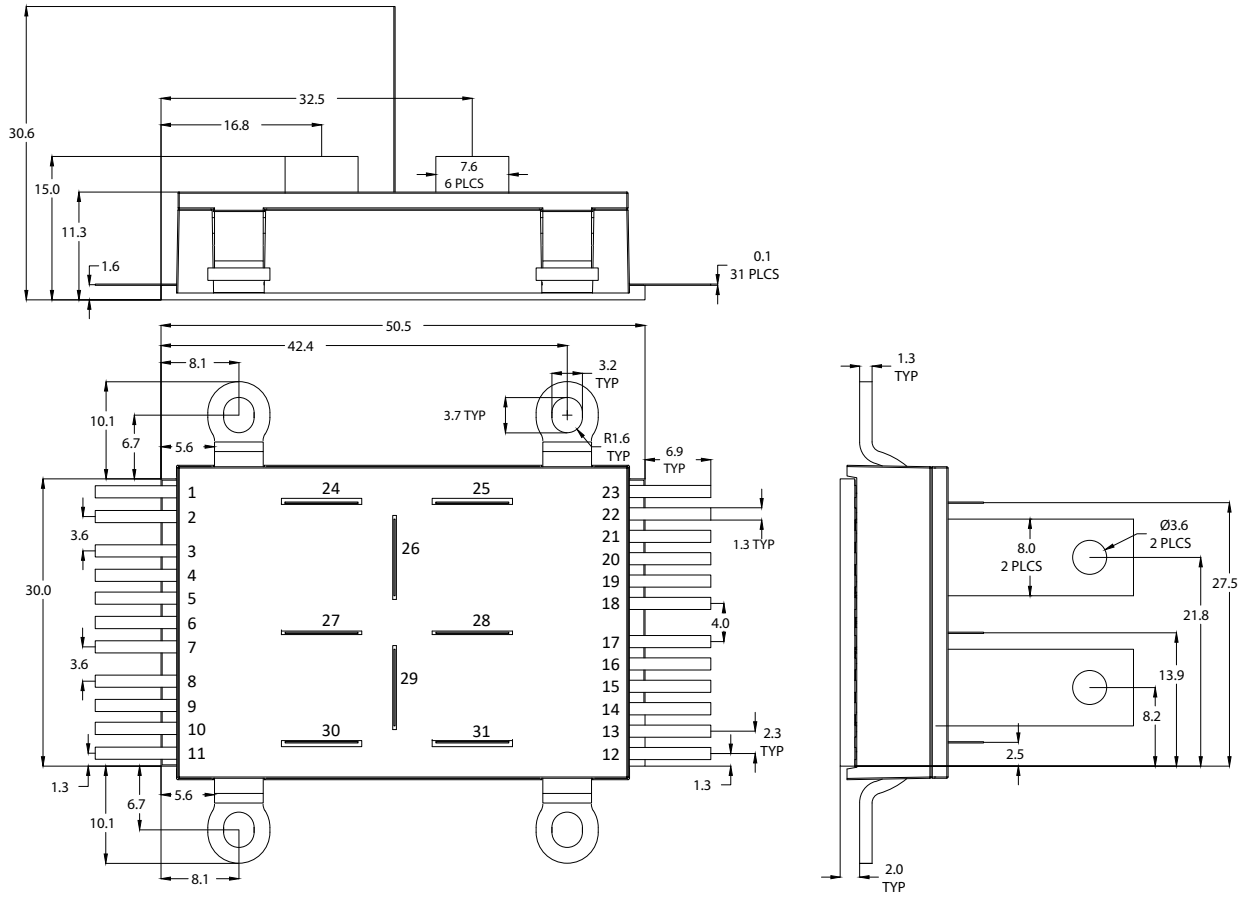
3. Package Specification

This section shows the package specification of this device.

3.1 Package Outline Drawing

The following figure illustrates the package outline of this device. The dimensions in the figure below are in millimeters.

Figure 3-1. Package Outline Drawing



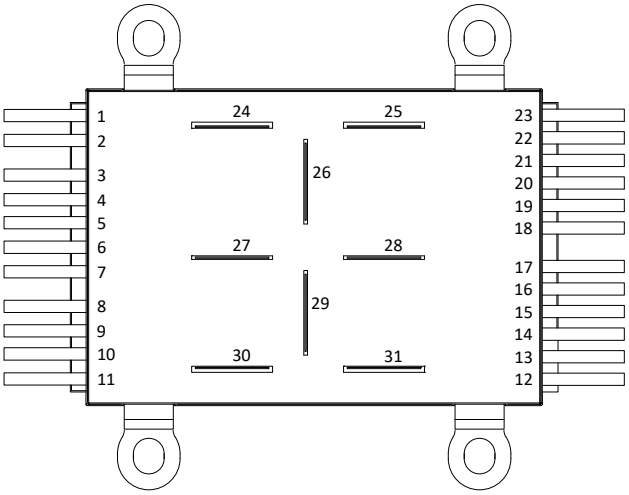
CAUTION

Hazardous Material Warning!

The white ceramic portion of the device between leads and mounting flange is beryllium oxide, BeO. Beryllium oxide dust is highly toxic when inhaled. Care must be take during handling and mounting to avoid damage to this area. These devices must never be thrown away with general industrial or domestic waste.

The following figure ilustrates the pin assignments of this device.

Figure 3-2. Pin Assignments



The following table shows the terminal pinout of this device.

Table 3-1. Terminal Pinout

Pin	Assignment	Pin	Assignment
Pin 1	PGND Low Side 1	Pin 17	FGND High Side 1
Pin 2	V_{DD} Low Side 1	Pin 18	FGND High Side 2
Pin 3	V_{in} Low Side 1	Pin 19	V_{DD} High Side 2
Pin 4	SGND Low Side 1	Pin 20	SGND High Side 2
Pin 5	V_{DD} Low Side 1	Pin 21	V_{in} High Side 2
Pin 6	PGND	Pin 22	V_{DD} High Side 2
Pin 7	V_{DD} Low Side 2	Pin 23	FGND High Side 2
Pin 8	V_{in} Low Side 2	Pin 24	Source
Pin 9	SGND Low Side 2	Pin 25	Drain
Pin 10	V_{DD} Low Side 2	Pin 26	Output 1
Pin 11	PGND Low Side 2	Pin 27	Source
Pin 12	FGND High Side 1	Pin 28	Drain
Pin 13	V_{DD} High Side 1	Pin 29	Output 2
Pin 14	SGND High Side 1	Pin 30	Source
Pin 15	V_{in} High Side 1	Pin 31	Drain
Pin 16	V_{DD} High Side 1		

Notes:

- FGND: Floating ground
- PGND: Power ground
- SGND: Signal ground

4. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 4-1. Revision History

Revision	Date	Description
C	12/2024	The following changes were made in this revision: • Updated Figures 1-2 and 1-4. • Updated values in Tables 1-1, 1-3, and 1-4. • Added explanatory circuit note below Test Configuration diagram Figure 2-2.
B	10/2024	The following changes were made in this revision: • Added Reference Design information to Product Overview section. • Added SGND definition to note in Terminal Pinout table in Package Outline Drawing section. • Updated title for Figure 1-3.
A	09/2024	Document migrated from Microsemi template to Microchip template; Assigned Microchip literature number DS-00005554A, which replaces the previous Microsemi literature number 050-4985.
Initial release (Microsemi Revisions A and B)	12/2015 – 03/2017	Initial releases.

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ISBN: 979-8-3371-0042-5

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