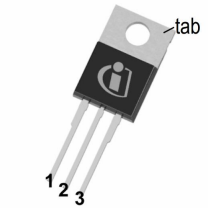
MOSFET

PG-TO220-3

StrongIRFET™2 Power-Transistor, 40 V



Features

- Optimized for wide range of applications
- N-channel, normal level
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Qualified according to JEDEC Standard

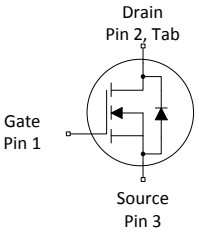
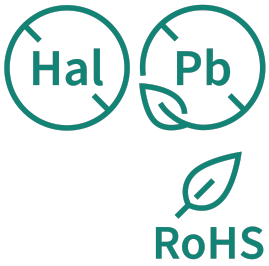


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	40	V
$R_{DS(on),max}$	2.6	mΩ
I_D	122	A
Q_{oss}	76	nC
Q_G(0V..10V)	68	nC



Type/Ordering Code	Package	Marking	Related Links
IPP026N04NF2S	PG-TO220-3	026N04NS	-

Table of Contents

1 Maximum ratings

at T_A=25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Continuous drain current [1]	I_D	-	-	122 94 29	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_A=25°C, R_{THJA}=40°C/W [2]
Pulsed drain current [3]	$I_{D,pulse}$	-	-	488	A	T_A=25 °C
Avalanche energy, single pulse [4]	E_{AS}	-	-	167	mJ	I_D=70 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	158 3.8	W	T_C=25 °C T_A=25 °C, R_{THJA}=40 °C/W [2]
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	-

[1] Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

[2] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

[3] See Diagram 3 for more detailed information

[4] See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.95	°C/W	-
Thermal resistance, junction - ambient, 6 cm² cooling area [5)]	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint	R_{thJA}	-	-	62	°C/W	-

[5)] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at T_j=25 °C, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	40	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.4	V	V_{DS}=V_{GS}, I_D=81 µA
Zero gate voltage drain current	I_{DSS}	-	0.1 10	1 100	µA	V_{DS}=40 V, V_{GS}=0 V, T_j=25 °C V_{DS}=40 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance [6]	$R_{DS(on)}$	-	2.1 2.3	2.6 3.2	mΩ	V_{GS}=10 V, I_D=70 A V_{GS}=6 V, I_D=35 A
Gate resistance	R_G	-	3.0	-	Ω	-
Transconductance [7]	g_{fs}	120	-	-	S	$\|V_{DS}\|\geq 2\|I_D\|R_{DS(on)max}$, I_D=70 A

[6] $R_{DS(on)}$ is specified at a distance of 1.8 mm distance to the package body; mounting at a larger distance increases the overall package resistance of approximately 0.04 mOhm/mm per leg.

[7] Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	4800	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Output capacitance	C_{oss}	-	1780	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	98	-	pF	V_{GS}=0 V, V_{DS}=20 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=70 A, $R_{G,ext}$=1.6 Ω
Rise time	t_r	-	15	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=70 A, $R_{G,ext}$=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	35	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=70 A, $R_{G,ext}$=1.6 Ω
Fall time	t_f	-	15	-	ns	V_{DD}=20 V, V_{GS}=10 V, I_D=70 A, $R_{G,ext}$=1.6 Ω

Table 6 Gate charge characteristics [8]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	21	-	nC	V_{DD}=20 V, I_D=70 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	14	-	nC	V_{DD}=20 V, I_D=70 A, V_{GS}=0 to 10 V
Gate to drain charge	Q_{gd}	-	13	-	nC	V_{DD}=20 V, I_D=70 A, V_{GS}=0 to 10 V

Table 6 Gate charge characteristics [8)]

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Switching charge	Q_{sw}	-	20	-	nC	V_{DD}=20 V, I_D=70 A, V_{GS}=0 to 10 V
Gate charge total [9)]	Q_g	-	68	102	nC	V_{DD}=20 V, I_D=70 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.3	-	V	V_{DD}=20 V, I_D=70 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	61	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge	Q_{oss}	-	76	-	nC	V_{DS}=20 V, V_{GS}=0 V

8) See "Gate charge waveforms" for parameter definition

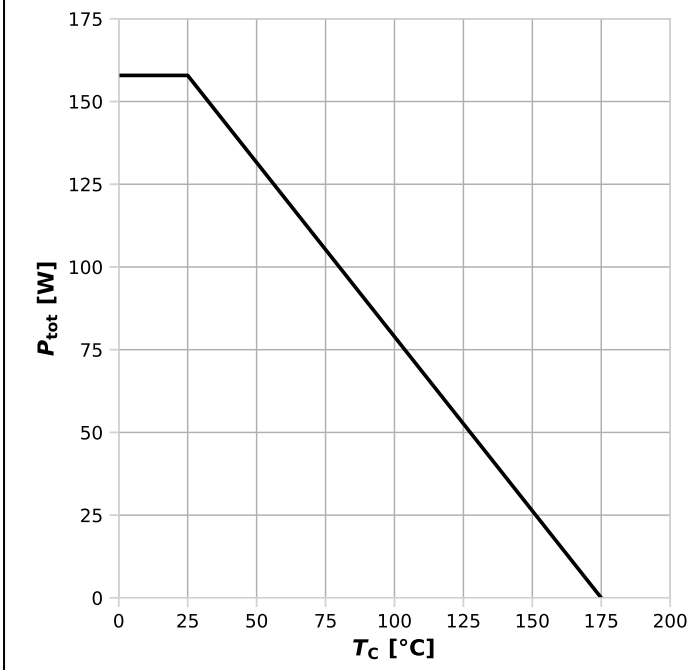
9) Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	95	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	488	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	0.88	1.1	V	V_{GS}=0 V, I_F=70 A, T_j=25 °C
Reverse recovery time	t_{rr}	-	44	-	ns	V_R=20 V, I_F=70 A, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	45	-	nC	V_R=20 V, I_F=70 A, di_F/dt=100 A/µs
Reverse recovery time	t_{rr}	-	31	-	ns	V_R=20 V, I_F=70 A, di_F/dt=500 A/µs
Reverse recovery charge	Q_{rr}	-	122	-	nC	V_R=20 V, I_F=70 A, di_F/dt=500 A/µs

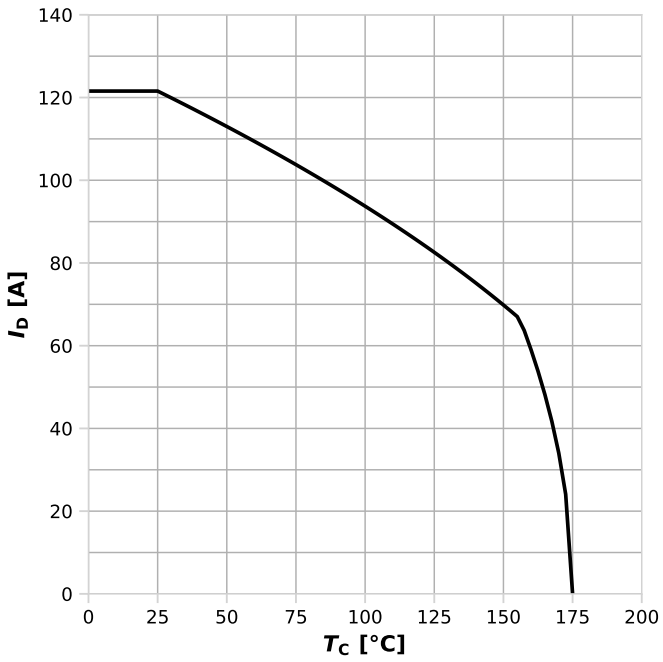
4 Electrical characteristics diagrams

Diagram 1: Power dissipation



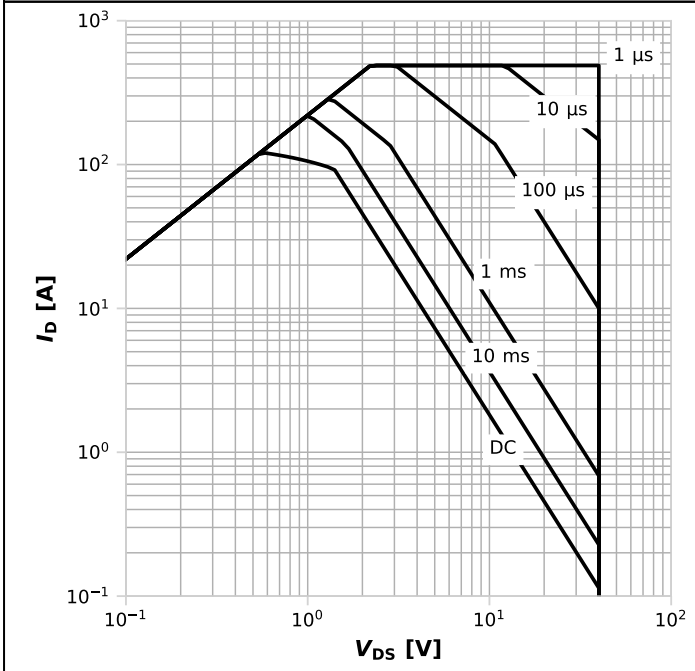
P_{tot}=f(T_C)

Diagram 2: Drain current



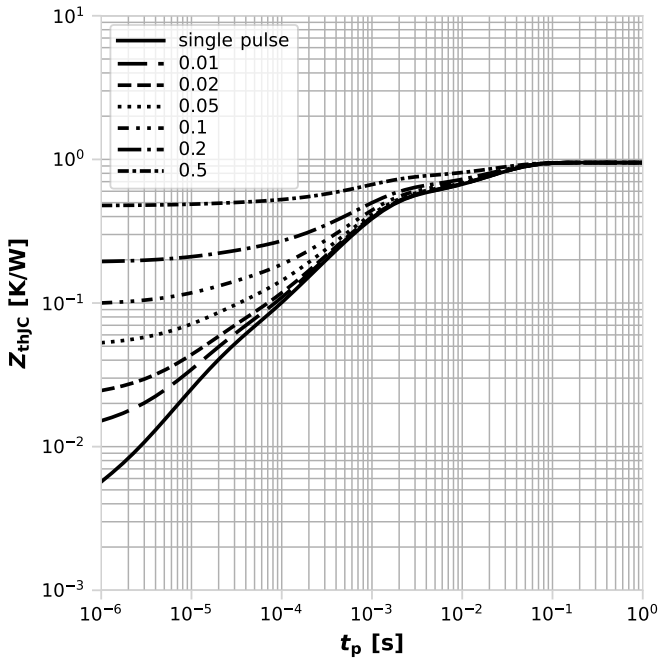
I_D=f(T_C); V_{GS}≥10 V

Diagram 3: Safe operating area



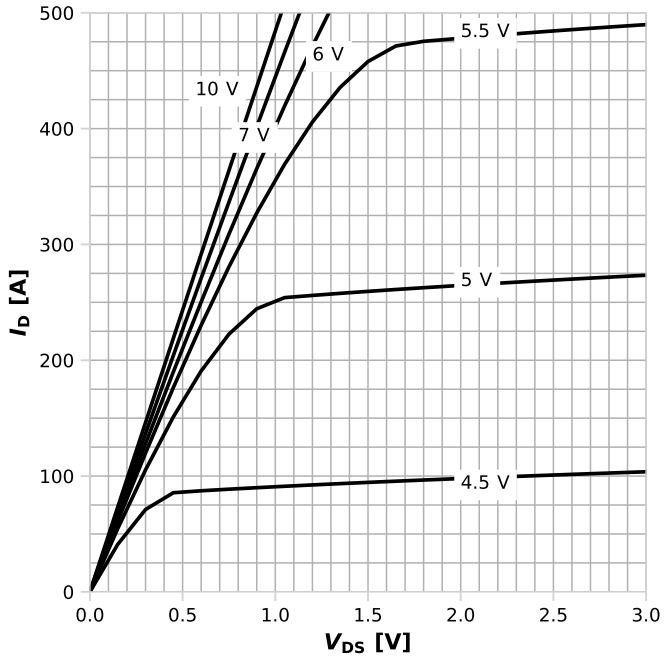
I_D=f(V_{DS}); T_C=25 °C; D=0; parameter: t_p

Diagram 4: Max. transient thermal impedance



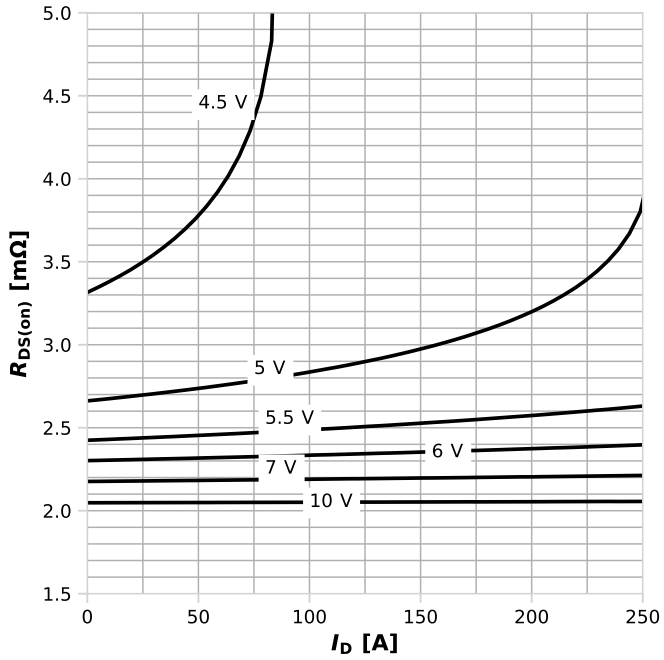
Z_{thJC}=f(t_p); parameter: D=t_p/T

Diagram 5: Typ. output characteristics



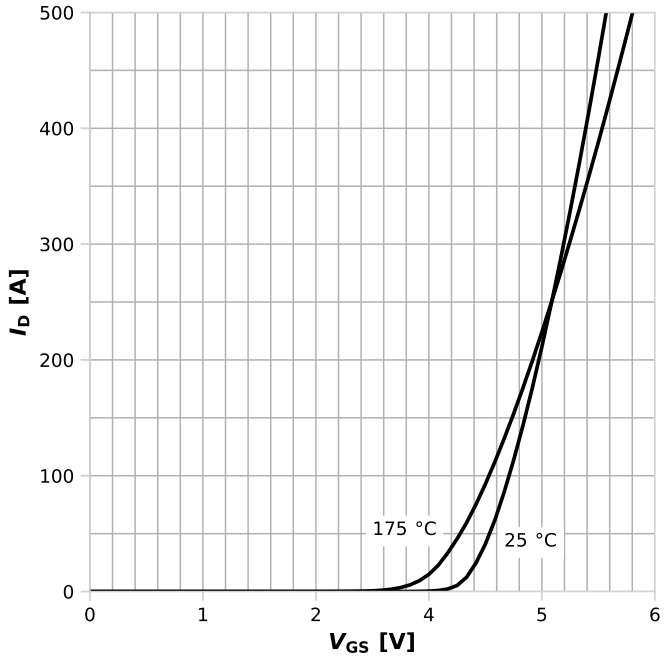
I_D=f(V_{DS}), T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



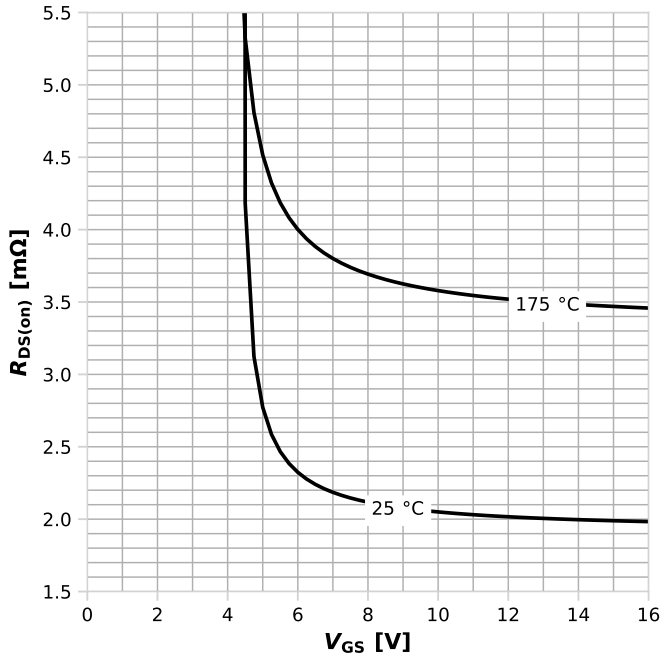
$R_{DS(on)}$=f(I_D), T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



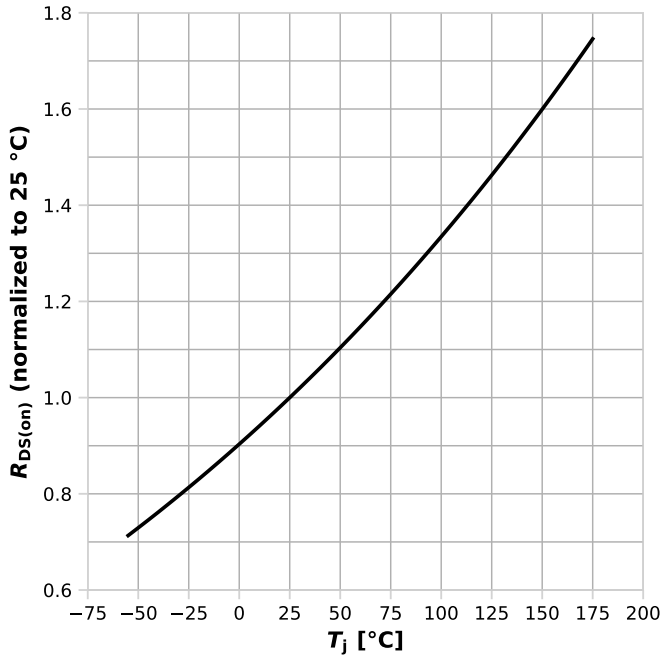
I_D=f(V_{GS}), $|V_{DS}|>2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



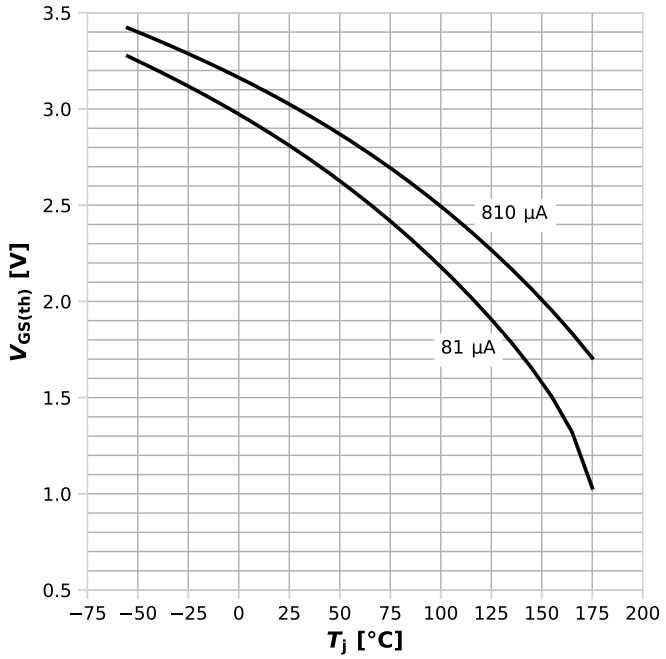
$R_{DS(on)}$=f(V_{GS}), I_D=70 A; parameter: T_j

Diagram 9: Normalized drain-source on resistance



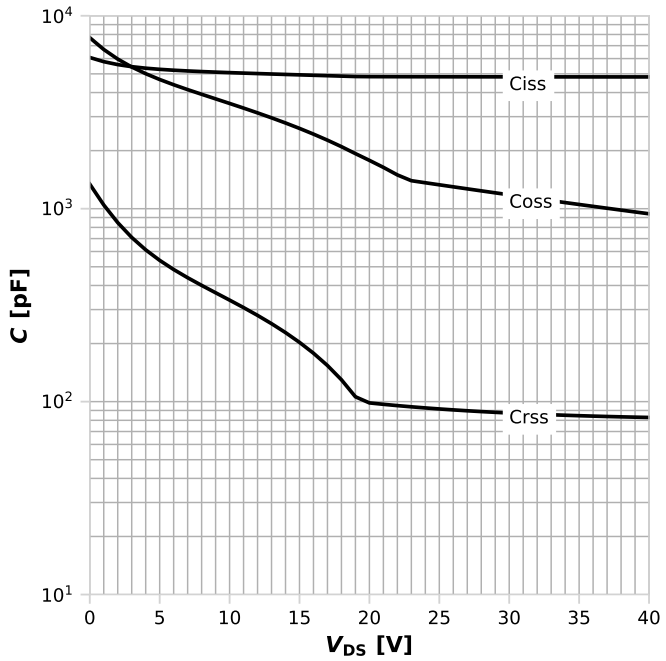
$R_{DS(on)}$=f(T_j), I_D=70 A, V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



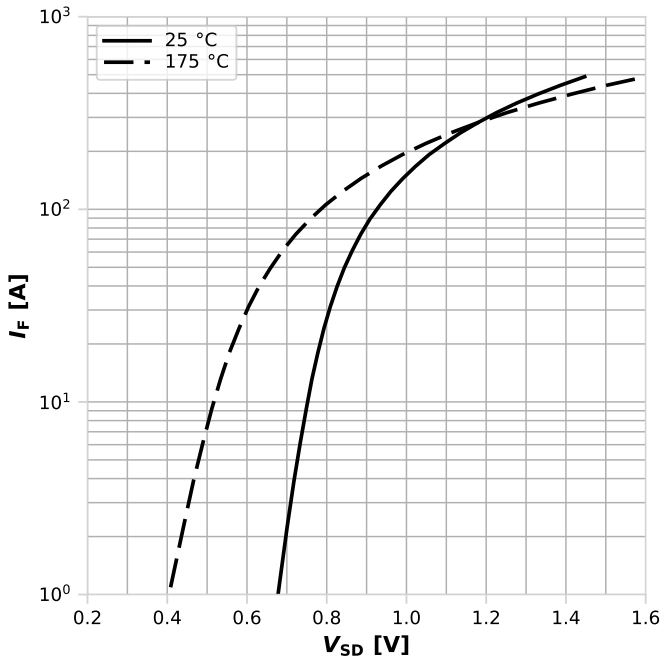
$V_{GS(th)}$=f(T_j), V_{GS}=V_{DS}; parameter: I_D

Diagram 11: Typ. capacitances



C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



I_F=f(V_{SD}); parameter: T_j

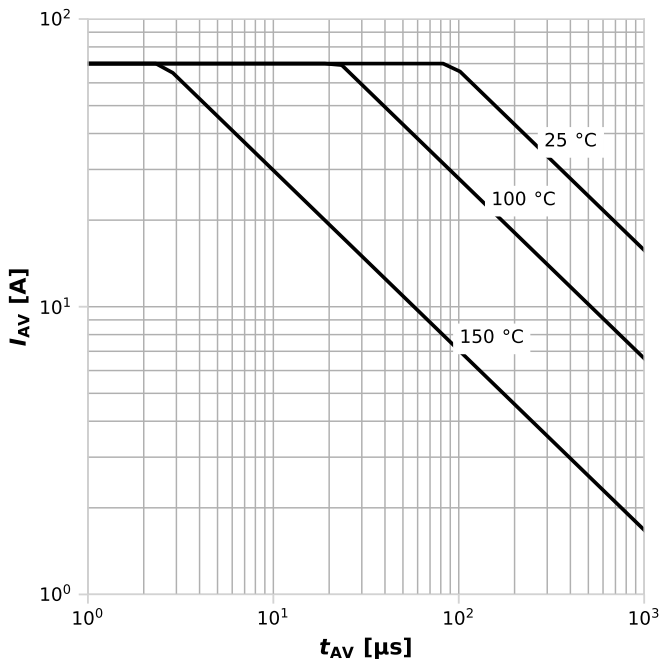
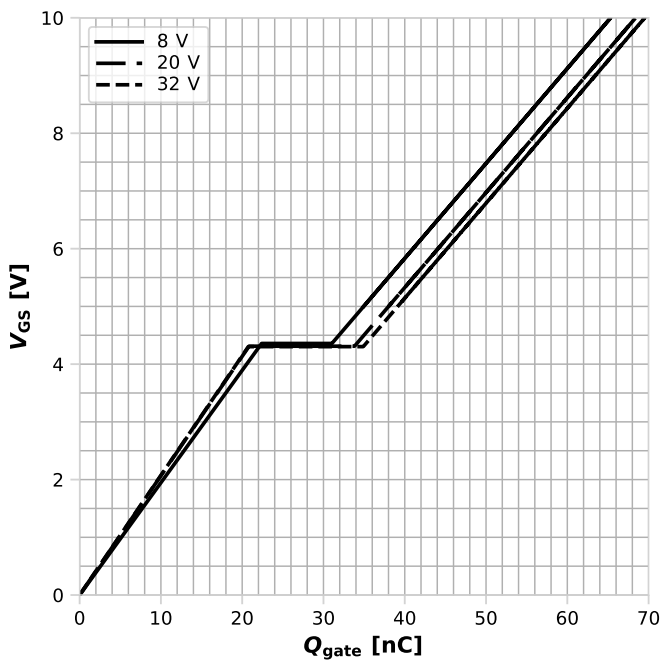
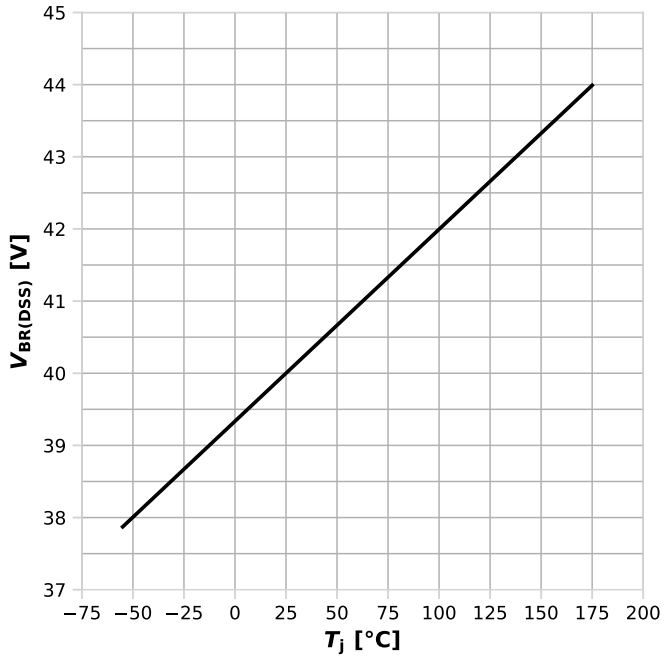
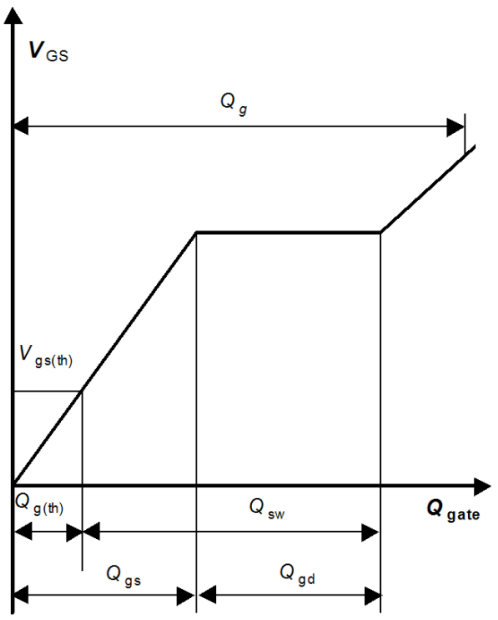
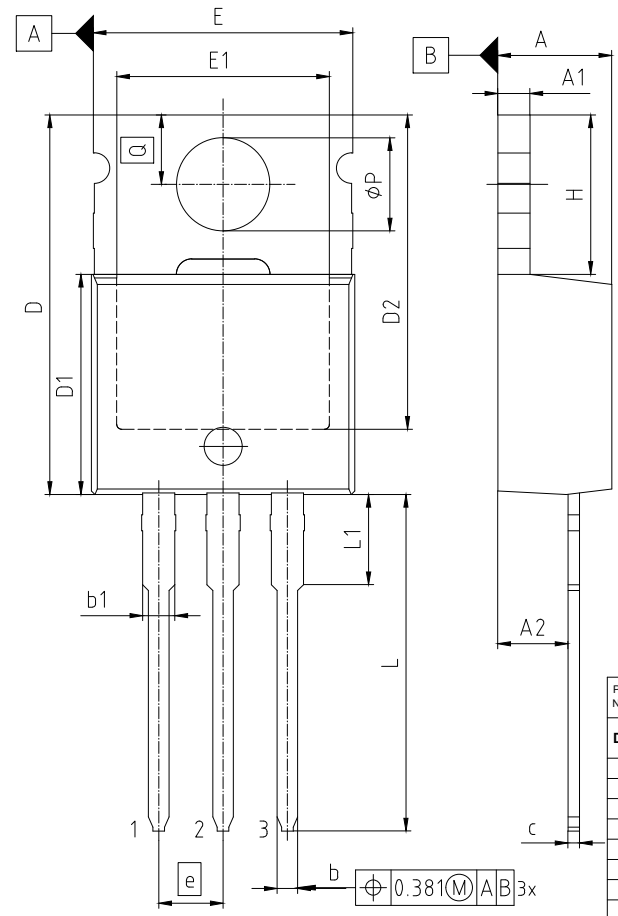
Diagram 13: Avalanche characteristics	Diagram 14: Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j,start}$	V_{GS}=f(Q_{gate}), I_D=70 A pulsed, T_j=25 °C; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage	Gate charge waveforms
	
$V_{BR(DSS)}$=f(T_j); I_D=1 mA	-

5 Package Outlines



NOTES:
DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS
GATE BURRS ARE LESS THAN 0.5 mm

PACKAGE - GROUP NUMBER:	PG-TO220-3-U05	
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	4.25	4.75
A1	1.14	1.40
A2	2.47	2.92
b	0.71	0.97
b1	1.14	1.78
c	0.36	0.61
D	14.32	15.80
D1	8.39	9.20
D2	11.89	12.80
E	9.90	10.67
E1	8.10	8.74
e	2.54	
N	3	
H	6.00	6.70
L	13.00	14.40
L1	3.56	4.06
øP	3.54	3.90
Q	2.54	2.94

Figure 1 Outline PG-TO220-3, dimensions in mm

Revision History

IPP026N04NF2S

Revision 2024-10-07, Rev. 2.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2022-06-07	Release of final version
2.1	2024-10-07	Added trr and Qrr at diF/dt=100 A/µs

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