9SQL4952/9SQL4954/9SQL4958D

3.3V PCIe® Gen1–5 and UPI Clock

The 9SQL4952/9SQL4954/9SQL4958D devices comprise a family of 3.3V PCIe Gen1–5 clock generators with UPI support. There are 2, 4 and 8 outputs versions available and each differential output has a dedicated OE# pin supporting PCIe CLKREQ# functionality.

Applications

- Servers/High-Performance Computing
- nVME Storage
- Networking
- Accelerators
- Industrial Control

Key Specifications

- 90fs RMS typical jitter (PCIe Gen5 CC)
- 70fs RMS typical jitter (QPI ≤ 11.4Gb/s, 12UI)
- < 50ps cycle-to-cycle jitter on differential outputs
- < 50ps output-to-output skew on differential outputs
- ±0ppm synthesis error on differential outputs

Output Features

- 2, 4 or 8 100MHz CPU/PCIe output pairs
- One 3.3V LVCMOS REF output with Wake-On-LAN (WOL) support
- See AN-891 for AC-coupling to other logic families

Features

- Integrated terminations for 85Ω systems
- 112–206 mW typical power consumption (at 3.3V)
- VDDIO rail allows 35% power savings at optional 1.05V (9SQL4958 only)
- Devices contain default configuration; SMBus not required
- SMBus features allow optimization to application:
  - Input polarity and pull-up/pull-downs
  - Output slew rate and amplitude
  - Output impedance (33Ω, 85Ω or 100Ω)
- Contact factory for customized default configurations
- 25MHz input frequency
- OE# pins support PCIe CLKREQ# function
- Pin-selectable SRnS 0%, CC 0% and CC/SRIS -0.5% spread
- SMBus-selectable CC/SRIS -0.25% spread
- Clean switching between CC/SRIS spread settings
- BCLK outputs blocked until PLL is locked for clean system startup
- Two selectable SMBus addresses
- Space-saving packages (see Ordering Information)

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum (SRIS, SRNS)

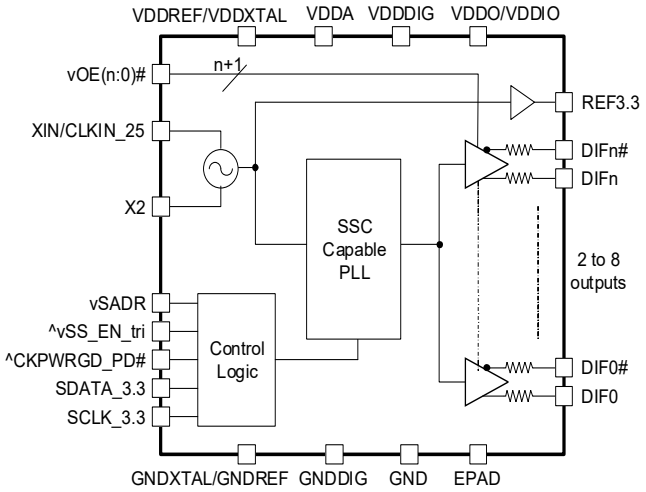
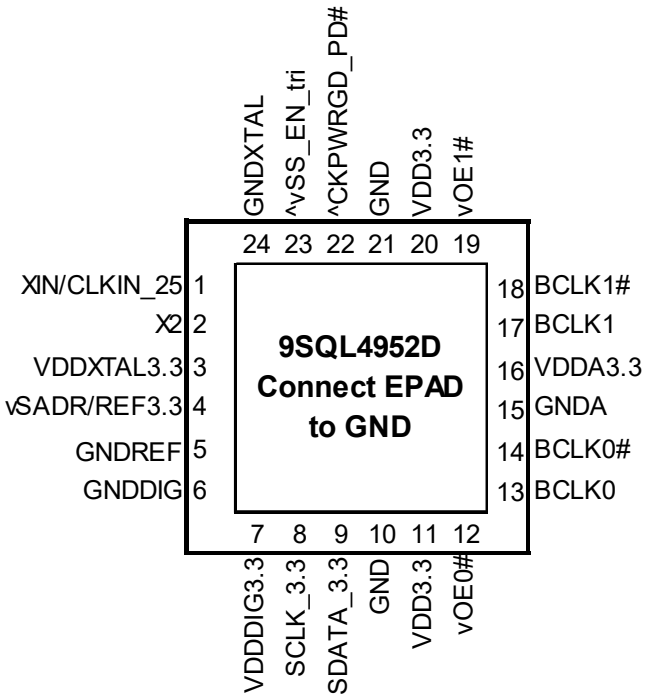


Figure 1. Block Diagram

Contents

1. Pin Information

1.1 9SQL4952D Pin Assignment



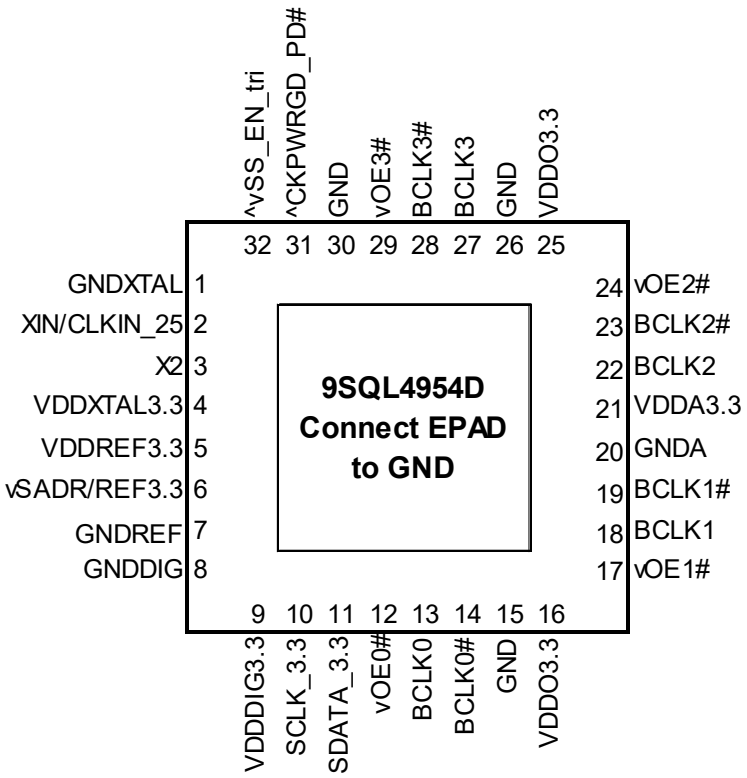
24-VFQFPN, 4 x 4 mm, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

Figure 2. Pin Assignments for 4 × 4 mm 24-VFQFPN Package – Top View

1.2 9SQL4954D Pin Assignment



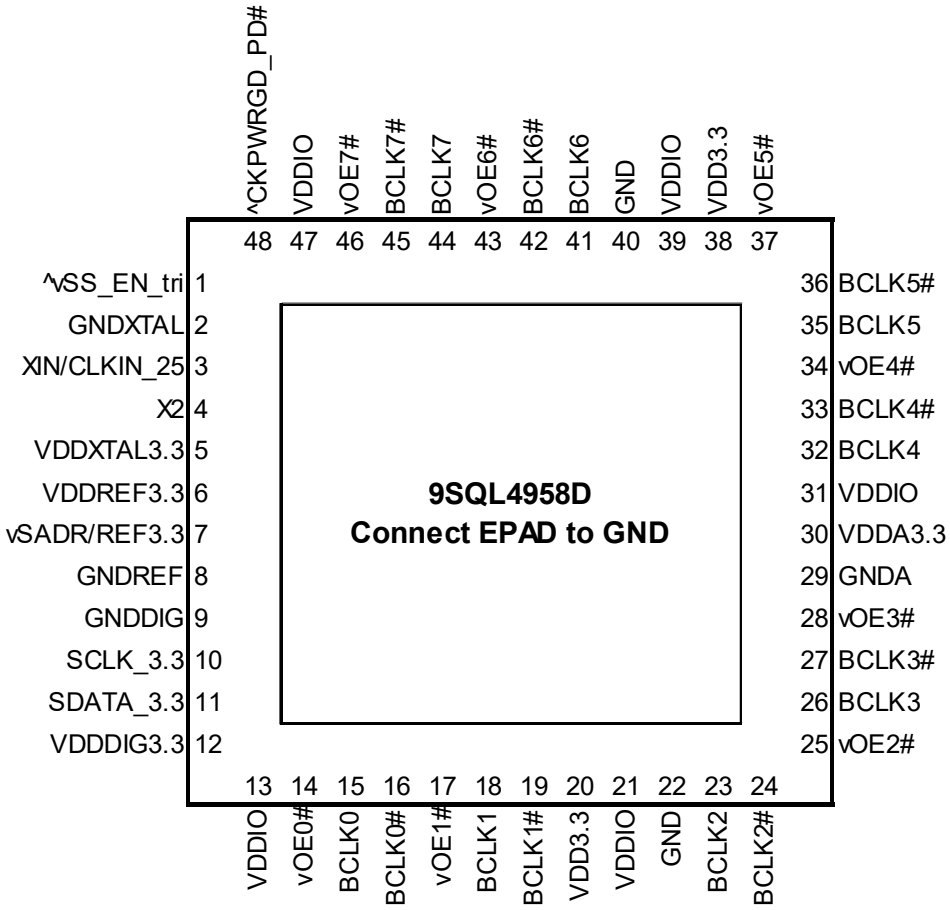
32-VFQFPN, 5 x 5 mm, 0.5mm pitch

^ prefix indicates internal 120kOhm pull-up resistor

v prefix indicates internal 120kOhm pull-down resistor

Figure 3. Pin Assignments for 5 × 5 mm 32-VFQFPN Package – Top View

1.3 9SQL4958D Pin Assignment



48-VFQFPN, 6 x 6 mm, 0.4mm pitch

^v prefix indicates internal 60kOhm pull-down resistor

v prefix indicates internal 120kOhm pull-down resistor

^ prefix indicates internal 120kOhm pull-up resistor

Figure 4. Pin Assignments for 6 × 6 mm 48-VFQFPN Package – Top View

1.4 Pin Descriptions

Name	Type	Description	9SQL4958 Pin No.	9SQL4954 Pin No.	9SQL4952 Pin No.
^CKPWRGD_PD#	Input	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode. This pin has internal pull-up resistor.	48	31	22
^vSS_EN_tri	Latched In	Latched select input to select spread spectrum amount at initial power up. See <Hyperlink>Spread Selection table.	1	32	23
BCLK0	Output	True output of differential BCLK.	15	13	13
BCLK0#	Output	Complement output of differential BCLK.	16	14	14
BCLK1	Output	True output of differential BCLK.	18	18	17
BCLK1#	Output	Complement output of differential BCLK.	19	19	18
BCLK2	Output	True output of differential BCLK.	23	22	-

Name	Type	Description	9SQL4958 Pin No.	9SQL4954 Pin No.	9SQL4952 Pin No.
BCLK2#	Output	Complement output of differential BCLK.	24	23	-
BCLK3	Output	True output of differential BCLK.	26	27	-
BCLK3#	Output	Complement output of differential BCLK.	27	28	-
BCLK4	Output	True output of differential BCLK.	32	-	-
BCLK4#	Output	Complement output of differential BCLK.	33	-	-
BCLK5	Output	True output of differential BCLK.	35	-	-
BCLK5#	Output	Complement output of differential BCLK.	36	-	-
BCLK6	Output	True output of differential BCLK.	41	-	-
BCLK6#	Output	Complement output of differential BCLK.	42	-	-
BCLK7	Output	True output of differential BCLK.	44	-	-
BCLK7#	Output	Complement output of differential BCLK.	45	-	-
EPAD	GND	Connect to ground.	49	33	25
GND	GND	Ground pin.	22	15	10
GND	GND	Ground pin.	40	26, 30	21
GNDA	GND	Ground pin for the PLL core.	29	20	15
GNDDIG	GND	Ground pin for digital circuitry.	9	8	6
GNDREF	GND	Ground pin for the REF outputs.	8	7	5
GNDXTAL	GND	GND for XTAL.	2	1	24
SCLK_3.3	Input	Clock pin of SMBus circuitry, 3.3V tolerant.	10	10	8
SDATA_3.3	I/O	Data pin for SMBus circuitry, 3.3V tolerant.	11	11	9
VDD3.3	Power	Power supply, nominally 3.3V.	20	16	11
VDD3.3	Power	Power supply, nominally 3.3V.	38	25	20
VDDA3.3	Power	3.3V power for the PLL core.	30	21	16
VDDDIG3.3	Power	3.3V digital power (dirty power).	12	9	7
VDDIO	Power	Power supply for differential outputs.	13	-	-
VDDIO	Power	Power supply for differential outputs.	21	-	-
VDDIO	Power	Power supply for differential outputs.	31	-	-
VDDIO	Power	Power supply for differential outputs.	39	-	-
VDDIO	Power	Power supply for differential outputs.	47	-	-
VDDREF3.3	Power	Power supply for REF output, nominally 3.3V.	6	5	-
VDDXTAL3.3	Power	Power supply for XTAL, nominally 3.3V.	5	4	3
vOE0#	Input	Active low input for enabling output 0. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	14	12	12
vOE1#	Input	Active low input for enabling output 1. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	17	17	19

Name	Type	Description	9SQL4958 Pin No.	9SQL4954 Pin No.	9SQL4952 Pin No.
vOE2#	Input	Active low input for enabling output 2. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	25	24	-
vOE3#	Input	Active low input for enabling output 3. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	28	29	-
vOE4#	Input	Active low input for enabling output 4. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	34	-	-
vOE5#	Input	Active low input for enabling output 5. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	37	-	-
vOE6#	Input	Active low input for enabling output 6. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	43	-	-
vOE7#	Input	Active low input for enabling output 7. This pin has an internal pull-down. 1 = disable output, 0 = enable output.	46	-	-
vSADR/REF3.3	Latched I/O	Latch to select SMBus Address/3.3V LVCMOS copy of X1/REFIN pin	7	6	4
X2	Output	Crystal output.	4	3	2
XIN/CLKIN_25	Input	Crystal input or Reference Clock input. nominally 25MHz.	3	2	1

Table 1. Spread Selection

^vSS_EN_tri Pin	B1[4:3]	Spread%	Note
0	00	0	12kHz to 20MHz mode.
-	01	-0.25	PCIe Common Clock or SRIS mode.
M (VDD/2)	10	0	PCIe Common Clock, SRIS, or SNS mode.
1	11	-0.50	PCIe Common Clock or SRIS mode.

If 12kHz to 20MHz mode is desired, power up with ^vSS_EN_tri = '0'. Do not attempt to switch to the other modes via SMBus control in Byte 1 or a system reset will be required. If Common Clock (CC) or SRIS mode is desired, power up with ^vSS_EN_tri at either 'M' or '1'. The desired spread spectrum amount can then be selected via Byte 1 without a requiring a system reset. Once 'M' or '1' is latched at power up, do not attempt to enter 12kHz to 20MHz mode or a system reset will be required.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Maximum	Unit
3.3V Supply Voltage [1][2]	V_{DDxx}	Applies to VDD, VDDA and VDDIO, if present.	-0.5	3.9	V
Input Voltage [1][3]	V_{IN}		-0.5	V_{DD} + 0.5	V
Input High Voltage, SMBus[1]	V_{IHSMB}	SMBus clock and data pins.	-	3.9	V
Storage Temperature[1]	Ts		-65	150	°C
Junction Temperature[1]	Tj		-	125	°C
Input ESD Protection[1]	ESD prot	Human Body Model.	2500	-	V

1. Confirmed by design and characterization, not 100% tested in production.
2. Operation under these conditions is neither implied nor guaranteed.
3. Not to exceed 4.6V.

2.2 Thermal Characteristics

Table 3. Thermal Characteristics [1]

Parameter	Symbol	Conditions	Package	Typical Values	Unit
9SQL4952 Thermal Resistance	θ_{JC}	Junction to case.	NLG24	62	°C/W
	θ_{Jb}	Junction to base.		5.4	
	θ_{JA0}	Junction to air, still air.		50	
	θ_{JA1}	Junction to air, 1 m/s air flow.		43	
	θ_{JA3}	Junction to air, 3 m/s air flow.		39	
	θ_{JA5}	Junction to air, 5 m/s air flow.		38	
9SQL4954 Thermal Resistance	θ_{JC}	Junction to case.	NLG32	42	°C/W
	θ_{Jb}	Junction to base.		2.4	
	θ_{JA0}	Junction to air, still air.		39	
	θ_{JA1}	Junction to air, 1 m/s air flow.		33	
	θ_{JA3}	Junction to air, 3 m/s air flow.		28	
	θ_{JA5}	Junction to air, 5 m/s air flow.		27	
9SQL4958 Thermal Resistance	θ_{JC}	Junction to case.	NDG48	33	°C/W
	θ_{Jb}	Junction to base.		2.1	
	θ_{JA0}	Junction to air, still air.		37	
	θ_{JA1}	Junction to air, 1 m/s air flow.		30	
	θ_{JA3}	Junction to air, 3 m/s air flow.		27	
	θ_{JA5}	Junction to air, 5 m/s air flow.		26	

1. EPAD soldered to board.

2.3 Electrical Characteristics

$T_A = T_{AMB}$. Supply voltages per normal operation conditions; see Test Loads for loading conditions.

Table 4. SMBus Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
SMBus Input Low Voltage	V_{ILSMB}	V_{DDSMB} = 3.3V.	-	-	0.8	V
SMBus Input High Voltage	V_{IHSMB}	V_{DDSMB} = 3.3V.	2.1	-	3.6	V
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP}.	-	-	0.4	V
SMBus Sink Current	I_{PULLUP}	At V_{OL}.	4	-	-	mA
Nominal Bus Voltage	V_{DDSMB}		2.7	-	3.6	V
SCLK/SDATA Rise Time [1]	t_{RSMB}	(Max. V_{IL} - 0.15V) to (Min. V_{IH} + 0.15V).	-	-	1000	ns
SCLK/SDATA Fall Time [1]	t_{FSMB}	(Min. V_{IH} + 0.15V) to (Max. V_{IL} - 0.15V).	-	-	300	ns
SMBus Operating Frequency [2]	f_{SMB}	SMBus operating frequency.	-	-	500	kHz

1. Confirmed by design and characterization, not 100% tested in production.
2. The device must be powered up for the SMBus to function.

Table 5. Input/Supply/Common Parameters – Normal Operating Conditions

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DDxxx}	Supply voltage for core, analog and single-ended LVCMOS outputs.	3.135	3.3	3.465	V
IO Supply Voltage	V_{DDIO}	Supply voltage for differential low power outputs.	0.9975	1.05–3.3	3.465	V
Ambient Operating Temperature	T_{AMB}	Industrial range.	-40	25	85	°C
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus.	0.75 x V_{DDx}	-	V_{DDx} + 0.3	V
Input Low Voltage	V_{IL}		-0.3	-	0.25 x V_{DDx}	V
Input High Voltage	V_{IHtri}	Single-ended tri-level inputs ('_tri' suffix).	0.8 x V_{DDx}	-	V_{DDx} + 0.3	V
Input Mid Voltage	V_{IMtri}		0.4 x V_{DDx}	0.5 x V_{DDx}	0.6 x V_{DDx}	V
Input Low Voltage	V_{ILtri}		-0.3	-	0.20 x V_{DDx}	V
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5	-	5	µA
	I_{INP}	Single-ended inputs. V_{IN} = 0V; inputs with internal pull-up resistors. V_{IN} = V_{DD}; inputs with internal pull-down resistors.	-50	-	50	µA
Input Frequency [1]	F_{IN}	XTAL or X1 input.	-	25	-	MHz
Pin Inductance [2]	L_{pin}		-	-	7	nH
Capacitance	C_{IN}	Logic inputs, except DIF_IN. [2]	1.5	-	5	pF
	C_{OUT}	Output pin capacitance. [2]	-	-	6	pF
CLK Stabilization [2][3]	t_{STAB}	From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock.	-	0.3	1.8	ms
SS Modulation Frequency [2]	f_{MOD}	Triangular modulation.	30	31.6	33	kHz
OE# Latency [2][4]	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	3	4	5	clocks
Fall Time [2][3]	t_F	Fall time of single-ended control inputs.	-	-	5	ns
Rise Time [2][3]	t_R	Rise time of single-ended control inputs.	-	-	5	ns

1. Contact the factory for other frequencies.
2. Confirmed by design and characterization, not 100% tested in production.
3. Control input must be monotonic from 20% to 80% of input swing.
4. Time from deassertion until outputs are > 200mV.

Table 6. Differential Low-Power HCSL Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Slew Rate	Trf	Scope averaging on, fast setting. [1] [2]	3.0	3.8	4.6	V/ns
		Scope averaging, slow setting. [1] [2]	2.0	2.7	3.5	V/ns
Crossing Voltage (abs)	Vcross_abs	Scope averaging off. [3] [4] [5]	250	429	550	mV
Crossing Voltage (var)	Δ-Vcross	Scope averaging off. [3] [4] [6]	-	26	140	mV
Avg. Clock Period Accuracy	T_{PERIOD_AVG}	6V4146x devices have 0 ppm synthesis error. -0.5% SSC. [1] [7] [8] [9]	-	0	+2500	ppm
		-.025% SSC	-	0	+1250	
Absolute Period	T_{PERIOD_ABS}	Includes jitter and spread spectrum modulation. [1] [10]	9.95	10	10.0503	ns
Jitter, Cycle to Cycle [1]	$t_{jcyc-cyc}$	-	-	16	50	ps
Voltage High [3]	V_{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	790	850	mV
Voltage Low [3]	V_{LOW}		-150	-4	150	mV
Absolute Maximum Voltage [3] [11] [12]	V_{MAX}	Measurement on single-ended signal using absolute value (scope averaging off).	-	832	1150	mV
Absolute Minimum Voltage [3] [12] [13]	V_{MIN}		-300	-61	-	
Duty Cycle [1]	t_{DC}	-	45	49	55	%
Slew Rate Matching [3] [14]	ΔTrf	Single-ended measurement.	-	9	20	%
Skew, Output to Output [1]	t_{sk3}	Averaging on, V_T = 50%.	-	32	50	ps

1. Measured from differential waveform.
2. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
3. Measured from single-ended waveform.
4. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
5. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
6. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.
7. Refer to Section 8.6.2 of the PCI Express Base Specification, Revision 5.0 for information regarding PPM considerations.
8. PCIe Gen1 through Gen4 specify ±300ppm frequency tolerances. PCIe Gen5 reduces the allowable tolerance to ±100ppm without spread spectrum.
9. “ppm” refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100ppm, then we have an error budget of 100Hz/ppm × 100ppm = 10kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±100ppm applies to systems that do not employ Spread Spectrum clocking, or that use common clock source. For systems employing Spread Spectrum clocking, there is an additional 2,500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600ppm for Common Clock architectures. Separate Reference Clock architectures may have a lower allowed spread percentage.
10. Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation.
11. Defined as the maximum instantaneous voltage including overshoot.
12. At default SMBus amplitude settings.

13. Defined as the minimum instantaneous voltage including undershoot.
14. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.
15. System board compliance measurements must use the test load. REFCLK+ and REFCLK- are to be measured at the load capacitors C_L. Single-ended probes must be used for measurements requiring single ended measurements. Either single-ended probes with math or differential probe can be used for differential measurements. Test load C_L = 2pF.

Table 7. 12kHz–20MHz Phase Jitter of Differential Outputs

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Phase Jitter, 12kHz–20MHz	$t_{jph12k20M}$	100MHz outputs with REF output enabled SSC Off	-	2.0	2.1	ps (rms)

Table 8. Current Consumption – 9SQL4952

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Supply Current	I_{DDAOP}	V_{DDA}, all outputs active at 100MHz.	-	13	17	mA
	I_{DDOP}	All V_{DD}, except V_{DDA}, all outputs active at 100MHz.	-	18	23	mA
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I_{DDAPD}	V_{DDA}, DIF outputs off, REF output running. [1]	-	0.9	1.5	mA
	I_{DDPD}	All V_{DD}, except V_{DDA}, DIF outputs off, REF output running. [1]	-	5.7	8	mA
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I_{DDAPD}	V_{DDA}, all outputs off.	-	0.9	1.5	mA
	I_{DDPD}	All V_{DD}, except V_{DDA}, all outputs off.	-	1.7	2.5	mA

1. This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 9. Current Consumption – 9SQL4954

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Supply Current	I_{DDAOP}	V_{DDA}, all outputs active at 100MHz.	-	13	17	mA
	I_{DDOP}	All V_{DD}, except V_{DDA}, all outputs active at 100MHz.	-	30	39	mA
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I_{DDAPD}	V_{DDA}, DIF outputs off, REF output running. [1]	-	0.9	1.5	mA
	I_{DDPD}	All other V_{DD}, except V_{DDA}, DIF outputs off, REF output running. [1]	-	5.9	8.0	mA
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I_{DDAPD}	V_{DDA}, all outputs off.	-	0.9	1.5	mA
	I_{DDPD}	All other V_{DD}, except V_{DDA}, all outputs off.	-	1.5	2.5	mA

1. This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 10. Current Consumption – 9SQL4958

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Operating Supply Current	I_{DDAOP}	V_{DDA}, all outputs active at 100MHz.	-	14	19	mA
	I_{DDOP}	All V_{DD}, except V_{DDA} and V_{DDIO}, all outputs active at100MHz.	-	18	24	mA
	I_{DDIOOP}	V_{DDIO}, all outputs active at 100MHz.	-	30	37	mA
Wake-on-LAN Current (Power down state and Byte 3, bit 5 = '1')	I_{DDAPD}	V_{DDA}, DIF outputs off, REF output running. [1]	-	0.9	1.5	mA
	I_{DDPD}	All V_{DD}, except V_{DDA} and V_{DDIO}, DIF outputs off, REF output running. [1]	-	5.2	8	mA
	I_{DDIOOP}	V_{DDIO}, DIF outputs off, REF output running. [1]	-	0.04	0.1	mA
Power Down Current (Power down state and Byte 3, bit 5 = '0')	I_{DDAPD}	V_{DDA}, all outputs off.	-	0.9	1.5	mA
	I_{DDPD}	All V_{DD}, except V_{DDA} and V_{DDIO}, all outputs off.	-	1.7	2.5	mA
	I_{DDIOOP}	V_{DDIO}, all outputs off.	-	0.04	0.1	mA

1. This is the current required to have the REF output running in Wake-on-LAN mode (Byte 3, bit 5 = 1).

Table 11. PCIe Phase Jitter of Differential Outputs

T_{AMB} = over the specified operating range. Supply voltages per normal operation conditions. See Test Loads for loading conditions.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Limit	Unit
PCIe Phase Jitter (Common Clocked Architecture)	$t_{jphPCIeG1-CC}$	PCIe Gen1 (2.5 GT/s) [1][2][3]		9,683	12,771	86,000	fs (p-p)
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Hi Band (5.0 GT/s) [1][2][3]		297	415	3,100	fs (RMS)
		PCIe Gen2 Lo Band (5.0 GT/s) [1][2]		377	531	3,000	
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (8.0 GT/s) [1][2][3][4]		177	228	1,000	
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (16.0 GT/s) [1][2][3][4][5]		177	228	500	
	$t_{jphPCIeG5-CC}$	PCIe Gen5 (32.0 GT/s) [1][2][3][4][6]		61	85	150	
PCIe Phase Jitter (SRIS Architecture) SSC = 0.5%	$t_{jphPCIeG2-SRIS}$	PCIe Gen2 (5.0 GT/s) [2]		1,422	1,503	N/A	fs (RMS)
	$t_{jphPCIeG3-SRIS}$	PCIe Gen3 (8.0 GT/s) [2]		559	595		
	$t_{jphPCIeG4-SRIS}$	PCIe Gen4 (16.0 GT/s) [2]		411	452		
PCIe Phase Jitter (SRIS Architecture) SSC = 0.25%	$t_{jphPCIeG5-SRIS}$	PCIe Gen5 (32.0 GT/s) [2]		126	159		
PCIe Phase Jitter SRNS Architecture - SSC =0% (Byte1[4:3] = 10, SS_EN_tri = M)	tjphPCIeG2-SRNS	PCIe Gen2 (5 GT/s) [2]	-	696	780	N/A	fs (RMS)
	tjphPCIeG3-SRNS	PCIe Gen3 (8 GT/s) [2]	-	255	318		
	tjphPCIeG4-SRNS	PCIe Gen4 (16 GT/s) [2]	-	259	315		
	tjphPCIeG5-SRNS	PCIe Gen5 (32 GT/s) [2]	-	111	167		

1. The REFCLK jitter is measured after applying the filter functions found in PCI Express Base Specification 5.0, Revision 1.0. See the Test Loads section of the data sheet for the exact measurement setup. Values for the Common Clock architecture are calculated for CC/SRIS spread off and spread on at -0.5%. SRIS values are calculated for CC/SRIS spread off and spread on at ≤-0.3%. If oscilloscope data is used, equipment noise is removed from all results.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.
3. Calculated for Byte1[4:3] spread settings of 01, 10 and 11.
4. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
5. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.

Table 12. REF Output

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Unit
Long Accuracy	ppm	See Tperiod min-max values. [1] [2]		0		ppm
Clock Period	T_{period}	REF output. [2]		40		ns
High Output Voltage	V_{HIGH}	I_{OH} = -2mA.	0.8 x V_{DDREF}	-	-	V
Low Output Voltage	V_{LOW}	I_{OL} = 2mA.	-	-	0.2 x V_{DDREF}	V
Rise/Fall Slew Rate	t_{rf1}	Byte 3 = 1F, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 × V_{DD}. [1]	0.5	0.9	1.5	V/ns
	t_{rf1}	Byte 3 = 5F, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 × V_{DD}. [1][3]	1.0	1.5	2.5	V/ns
	t_{rf1}	Byte 3 = 9F, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 × V_{DD}. [1]	1.5	2.1	3.1	V/ns
	t_{rf1}	Byte 3 = DF, V_{OH} = 0.8 × V_{DD}, V_{OL} = 0.2 × V_{DD}. [1]	2.0	2.7	3.8	V/ns
Duty Cycle	d_{t1X}	V_T = V_{DD}/2 V. [1][4]	45	49.7	55	%
Jitter, Cycle to Cycle	$t_{jcyc-cyc}$	V_T = V_{DD}/2 V. [1][4]	-	35	125	ps
Noise Floor	t_{jdBc1k}	1kHz offset. [1][4]	-	-132	-115	dBc
	$t_{jdBc10k}$	10kHz offset to Nyquist. [1][4]	-	-150	-140	dBc
Jitter, Phase	t_{jphREF}	12kHz to 5MHz, DIF SSC off. [1][4]	-	0.13	0.3	ps (rms)
		12kHz to 5MHz, DIF SSC on.[1][4]	-	1.4	1.5	

1. Confirmed by design and characterization, not 100% tested in production.
2. All Long Term Accuracy and Clock Period specifications are guaranteed assuming that REF is trimmed to 25.00MHz.
3. Default SMBus value.
4. When driven by a crystal.
5. Does not apply to the 6V41466 devices.

3. Power Management

Table 13. Power Management [1]

CKPWRGD_PD #	SMBus OE bit	OEx# Pin	Differential Output		REF
			True O/P	Comp. O/P	
0	X	X	Low [2]	Low [2]	Hi-Z [3]
1	1	0	Running	Running	Running
1	1	1	Disabled [2]	Disabled [2]	Running
1	0	X	Disabled [2]	Disabled [2]	Disabled[4]

1. Input polarities defined at default values.
2. The output state is set by B11[1:0] (Low/Low default).
3. REF is Hi-Z until the 1st assertion of CKPWRGD_PD# high. After this, when CKPWRG_PD# is low, REF is disabled unless Byte3[5] = 1, in which case REF is running.
4. See SMBus description for Byte 3, bit 4.

Table 14. SMBus Address Selection

	SADR	Address	+ Read/Write Bit
State of SADR on first application of CKPWRGD_PD#	0	1101000	X
	1	1101010	X

4. Test Loads

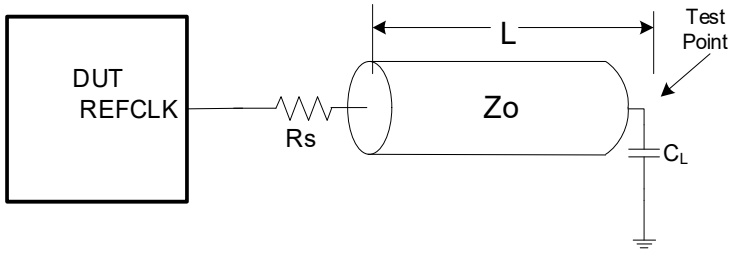


Figure 5. Single-ended Output Test Load

Table 15. Terminations for Single-ended Output

Clock Source	Device Under Test (DUT)	Rs (Ω)	Zo (Ω)	L (cm)	C_L (pF)
N/A	9SQL495x	33	50	12.7	4.7

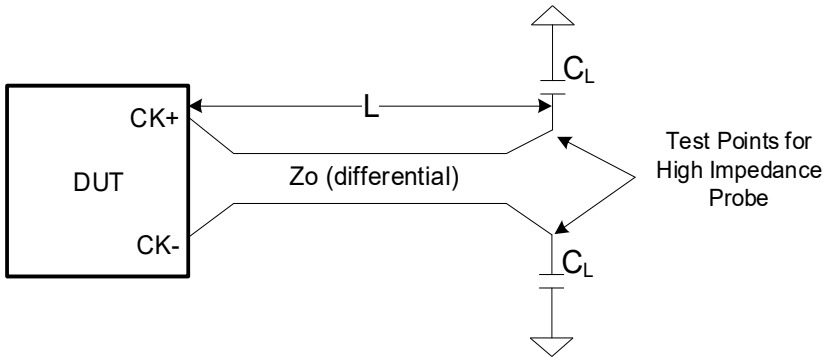


Figure 6. Test Load for AC/DC Measurements

Table 16. Terminations for AC/DC Measurements

Clock Source	Device Under Test (DUT)	Rs (Ω)	Zo (Ω)	L (cm)	C_L (pF)
N/A	9SQL495x	Internal	85	12.7	2

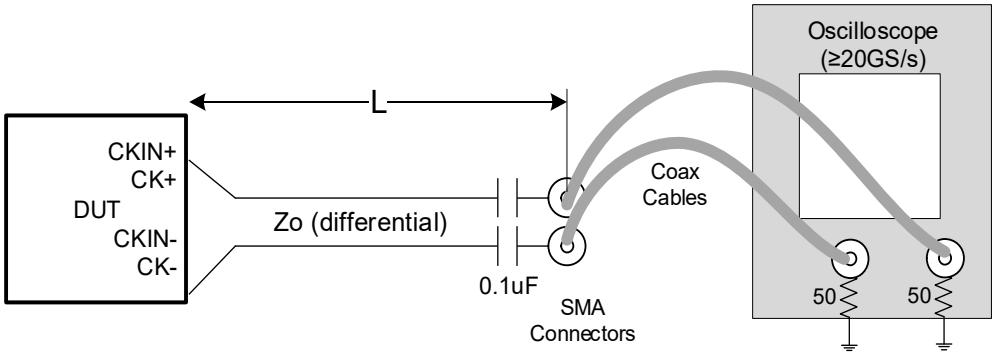


Figure 7. Test Setup for PCIe Clock Phase Jitter Measurements

Table 17. Terminations for PCIe Clock Phase Jitter Measurements

Clock Source	Device Under Test (DUT)	Rs (Ω)	Zo (Ω)	L (cm)	C_L (pF)
N/A	9SQL495x	Internal	85	12.7	N/A

5. Alternate Terminations

The device family can easily drive LVPECL, LVDS, and CML logic. See "AN-891 Driving LVPECL, LVDS, and CML Logic with "Universal" Low-Power HCSL Outputs" for details.

6. Crystal Characteristics

Table 18. Recommended Crystal Characteristics

Parameter	Value	Units
Frequency[1]	25	MHz
Resonance Mode	Fundamental	-
Frequency Tolerance at 25°C	±20	ppm maximum
Frequency Stability, reference at 25°C over operating temperature range	±20	ppm maximum
Temperature Range (industrial)	-40 to +85	°C
Temperature Range (commercial)	0 to +70	°C
Equivalent Series Resistance (ESR)	50	Ω maximum
Shunt Capacitance (C_O)	7	pF maximum
Load Capacitance (C_L)	8	pF maximum
Drive Level	0.1	mW maximum
Aging per year	±5	ppm maximum

1. When driven by an external oscillator via the XIN/CLKIN_25 pin, X2 should be floating.

7. General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Note: Address is latched on SADR pin.

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
Data Byte Count=X			
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table 19. Byte 0: Output Enable Register

Byte 0 [1]	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable	Output Enable
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	See B11[1:0]							
1	OE# Pin Controls Output							
9SQL4958 Name	OE7	OE6	OE5	OE4	OE3	OE2	OE1	OE0
9SQL4958 Default	1	1	1	1	1	1	1	1
9SQL4954 Name	Reserved	Reserved	Reserved	Reserved	OE3	OE2	OE1	OE0
9SQL4954 Default	x	x	x	x	1	1	1	1
9SQL4952 Name	Reserved	Reserved	Reserved	Reserved	Reserved	OE1	OE0	Reserved
9SQL4952 Default	x	x	x	x	x	1	1	x

1. A low on these bits will override the OE# pin and force the differential output to the state indicated by B11[1:0] (Low/Low default)

Table 20. Byte 1: Spread Spectrum with V_{HIGH} Control Register

Byte 1	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	SS Enable Readback Bit1	SS Enable Readback Bit0	Enable software control of spread spectrum	SS Software Control Bit1	SS Software Control Bit0	Reserved	Controls Output Amplitude	
Type	R	R	RW	RW [1]	RW [1]		RW	RW
0	See Spread Selection table		SS controlled by latch (B1[7:6])	See Spread Selection table			00 = 0.6V	10 = 0.75V
1			Values in B1[4:3] control SS amount				01 = 0.68V	11 = 0.85V
Name	SSENRB1	SSENRB1	SSEN_SWCNTRL	SSENSW1	SSENSW0		AMPLITUDE 1	AMPLITUDE 0
Default	Latch	Latch	0	0	0	x	1	0

1. See notes on Spread Selection table. B1[5] must be set to a 1 in order to use B1[4:3].

Table 21. Byte 2: DIF Slew Selection Register

Byte 2	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function [1]	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate	Select fast or slow slew rate
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	Slow Slew Rate							
1	Fast Setting							
9SQL4958 Name	DIF7_slew	DIF6_slew	DIF5_slew	DIF4_slew	DIF3_slew	DIF2_slew	DIF1_slew	DIF0_slew
9SQL4958 Default	1	1	1	1	1	1	1	1
9SQL4954 Name	Reserved	Reserved	Reserved	Reserved	DIF3_slew	DIF2_slew	DIF1_slew	DIF0_slew
9SQL4954 Default	x	x	x	x	1	1	1	1
9SQL4952 Name	Reserved	Reserved	Reserved	Reserved	Reserved	DIF1_slew	DIF0_slew	Reserved
9SQL4952 Default	x	x	x	x	x	1	1	x

1. See Differential Low-Power HCSL Outputs table for slew rates.

Table 22. Byte 3: REF Slew Rate Control Register

Byte 3	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Slew Rate Control		Wake-on-Lan Enable for REF	REF Output Enable	Reserved	Reserved	Reserved	Reserved
Type	RW	RW	RW	RW				
0	00 = Slowest	10 = Fast	REF disabled in Power Down	Disabled [1]				
1	01 = Slow	11 = Fastest	REF runs in Power Down	Enabled				
Name	REF Slew Rate [1:0]		REF Power Down Function	REF OE				
Default	0	1	0	1	x	x	x	x

1. The disabled state depends on Byte11[1:0]. '00' = Low, '01'= HiZ, '10' = Low, '11' = High.

Byte 4 is Reserved

Table 23. Byte 5: Revision and Vendor ID Register

Byte 5	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Revision ID				VENDOR ID			
Type	R	R	R	R	R	R	R	R
0	D rev = 0011				0001 = Renesas			
1								
Name	RID3	RID2	RID1	RID0	VID3	VID2	VID1	VID0

Table 24. Byte 6: Device Type/Device ID Register

Byte 6	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Device Type		Device ID					
Type	R	R	R	R	R	R	R	R
0	00 = 9SQL		9SQL4958 = 0b00100 9SQL4954 = 0b00100 9SQL4952 = 0b00010					
1								
Name	Device Type1	Device Type0	Device ID5	Device ID4	Device ID3	Device ID2	Device ID1	Device ID0

Table 25. Byte 7: Byte Count Register

Byte 7	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Byte Count Programming				
Type				RW	RW	RW	RW	RW
0				Writing to this register will configure how many bytes will be read back.				
1								
Name				BC4	BC3	BC2	BC1	BC0
Default	x	x	x	0	1	0	0	0

Bytes 8 and 9 are Reserved

Table 26. Byte 10: PLL MN Enable, PD_Restore Register

Byte 10	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	M/N Programming Enable	Restore Default Config. In PD	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Type	RW	RW						
0	M/N Prog. Disabled	Clear Config in PD						
1	M/N Prog. Enabled	Keep Config in PD						
Name	PLL M/N En	Power-Down (PD) Restore						
Default	0	1	x	x	x	x	x	x

Table 27. Byte 11: Stop State Control Register

Byte 11	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	True/Complement DIF Output Disable State	
Type							RW	RW
0							00 = Low/Low	01 = HiZ/HiZ
1							10 = High/Low	11 = Low/High
Name							STP[1]	STP[0]
Default	x	x	x	x	x	x	0	0

Table 28. Byte 12: Impedance Control Register 1

Byte 12	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	00 = Reserved, 01 = 85ohm DIF Zout 10 = 100ohm DIF Zout, 11 = Reserved							
1								
9SQL4958 Name	DIF3_imp[1]	DIF3_imp[0]	DIF2_imp[1]	DIF2_imp[0]	DIF1_imp[1]	DIF1_imp[0]	DIF0_imp[1]	DIF0_imp[0]
9SQL4958 Default	9SQL4958 defaults to 0b01010101							
9SQL4954 Name	DIF1_imp[1]	DIF1_imp[0]	Reserved	Reserved	DIF0_imp[1]	DIF0_imp[0]	Reserved	Reserved
9SQL4954 Default	9SQL4954 defaults to 0b01xx01xx							

Table 28. Byte 12: Impedance Control Register 1 (Cont.)

Byte 12	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9SQL4952 Name	DIF0_imp[1]	DIF0_imp[0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
9SQL4952 Default	9SQL4952 defaults to 0b01xxxxxx							

Table 29. Byte 13: Impedance Control Register 2

Byte 13	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]		Output impedance control [1:0]	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	00 = Reserved, 01 = 85ohm DIF Zout 10 = 100ohm DIF Zout, 11 = Reserved							
1								
9SQL4958 Name	DIF7_imp[1]	DIF7_imp[0]	DIF6_imp[1]	DIF6_imp[0]	DIF5_imp[1]	DIF5_imp[0]	DIF4_imp[1]	DIF4_imp[0]
9SQL4958 Default	9SQL4958 defaults to 0h55							
9SQL4954 Name	Reserved	Reserved	DIF3_imp[1]	DIF3_imp[0]	DIF2_imp[1]	DIF2_imp[0]	Reserved	Reserved
9SQL4954 Default	9SQL4954 defaults to 0bxx0101xx							
9SQL4952 Name	Reserved	Reserved	Reserved	Reserved	DIF1_imp[1]	DIF1_imp[0]	Reserved	Reserved
9SQL4952 Default	9SQL4952 defaults to 0bxxxx01xx							

Table 30. Byte 14: Pull-up Pull-down Control Register 1

Byte 14	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Pull-up (pu)/ Pull-down (pd) control		Pull-up (pd)/ Pull-down (pd) control		Pull-up (pd)/ Pull-down (pd) control		Pull-up (pd)/ Pull-down (pd) control	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd
1	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd
9SQL4958 Name	OE3_pu/pd [1]	OE3_pu/pd [0]	OE2_pu/pd [1]	OE2_pu/pd [0]	OE1_pu/pd [1]	OE1_pu/pd [0]	OE0_pu/pd [1]	OE0_pu/pd [0]
9SQL4958 Default	0	1	0	1	0	1	0	1
9SQL4954 Name	OE1_pu/pd [1]	OE1_pu/pd [0]	Reserved	Reserved	OE0_pu/pd [1]	OE0_pu/pd [0]	Reserved	Reserved
9SQL4954 Default	0	1	x	x	0	1	x	x

Table 30. Byte 14: Pull-up Pull-down Control Register 1 (Cont.)

Byte 14	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
9SQL4952 Name	OE0_pu/pd [1]	OE0_pu/pd [0]	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
9SQL4952 Default	0	1	x	x	x	x	x	x

Table 31. Byte 15: Pull-up Pull-down Control Register 2

Byte 15	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Pull-up (pd)/ Pull-down (pd) control		Pull-up (pd)/ Pull-down (pd) control		Pull-up (pd)/ Pull-down (pd) control		Pull-up (pd)/ Pull-down (pd) control	
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd	00 = None	01 = pd
1	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd	10 = pu	11 = pu+pd
9SQL4958 Name	OE7_pu/pd [1]	OE7_pu/pd0]	OE6_pu/pd [1]	OE6_pu/pd [0]	OE5_pu/pd [1]	OE5_pu/pd [0]	OE4_pu/pd [1]	OE4_pu/pd [0]
9SQL4958 Default	0	1	0	1	0	1	0	1
9SQL4954 Name	Reserved	Reserved	OE3_pu/pd [1]	OE3_pu/pd [0]	OE2_pu/pd [1]	OE2_pu/pd [0]	Reserved	Reserved
9SQL4954 Default	0	1	0	1	0	1	0	1
9SQL4952 Name	Reserved	Reserved	Reserved	Reserved	OE1_pu/pd [1]	OE1_pu/pd [0]	Reserved	Reserved
9SQL4952 Default	0	1	0	1	0	1	0	1

Table 32. Byte 16: Pull-up Pull-down Control Register 3

Byte 16	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Pull-up (pd)/ Pull-down (pd) control	
Type							RW	RW
0							00 = None	01 = pd
1							10 = pu	11 = pu+pd
Name							CKPWRGD_ PD_pu/pd[1]	CKPWRGD_ PD_pu/pd[0]
Default	0	0	1	0	0	1	1	0

Byte 17 is Reserved

Table 33. Byte 18: Polarity Control Register 2

Byte 18	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity	Sets OE pin polarity
Type	RW	RW	RW	RW	RW	RW	RW	RW
0	Output enabled when OE pin is low							
1	Output enabled when OE pin is high							
9SQL4958 Name	OE7_polarity	OE6_polarity	OE5_polarity	OE4_polarity	OE3_polarity	OE2_polarity	OE1_polarity	OE0_polarity
9SQL4958 Default	0	0	0	0	0	0	0	0
9SQL4954 Name	Reserved	OE3_polarity	OE2_polarity	Reserved	OE1_polarity	Reserved	OE0_polarity	Reserved
9SQL4954 Default	0	0	0	0	0	0	0	0
9SQL4952 Name	Reserved	Reserved	OE1_polarity	Reserved	OE0_polarity	Reserved	Reserved	Reserved
9SQL4952 Default	0	0	0	0	0	0	0	0

Table 34. Byte 19: Polarity Control Register 1

Byte 19	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Control Function	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Sets CKPWRGD_PD polarity
Type								RW
0								Power Down when Low
1								Power Down when High
Name								CKPWRGD_PD_polarity
Default	0	0	0	0	0	0	0	0

8. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

9. Marking Diagrams

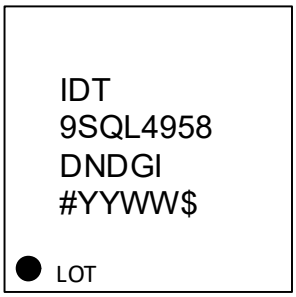
9.1 9SQL4952D

- Line 1: truncated part number.
- Line 2:
  - “YYWW” is the last two digits of the year and the work week the part was assembled.
  - “$” denotes the mark code.
- “LOT” denotes the lot number.

9.2 9SQL4954D

- Lines 2 and 3: part number.
- Line 4:
  -
  - “YYWW” is the last two digits of the year and the work week the part was assembled.
  - “$” denotes the mark code.
- “LOT” denotes the lot number.

9.3 9SQL4958D



- Lines 2 and 3: part number.
- Line 4:
  - “#” denotes the stepping sequence number
  - “YYWW” is the last two digits of the year and the work week the part was assembled.
  - “$” denotes the mark code.
- “LOT” denotes the lot number.

10. Ordering Information

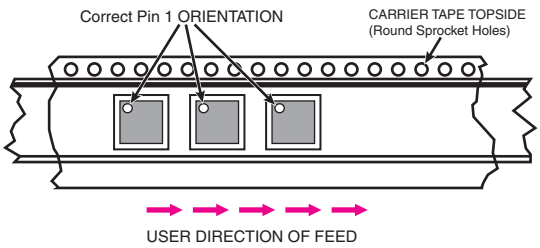
Table 35. Ordering Information

Part Number	Clock Output Count	Output Impedance	Package Description	Carrier Type	Temp. Range
9SQL4952DNLGI	2	85	4.0 × 4.0 × 0.90 mm 24-pin VFQFPN	None - Trays 8 = Tape and Reel, Pin 1 Orientation: EIA-481C (see Table 36 for more details)	-40°C to +85°C
9SQL4952DNLGI8					
9SQL4954DNLGI	4	85	5.0 × 5.0 × 0.90 mm 32-pin VFQFPN		
9SQL4954DNLGI8					
9SQL4958DNDGI	8	85	6.0 × 6.0 × 0.90 mm 48-pin VFQFPN		
9SQL4958DNDGI8					

“D” is the device revision designator (will not correlate with the datasheet revision).

“G” denotes Pb-free configuration, RoHS compliant.

Table 36. Pin 1 Orientation in Tape and Reel Packaging

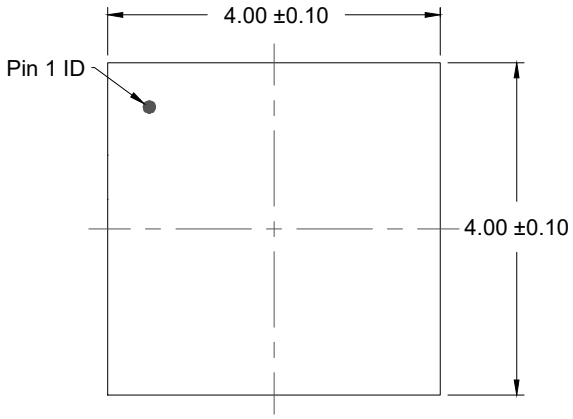
Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	

11. Revision History

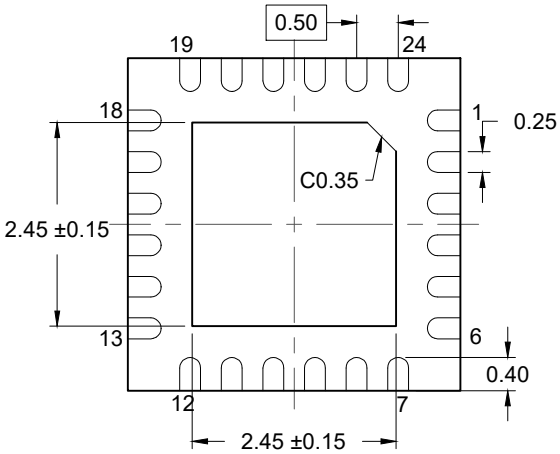
Revision	Date	Description
1.01	Aug 5, 2024	▪ Updated Package Outline Drawings text. ▪ Updated POD links in Ordering Information.
1.00	Jul 1, 2022	Initial release of the rev D devices datasheet.

Package Outline Drawing

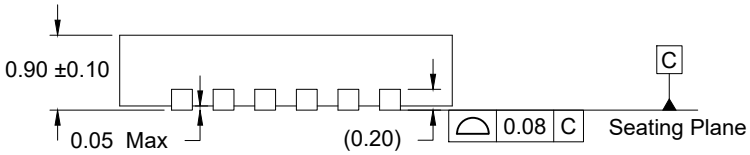
Package Code:NLG24P1
24-VFQFPN 4.0 x 4.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4192-01, Revision: 05, Date Created: Aug 1, 2022



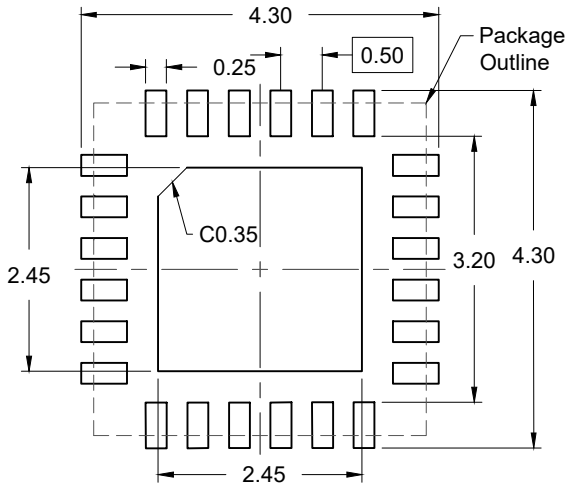
TOP VIEW



BOTTOM VIEW



SIDE VIEW



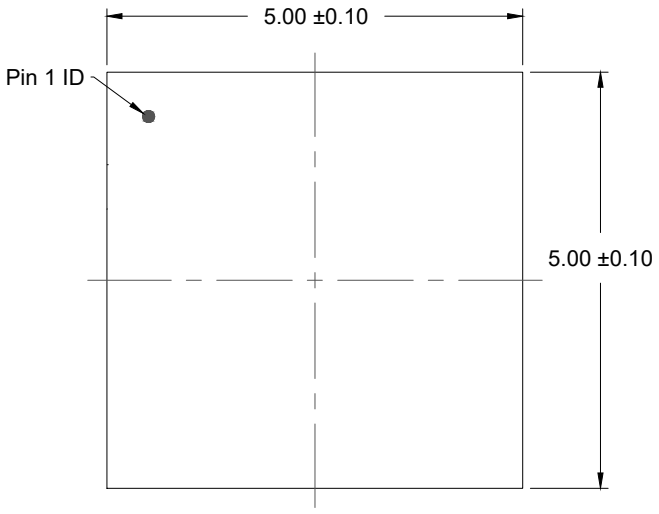
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

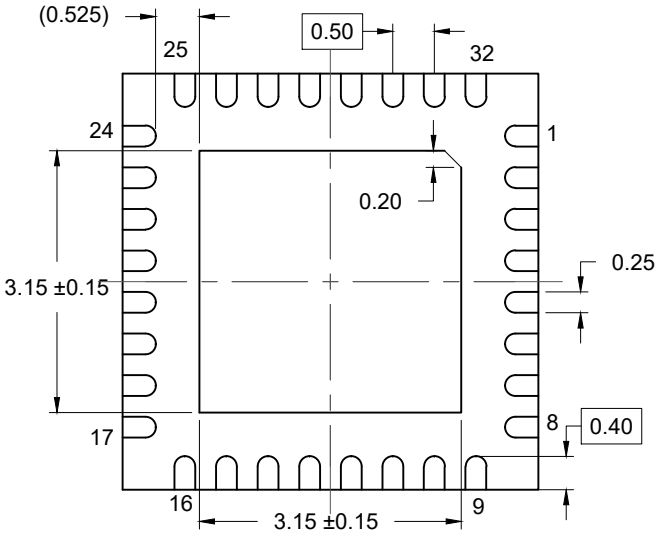
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

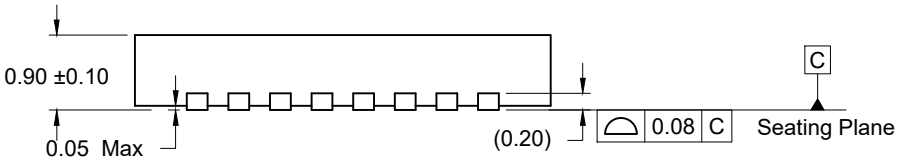
Package Code:NLG32P1
32-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.5mm Pitch
PSC-4171-01, Revision: 04, Date Created: Aug 15, 2022



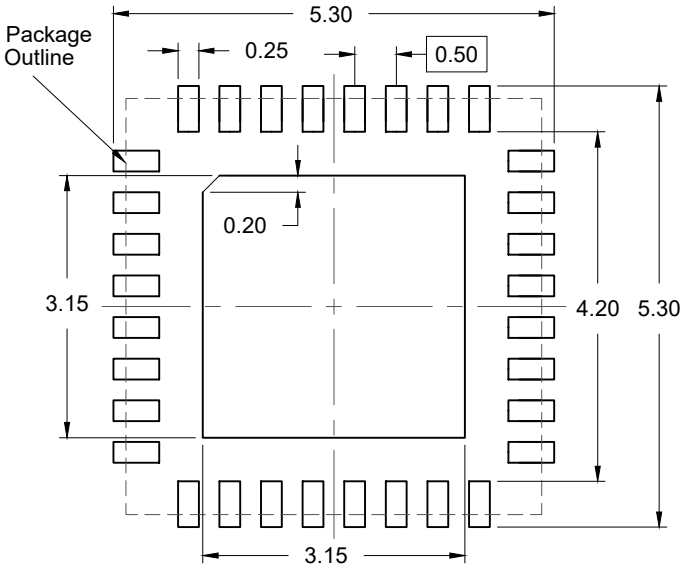
TOP VIEW



BOTTOM VIEW



SIDE VIEW



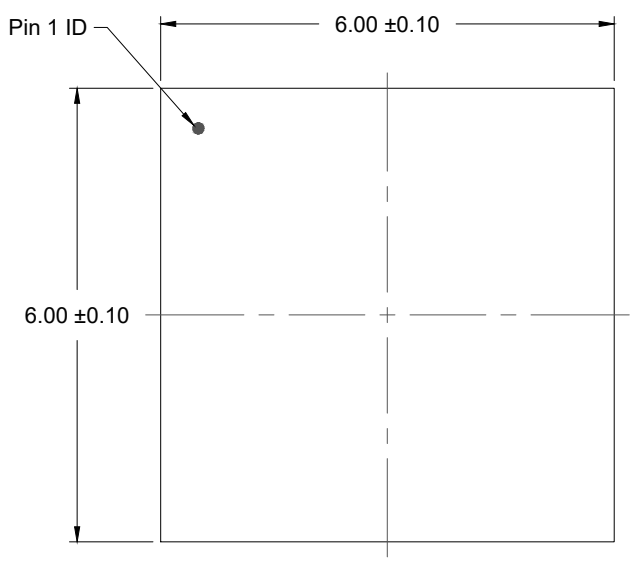
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

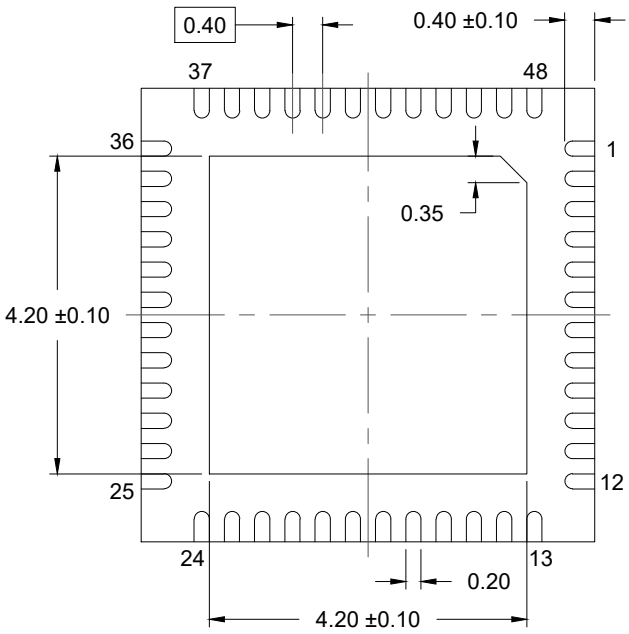
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

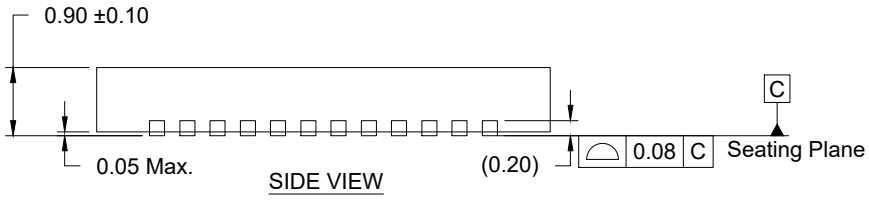
Package Code:NDG48P2
48-VFQFPN 6.0 x 6.0 x 0.9 mm Body, 0.4mm Pitch
PSC-4212-02, Revision: 04, Date Created: Sep 28, 2022



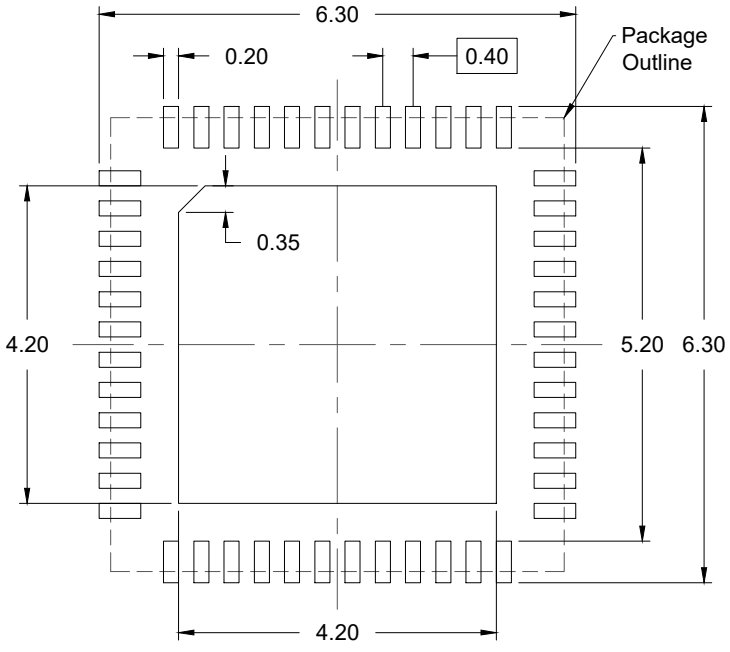
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.