Description

The XP devices are ultra-low phase noise quartz-based PLL oscillators supporting a large range of frequencies and output interface types. These devices are designed to operate at three different power supplies and are available in three package sizes with several pinout configurations, as well as three operational temperature ranges.

The XP devices can be programmed to generate an output frequency from 15MHz to 2100MHz with a resolution as low as 1Hz accuracy. The configuration capability of this family of devices allows for fast delivery times for both sample and large production orders.

Parts are for one time programming (OTP) at the factory for a fixed frequency application, or can be field programmable using I2C, based on system needs (see note 1 under Pin Descriptions).

Features

- Output types: LVDS, LVPECL, CML
  - Frequency range: 15MHz to 2100MHz
- Output type: HCSL
  - Frequency range: 15MHz to 725MHz
- Supply voltage options: 1.8V, 2.5V, or 3.3V
- Phase jitter (12kHz to 20MHz): 120fs typical
- Package options:
  - 7.0 × 5.0 × 1.7 mm
  - 5.0 × 3.2 × 1.17 mm
  - 3.2 × 2.5 × 1.07 mm
- Operating temperatures and frequency stability:
  - -40°C to +85°C, ±25ppm
  - -40°C to +105°C, ±50ppm

Pin Assignments

Figure 1. 7.0 × 5.0 mm, 5.0 × 3.2 mm, and 3.2 × 2.5 mm Packages

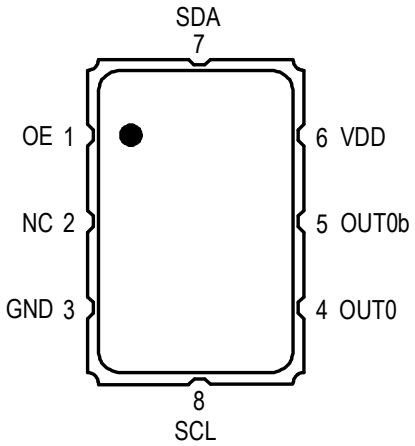


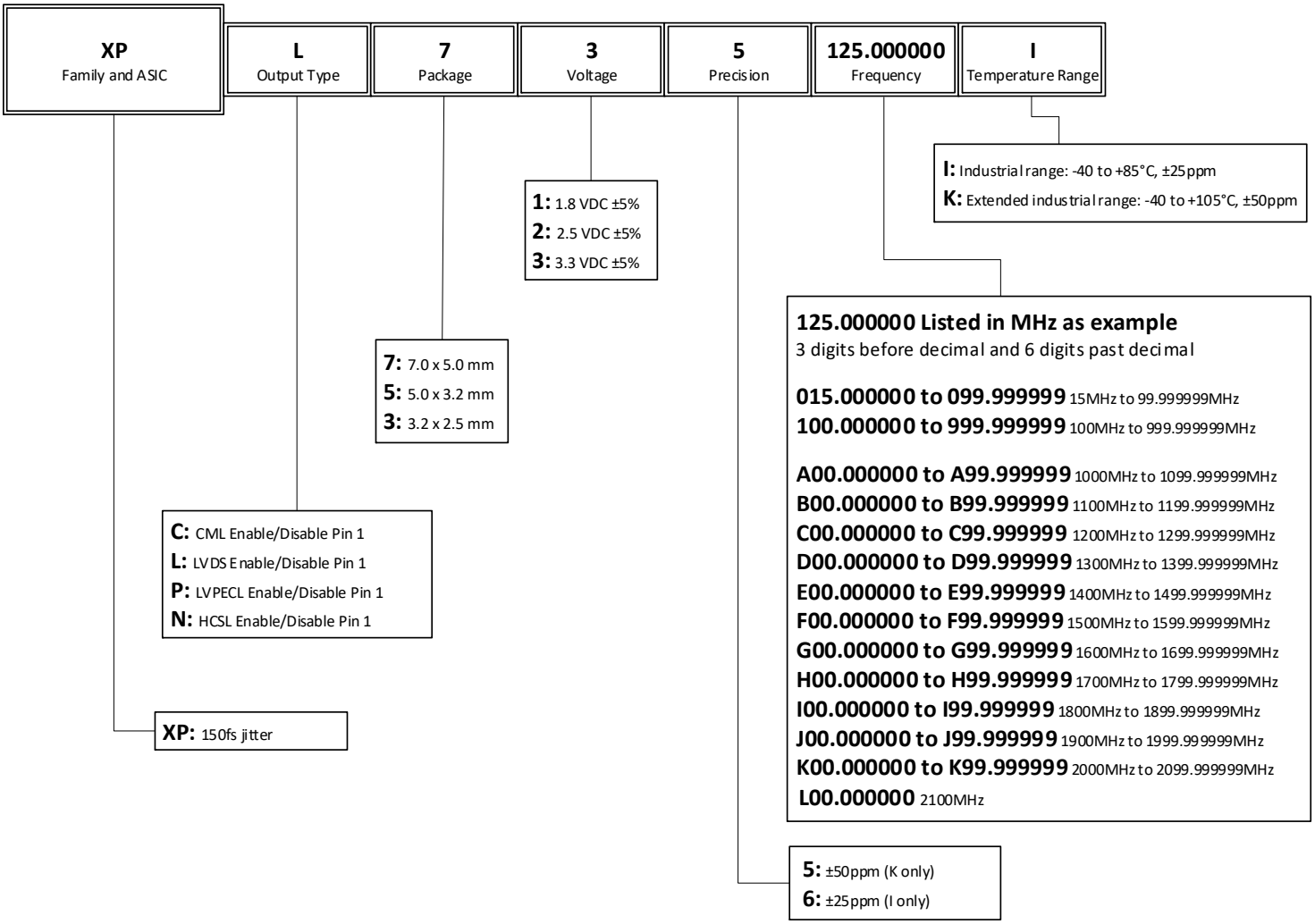
Table 1. Pin Descriptions

Pin #	Pin Name	Description
1	OE	Output Enable (0 = output disabled, pulled high internally)
2	NC	No connect
3	GND	Connect to ground
4	OUT0	Output
5	OUT0b	Complementary output
6	V_{DD}	Supply voltage
7	SDA [1]	Serial data
8	SCL [1]	Serial clock

[1] Pins 7 and 8 are no connect for non-I2C applications.

See Revision History for more details.

Ordering Information



Contents

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the device. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range. Thermal characteristics, in actual applications, should be assessed case by case to guarantee junction temperature does not exceed 125°C.

Table 2. Absolute Maximum Ratings

Item	Rating					
V_{DD}	-0.5V to +3.8V					
OE	-0.5V to +3.8V					
Storage Temperature	-55°C to 125°C					
Maximum Junction Temperature	125°C					
Theta J_A [1]	JD8	75.9 °C/W	JX8	89.6 °C/W	JSW8	97.4 °C/W
Theta J_B [1]		48.6 °C/W		54.3 °C/W		66.8 °C/W

[1] Thermal characteristics are based on simulation in standard condition.

ESD Compliance

Table 3. ESD Compliance

Human Body Model (HBM)	2000V

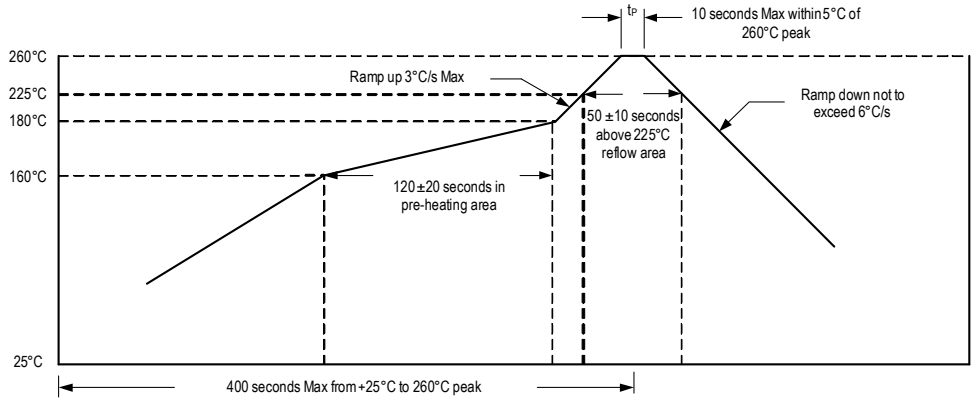
Mechanical Testing

Table 4. Mechanical Testing *

Parameter	Test Method
Mechanical Shock	Half-sine wave with 0.3ms 3000G. X, Y, Z each direction 1 time.
Mechanical Vibration	Frequency: 10 to 55MHz amplitude: 1.5mm. Frequency: 55–2000Hz peak value: 20G. Duration time: 4H for each X,Y,Z axis; total 12hours.
High Temp Operating Life (HTOL)	1000 hours at 125°C (under power).
Hermetic Seal	Gross leak (air leak test). Fine leak (Helium leak test) He-pressure: 6kgf/cm² 2 hours.

* MSL level does not apply.

Solder Reflow Profile



DC Electrical Characteristics

Note for all DC Electrical Characteristics tables: A pull-up resistor from V_{DD} to OE enables output when pin 1 is left open.

Table 5. 3.3V IDD DC Electrical Characteristics

V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C, -40°C to +105°C, typical at 156.25MHz.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Current Consumption	LVDS	15MHz to 400MHz.	—	59	67	mA
			400MHz to 2.1GHz.	—	—	85	
		LVPECL	15MHz to 212.5MHz.	—	84	94	
			212MHz to 400MHz.	—	—	110	
			400MHz to 2.1GHz.	—	—	110	
		HCSL	15MHz to 725MHz.	—	74	83	
		CML	15MHz to 2.1GHz.	—	45	61	

Table 6. 2.5V IDD DC Electrical Characteristics

V_{DD} = 2.5V ±5%, T_A = -40°C to +85°C, -40°C to +105°C, typical at 156.25MHz.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Current Consumption	LVDS	15MHz to 400MHz.	—	59	66	mA
			400MHz to 2.1GHz.	—	—	85	
		LVPECL	15MHz to 156.25MHz.	—	84	94	
			156.25MHz to 400MHz.	—	—	110	
			400MHz to 2.1GHz.	—	—	110	
		HCSL	15MHz to 400MHz.	—	—	95	
			400MHz to 725MHz.	—	74	82	
		CML	15MHz to 2.1GHz.	—	54	61	

Table 7. 1.8V IDD DC Electrical Characteristics

V_{DD} = 1.8V ±5%, T_A = -40°C to +85°C, -40°C to +105°C, typical at 156.25MHz.

Symbol	Parameter	Output Type	Conditions	Minimum	Typical	Maximum	Units
I_{DD}	Current Consumption	LVDS	15MHz to 400MHz.	—	59	66	mA
			400MHz to 2.1GHz.	—	—	85	
		LVPECL	15MHz to 250MHz.	—	84	93	
			250MHz to 2.1GHz.	—	—	110	
		HCSL	15MHz to 400MHz.	—	—	95	
			400MHz to 725MHz.	—	74	81	
		CML	15MHz to 2.1GHz.	—	54	61	

Table 8. LVCMOS DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V, 1.8V ±5%, T_A = -40°C to +85°C, -40°C to +105°C, typical at 156.25MHz.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage (OE pin only)	V_{DD} = 3.3V, 2.5V, 1.8V ±5%	0.7 × V_{DD}	—	V_{DD} + 0.3	V
V_{IL}	Input Low Voltage (OE pin only)	V_{DD} = 3.3V, 2.5V, 1.8V ±5%	GND - 0.3	—	0.3 × V_{DD}	V

Table 9. LVDS DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V, 1.8V ±5%, T_A = -40°C to +85°C, -40°C to +105°C, typical at 156.25MHz.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage	V_{DD} = 3.3V, 2.5V, 1.8V ±5%	0.30	0.44	0.60	V
V_{OS}	Output Offset Voltage	V_{DD} = 3.3V ±5%	1.11	1.26	1.41	V
		V_{DD} = 2.5V ±5%	1.08	1.25	1.41	
		V_{DD} = 1.8V ±5%	0.75	0.88	1.01	

Table 10. LVPECL DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V, 1.8V ±5%, T_A = -40°C to +85°C, -40°C to +105°C, typical at 156.25MHz.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	V_{DD} = 3.3V ±5%.	2.28	2.49	2.72	V
		V_{DD} = 2.5V ±5%.	1.52	1.69	1.87	
		V_{DD} = 1.8V ±5%.	0.83	0.96	1.11	
V_{OL}	Output Low Voltage	V_{DD} = 3.3V ±5%.	1.68	1.84	2.01	
		V_{DD} = 2.5V ±5%.	0.92	1.04	1.17	
		V_{DD} = 1.8V ±5%.	0.19	0.30	0.42	

Table 11. HCSL DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V, 1.8V ±5%, T_A = -40°C to +85°C, -40°C to +105°C, typical at 156.25MHz.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	V_{DD} = 3.3V ±5%.	0.78	0.92	1.07	V
		V_{DD} = 2.5V ±5%.	0.74	0.88	1.03	
		V_{DD} = 1.8V ±5%.	0.67	0.81	0.95	
V_{OL}	Output Low Voltage	—	-0.06	0.07	0.20	

Table 12. CML DC Electrical Characteristics

V_{DD} = 3.3V, 2.5V, 1.8V ±5%, T_A = -40°C to +85°C, -40°C to +105°C, typical at 156.25MHz.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage	V_{DD} = 3.3V ±5%.	3.09	3.26	3.43	V
		V_{DD} = 2.5V ±5%.	2.33	2.46	2.59	
		V_{DD} = 1.8V ±5%.	1.66	1.76	1.85	
V_{OL}	Output Low Voltage	V_{DD} = 3.3V ±5%.	2.70	2.85	3.00	V
		V_{DD} = 2.5V ±5%.	1.95	2.06	2.17	
		V_{DD} = 1.8V ±5%.	1.30	1.37	1.45	

Table 13. DC Electrical Characteristics – Leakage Current

V_{DD} = 3.3V, 2.5V, 1.8V ±5%, T_A = -40°C to +85°C, -40°C to +105°C, typical at 156.25MHz.

Symbol	Parameter	Input	Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input Leakage High	OE	V_{DD} = 3.3V ±5%.	-5	0.81	5	µA
		SCLK		-5	1.36	5	
		SDATA		-5	1.44	5	
I_{IL}	Input Leakage Low	OE	V_{DD} = 3.3V ±5%.	-20	-17.44	-14	µA
		SCLK		-37	-33.49	-30	
		SDATA		-20	-17.02	-14	

AC Electrical Characteristics

Notes for all AC Electrical Characteristics tables:

1. A pull-up resistor from V_{DD} to OE enables output when pin 1 is left open.

2. Installation should include a 0.01µF bypass capacitor placed between V_{DD} and GND to minimize power supply line noise.

Table 14. 3.3V AC Electrical Characteristics

V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS, LVPECL, CML.		15	—	2100	MHz
		HCSL.		15	—	725	
	Frequency Stability	Temperature = -40°C to +85°C.		—	—	±25	ppm
		Temperature = -40°C to +105°C.		—	—	±50	ppm
	Frequency Tolerance (25°C)	Temperature = 25°C.		-15	±10	-15	ppm
	Aging (1st year)	T_A = 25°C.		—	—	±3	ppm
	Aging (10 years)	T_A = 25°C.		—	—	±10	ppm
	Output Load	LVDS.	Differential.	—	100	—	Ω
		LVPECL.	V_{DD} - 2.0V.	—	50	—	
		HCSL.	To GND.	—	50	—	
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		—	5	—	ms
t_R	Output Rise Time	LVDS.	20% – 80%, 156.25MHz	—	299	400	ps
		LVPECL.		—	287	400	
		HCSL.		—	306	400	
		CML		—	301	400	
t_F	Output Fall Time	LVDS.	80% – 20%, 156.25MHz	—	279	400	ps
		LVPECL.		—	274	400	
		HCSL.		—	284	400	
		CML		—	279	400	
O_{DC}	Output Clock Duty Cycle	LVDS.	156.25MHz	48	—	52	%
		LVPECL.	156.25MHz	48	—	52	
		HCSL.	156.25MHz	48	—	52	
		CML	156.25MHz	48	—	52	
T_{OE}	Output Enable/Disable Time	—	—	—	1	—	ms

Table 15. 2.5V AC Electrical Characteristics

V_{DD} = 2.5V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS, LVPECL, CML.		15	—	2100	MHz
		HCSL.		15	—	725	
	Frequency Stability	Temperature = -40°C to +85°C.		—	—	±25	ppm
		Temperature = -40°C to +105°C.		—	—	±50	ppm
	Frequency Tolerance (25°C)	Temperature = 25°C.		-15	±10	+15	ppm
	Aging (1st year)	T_A = 25°C.		—	—	±3	
	Aging (10 years)	T_A = 25°C.		—	—	±10	
	Output Load	LVDS.	Differential.	—	100	—	Ω
		LVPECL.	V_{DD} - 2.0V.	—	50	—	
		HCSL.	To GND.	—	50	—	
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		—	5	—	ms
t_R	Output Rise Time	LVDS.	20% – 80%, 156.25MHz	—	303	400	ps
		LVPECL.		—	292	400	
		HCSL.		—	310	400	
		CML		—	304	400	
t_F	Output Fall Time	LVDS.	80% – 20%, 156.25MHz	—	282	400	ps
		LVPECL.		—	278	400	
		HCSL.		—	288	400	
		CML		—	281	400	
O_{DC}	Output Clock Duty Cycle	LVDS.	156.25MHz	48	—	52	%
		LVPECL.	156.25MHz	48	—	52	
		HCSL.	156.25MHz	48	—	52	
		CML	156.25MHz	48	—	52	
T_{OE}	Output Enable/Disable Time	—	—	—	1	—	ms

Table 16. 1.8V AC Electrical Characteristics

V_{DD} = 1.8V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Units
F	Output Frequency Range	LVDS, LVPECL, CML.		15	—	2100	MHz
		HCSL.		15	—	725	
	Frequency Stability	Temperature = -40°C to +85°C.		—	—	±25	ppm
		Temperature = -40°C to +105°C.		—	—	±50	ppm
	Frequency Tolerance (25°C)	Temperature = 25°C.		-15	±10	+15	ppm
	Aging (1st year)	T_A = 25°C.		—	—	±3	
	Aging (10 years)	T_A = 25°C.		—	—	±10	
	Output Load	LVDS.	Differential.	—	100	—	Ω
		LVPECL, HCSL.	To GND.	—	50	—	
T_{ST}	Start-up Time	Output valid time after V_{DD} meets minimum specified level.		—	5	—	ms
t_R	Output Rise Time	LVDS.	20% – 80%, 156.25MHz	—	311	450	ps
		LVPECL.		—	312	450	
		HCSL.		—	316	450	
		CML		—	313	450	
t_F	Output Fall Time	LVDS.	80% – 20%, 156.25MHz	—	290	450	ps
		LVPECL.		—	297	450	
		HCSL.		—	294	450	
		CML		—	289	450	
O_{DC}	Output Clock Duty Cycle	LVDS.	156.25MHz	48	—	52	%
		LVPECL.	156.25MHz	48	—	52	
		HCSL.	156.25MHz	48	—	52	
		CML	156.25MHz	48	—	52	
T_{OE}	Output Enable/Disable Time	—	—	—	1	—	ms

Table 17. Phase Jitter Characteristics

V_{DD} = 3.3V, 2.5V, 1.8V ±5%, T_A = -40°C to +85°C, -40°C to +105°C.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
f_{JITTER}	Phase Jitter (12kHz – 20MHz)	250.00MHz	—	115	—	fsec
		312.50MHz	—	125	—	fsec
		625.00MHz	—	123	—	fsec
		644.53MHz	—	120	—	fsec

Output Waveforms

Figure 2. LVDS Output Waveforms

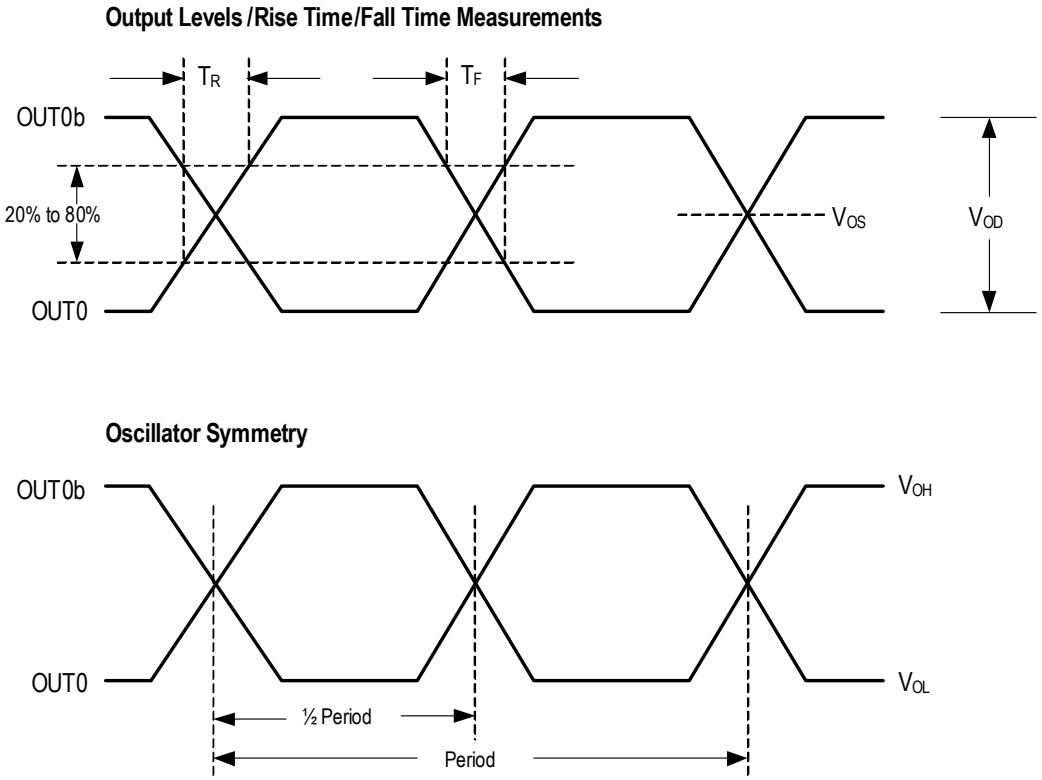


Figure 3. LVPECL Output Waveforms

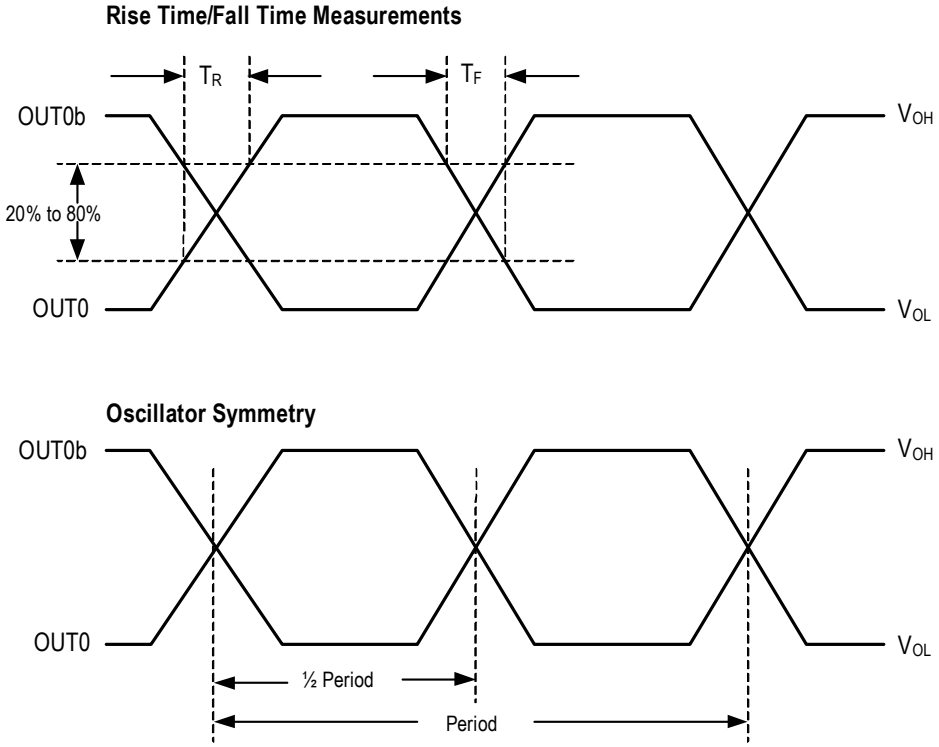


Figure 4. HCSL Output Waveforms

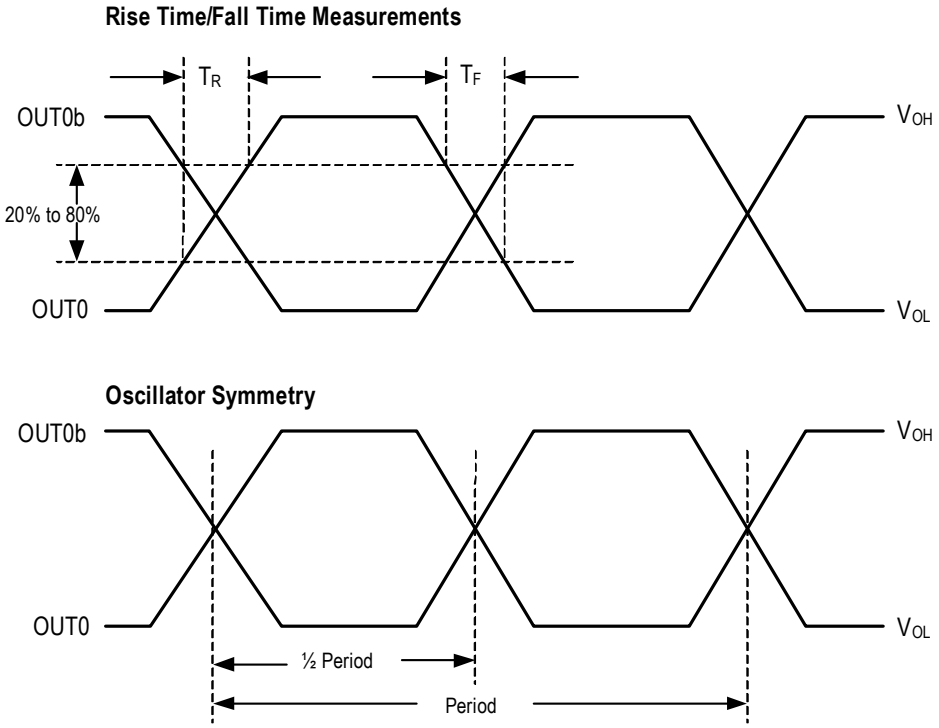
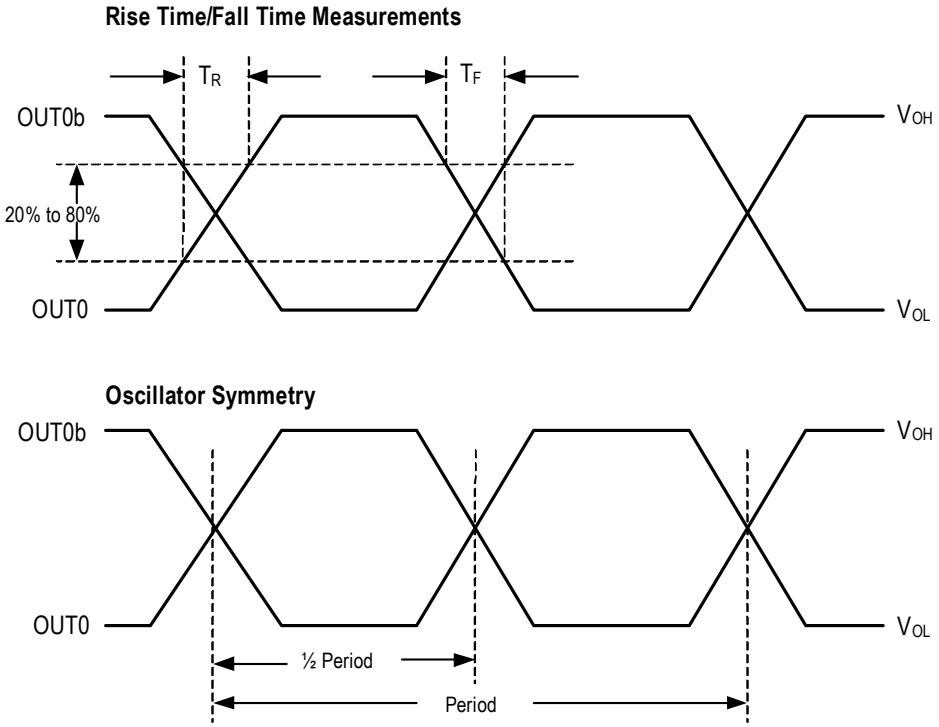


Figure 5. CML Output Waveforms



Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential output is a low impedance follower output that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figure 6 and Figure 7 show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

Figure 6. 3.3V LVPECL Output Termination

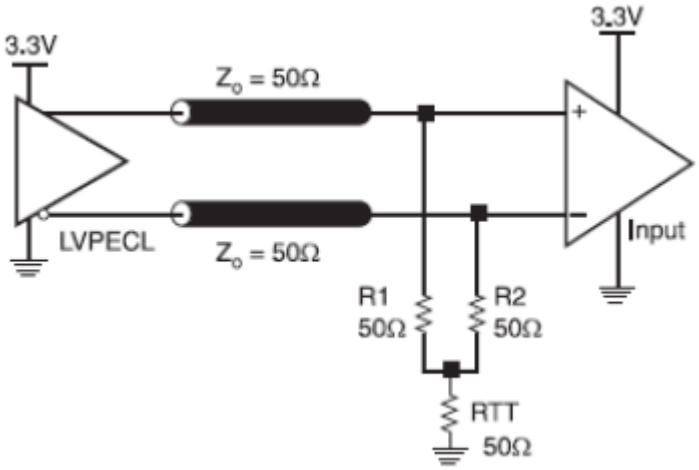
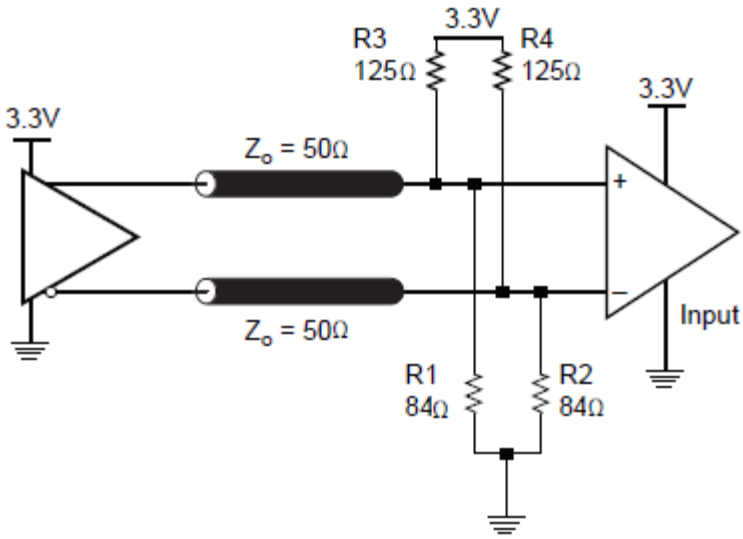


Figure 7. 3.3V LVPECL Output Termination



Termination for 2.5V LVPECL Outputs

Figure 8 and Figure 9 show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 9 can be eliminated and the termination is shown in Figure 10.

Figure 8. 2.5V LVPECL Driver Termination Example

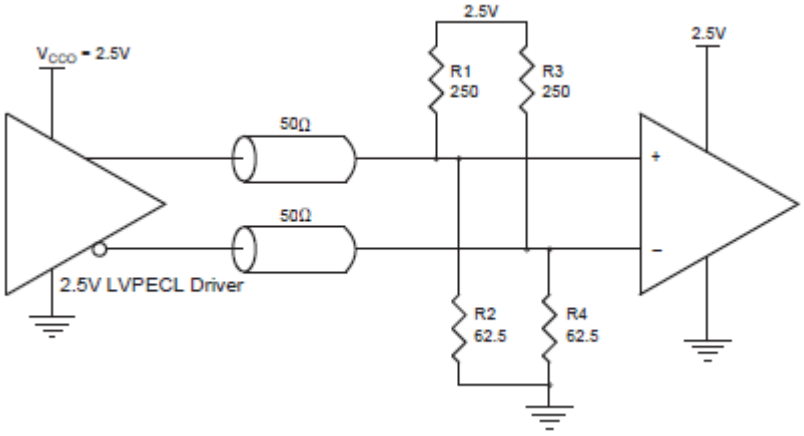


Figure 9. 2.5V LVPECL Driver Termination Example

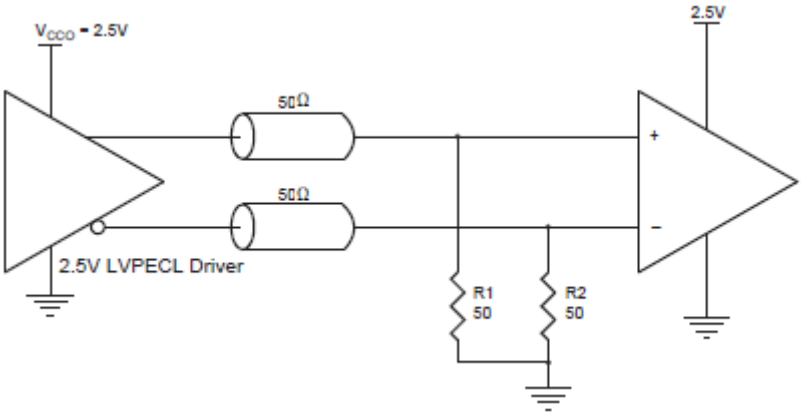
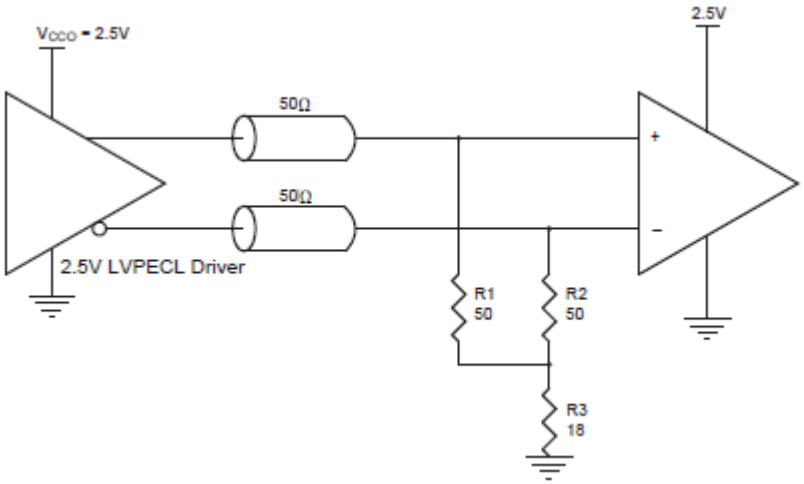


Figure 10. 2.5V LVPECL Driver Termination Example



LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. Renesas offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source.

The standard termination schematic as shown in Figure 11 can be used with either type of output structure. Figure 12, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact Renesas and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

Figure 11. Standard LVDS Termination

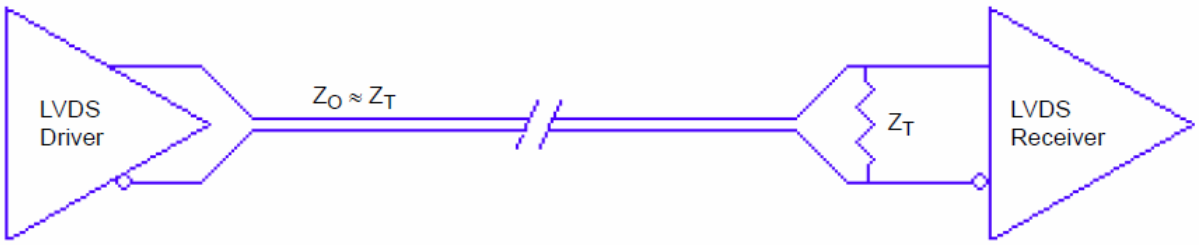
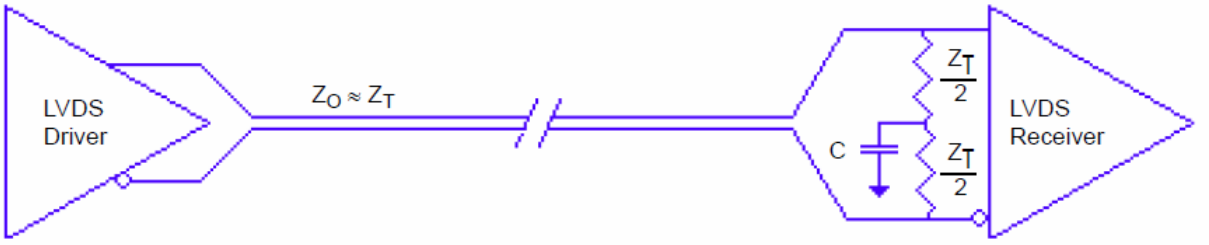


Figure 12. Optional LVDS Termination



Recommended Termination for HCSL Outputs

Figure 13 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential. Figure 14 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 13. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

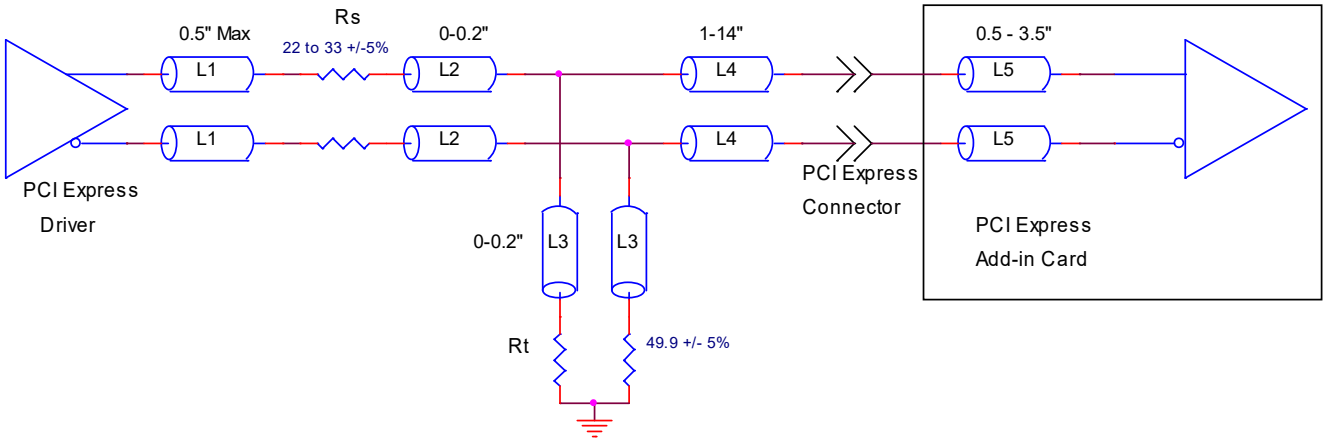
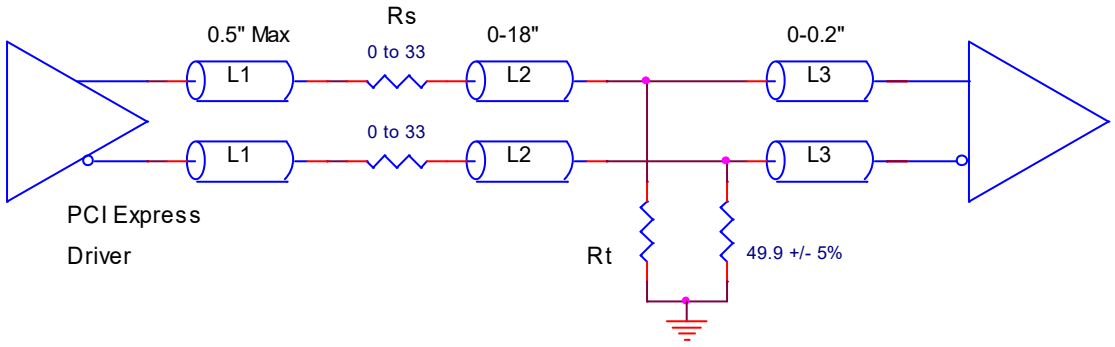


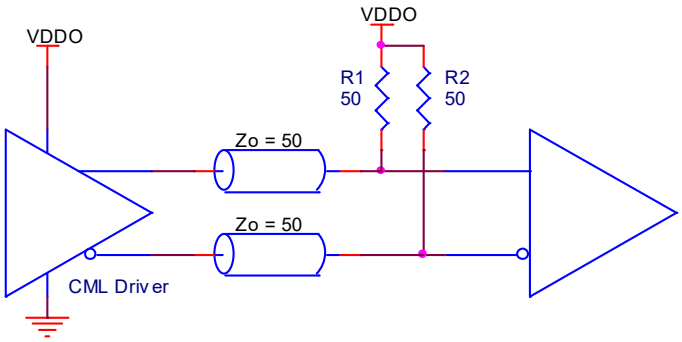
Figure 14. Recommended Termination (where a point-to-point connection can be used)



CML Termination

Figure 15 shows an example of the termination for a CML driver. In this example, the transmission line characteristic impedance is 50Ω. The R1 and R2 50Ω matched load terminations are pulled up to VDDO. The matched loads are located close to the receiver.

Figure 15. CML Termination Example



Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

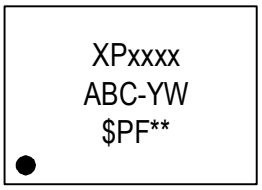
7.0 × 5.0 mm, 8-CLCC (JD8D1) package

5.0 × 3.2 mm, CLCC-8 (JX8D1) package

3.2 × 2.5 mm, 8-COL (JSW8D1) package

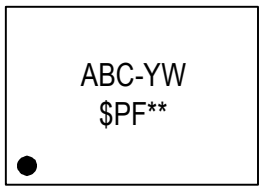
Marking Diagrams

Figure 16. Marking Configuration for the 7.0 × 5.0 mm and 5.0 × 3.2 mm Packages



- Line 1 denotes the truncated part number (e.g., “xxxx” is L726, P516).
- Line 2 indicates the following:
  - “ABC” denotes the truncated first three digits of the frequency code (e.g., 156).
  - “-YW” denotes the last digit of the year and week when the part was assembled.
- Line 3 indicates the following:
  - “$” denotes the mark location.
  - “PF” is where “P” denotes the package coding number and “F” denotes the frequency coding number.
  - “**” denotes the sequential lot number.

Figure 17. Marking Configuration for the 3.2 × 2.5 mm Package



- Line 1 indicates the following:
  - “ABC” denotes the truncated first three digits of the frequency code (e.g., 156).
  - “-YW” denotes the last digit of the year and week when the part was assembled.
- Line 2 indicates the following:
  - “$” denotes the mark location.
  - “PF” is where “P” denotes the package coding number and “F” denotes the frequency coding number.
  - “**” denotes the sequential lot number.

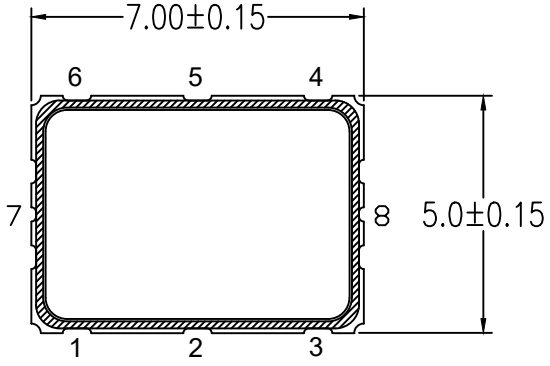
Revision History

Revision Date	Description of Change
February 10, 2022	Updated Output Clock Duty Cycle minimum and maximum specifications for LVDS, LVPECL, HCSL, and CML in Table 14, Table 15, and Table 16.
July 13, 2021	▪ Updated Ordering Information “Precision” option. ▪ Updated Package Outline Drawings section.
September 21, 2020	Updated ordering code to have I2C (was precision field, which is redundant with temperature field).
July 22, 2019	Updated LVDS Differential Output Voltage minimum from 0.28 to 0.30V.
May 22, 2019	Changed 3.3V, 2.5V, and 1.8V LVPECL current consumption conditions value from 670MHz to 2.1GHz.
April 1, 2019	Initial release.

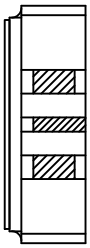
8-CLCC, Package Outline Drawing

7.0 x 5.0 x 1.7 mm Body, 2.54mm Pitch

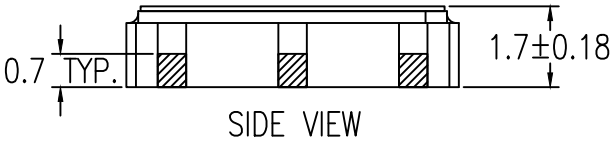
JD8D1, PSC-4733-01, Rev 01, Page 1



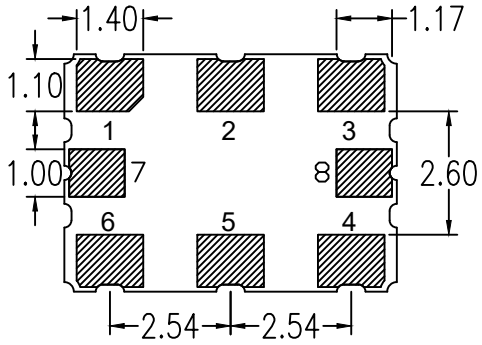
TOP VIEW



SIDE VIEW



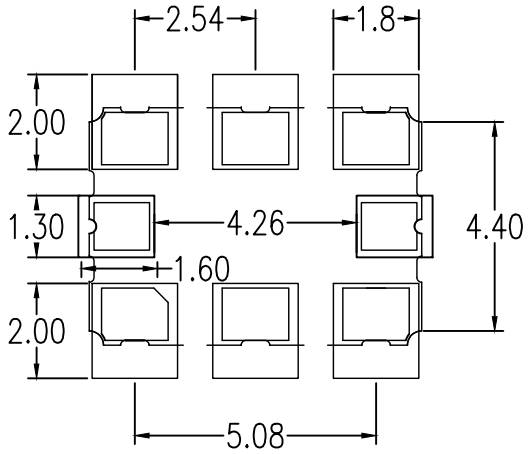
SIDE VIEW



BOTTOM VIEW

NOTES:

1.ALL DIMENSIONS IN MM.



RECOMMENDED LAND PATTERN DIMENSION

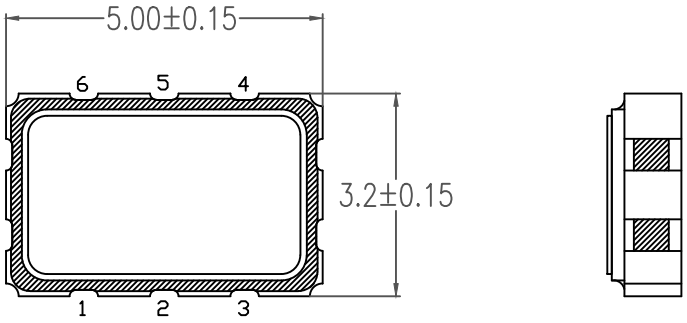
NOTES: ALL DIMENSION ARE IN MM. ANGLES IN DEGREES.

Package Revision History		
Date Created	Rev No.	Description
March 6, 2019	Rev 01	Update Drawing and Dimensions
Aug. 9, 2018	Rev 00	Initial Release

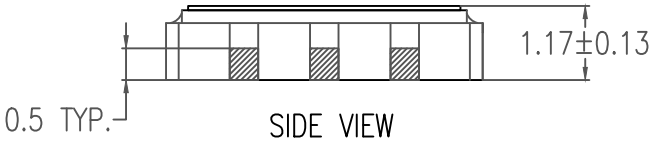
CLCC-8, Package Outline Drawing

5.0 x 3.2 x 1.17 mm Body 1.27mm Pitch

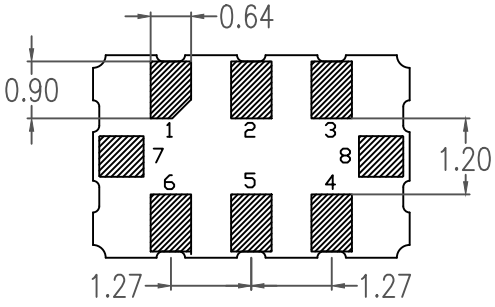
JX8D1, PSC-4754-01, Rev 01, Page 1



TOP VIEW

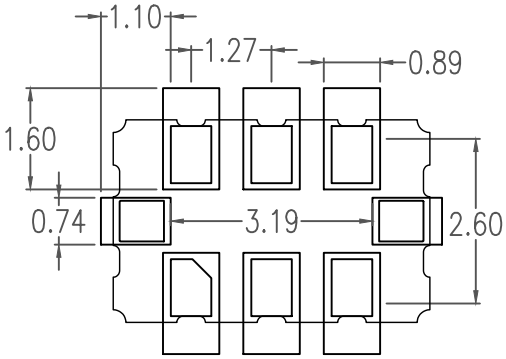


SIDE VIEW



BOTTOM VIEW

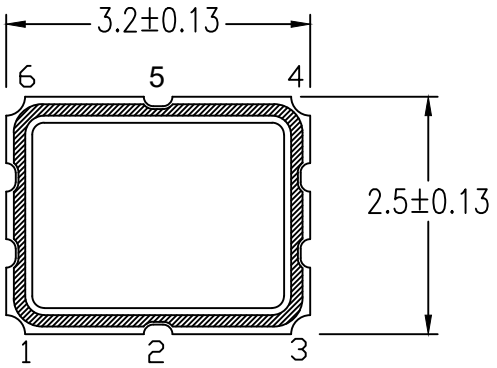
NOTES:
1.ALL DIMENSIONS IN MM.



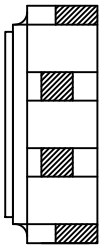
RECOMMENDED LAND PATTERN DIMENSIONS

NOTE:
1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES
2. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

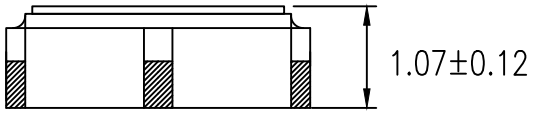
Package Revision History		
Date Created	Rev No.	Description
March 6, 2019	Rev 01	Update Drawing and Dimensions
July 13, 2018	Rev 00	Initial Release



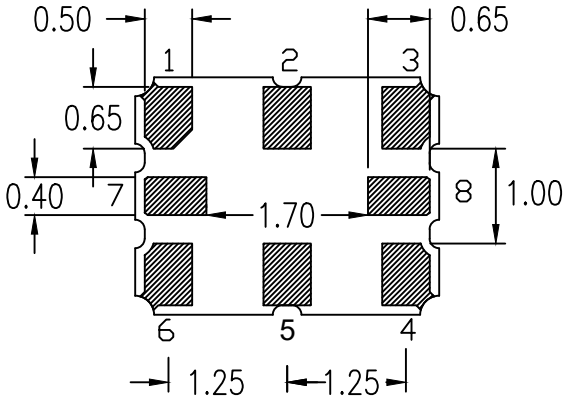
TOP VIEW



SIDE VIEW



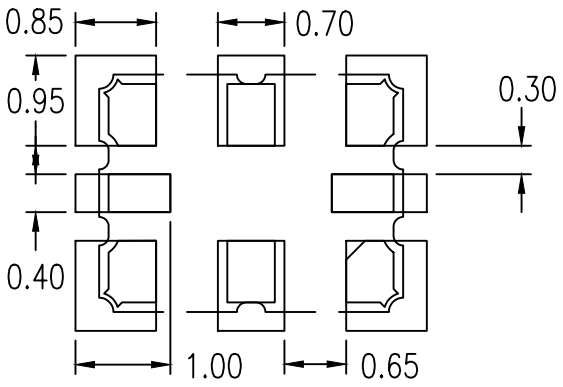
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSION ARE IN MM.



RECOMMENDED LAND PATTERN DIMENSIONS

NOTES: ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
April 10, 2019	Rev 01.	Update Drawing, Thickness and Tolerance
Aug. 8, 2018	Rev 00	Initial Release

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