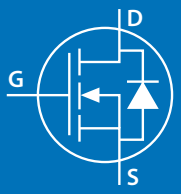
EPC2031 – Enhancement Mode Power Transistor

V_{DS}, 60 V
$R_{DS(on)}$, 2.6 mΩ
I_D, 48 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised June 19, 2020

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Questions: Ask a GaN Expert

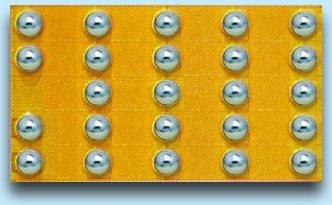
Maximum Ratings			
PARAMETER		**VALUE**	**UNIT**
V_{DS}	Drain-to-Source Voltage (Continuous)	60	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	72	
I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 11°C/W)	48	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	450	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		**TYP**	**UNIT**
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.45	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	3.9	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	45	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 1 mA	60			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 48 V		0.1	0.8	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		1	9	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.1	0.8	mA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 15 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 30 A		2	2.6	mΩ
V_{SD}	Source-Drain Forward Voltage#	V_{GS} = 0 V, I_S = 0.5 A		1.8		V

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.



Die size: 4.6 x 2.6 mm

EPC2031 eGaN® FETs are supplied only in passivated die form with solder bumps.

Applications

- High frequency DC-DC conversion
- Motor drive
- Industrial automation
- Synchronous rectification
- Class-D audio

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2031

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{GS} = 0 V, V_{DS} = 30 V		1640	2000	pF
C_{RSS}	Reverse Transfer Capacitance			35		
C_{OSS}	Output Capacitance			980	1500	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{GS} = 0 V, V_{DS} = 0 to 30 V		1340		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			1580		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{GS} = 5 V, V_{DS} = 30 V, I_D = 30 A		16	21	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 30 V, I_D = 30 A		5		
Q_{GD}	Gate-to-Drain Charge			3.2		
$Q_{G(TH)}$	Gate Charge at Threshold			3.6		
Q_{OSS}	Output Charge	V_{GS} = 0 V, V_{DS} = 30 V		48	72	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

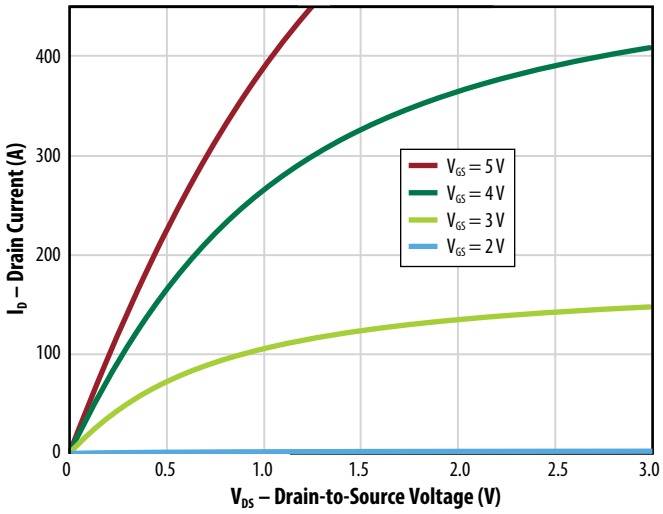


Figure 2: Typical Transfer Characteristics

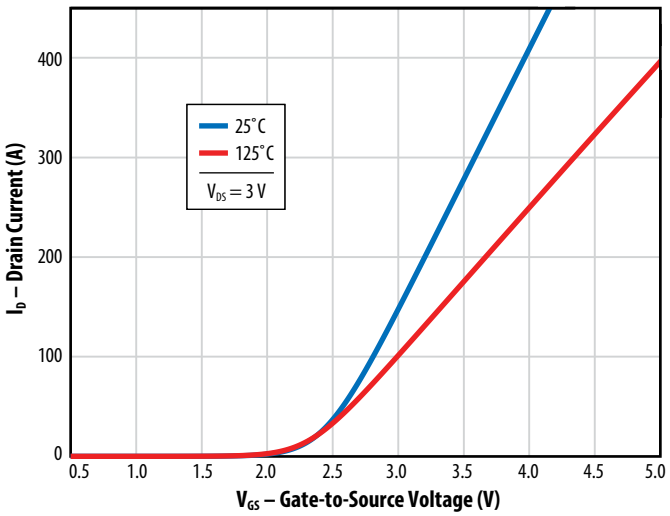


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

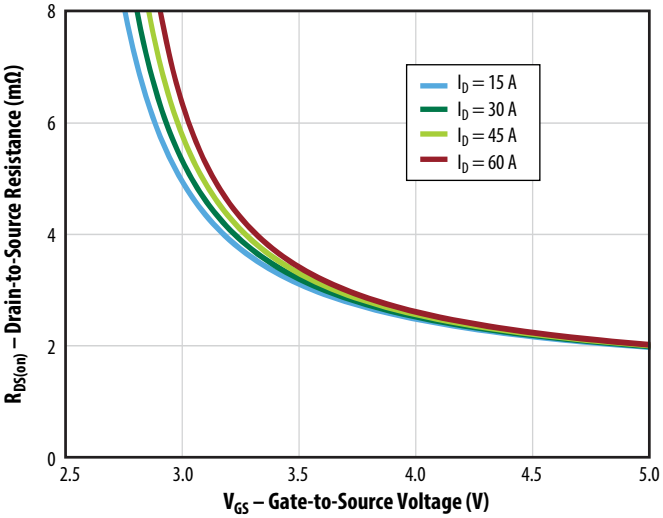


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

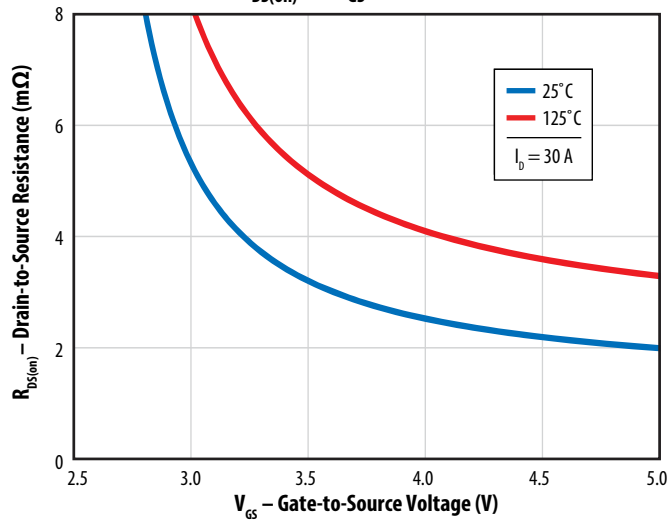


Figure 5a: Typical Capacitance (Linear Scale)

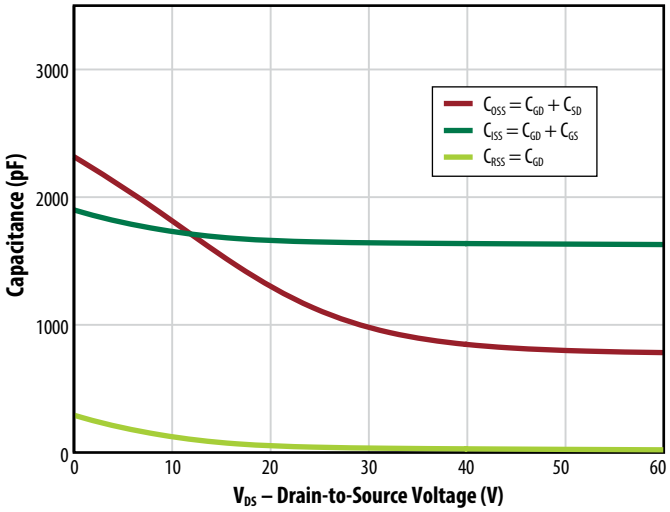


Figure 5b: Typical Capacitance (Log Scale)

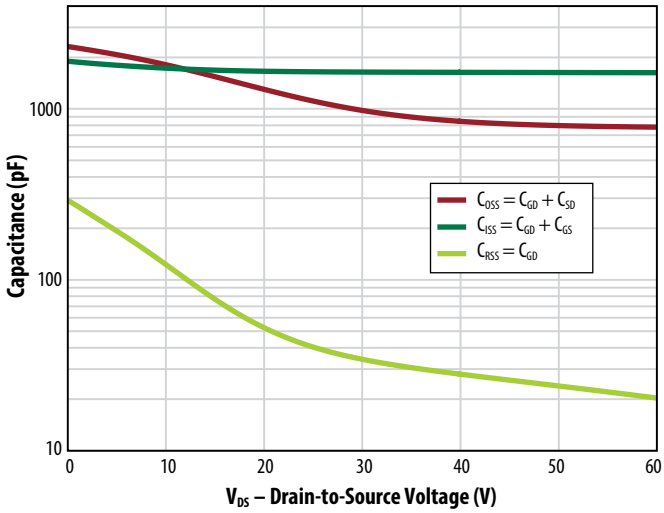


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

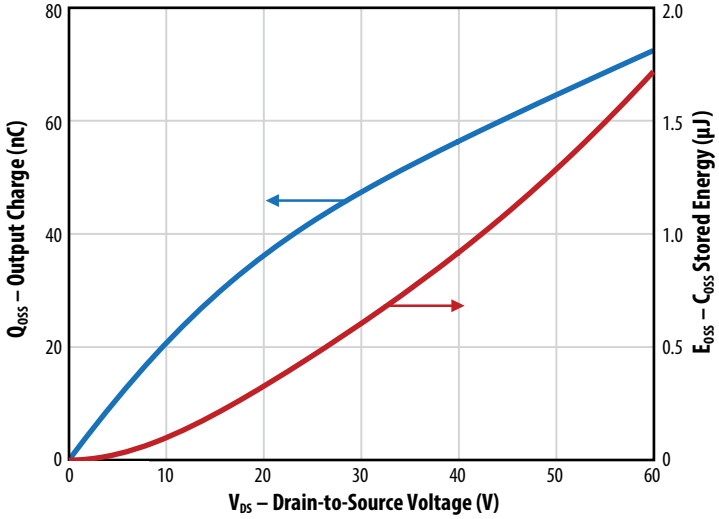


Figure 7: Typical Gate Charge

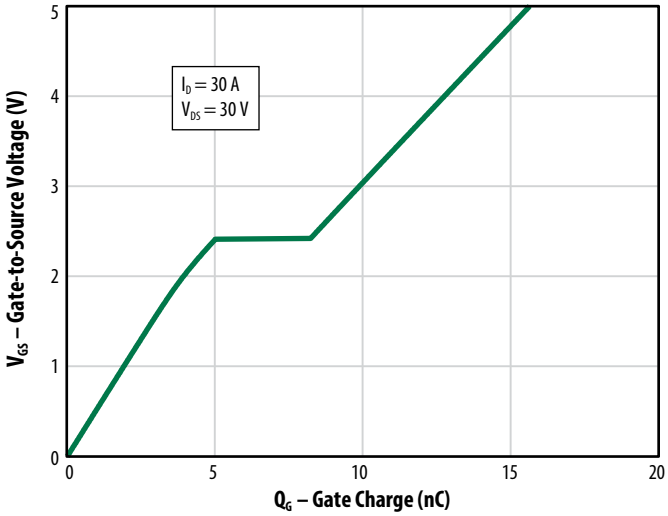


Figure 8: Typical Reverse Drain-Source Characteristics

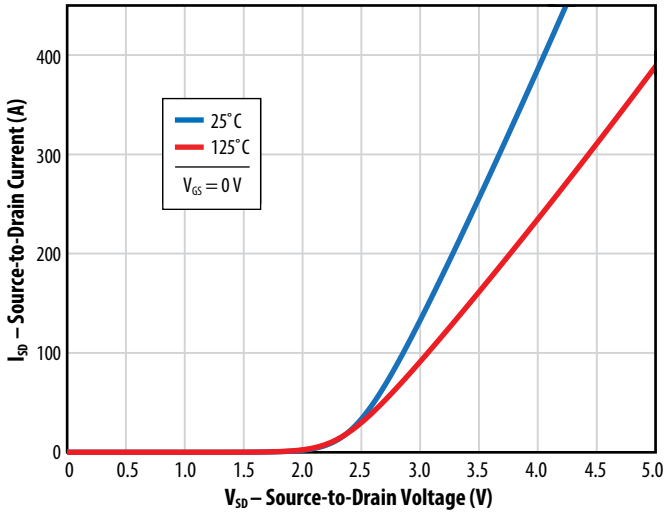
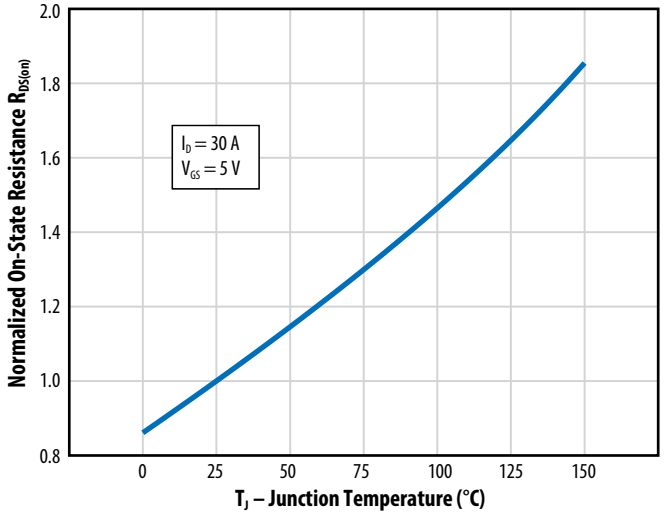


Figure 9: Typical Normalized On-State Resistance vs. Temp.



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

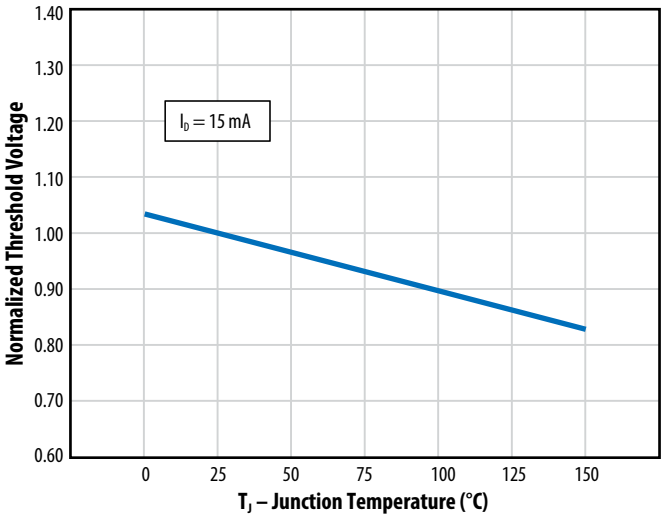


Figure 11: Safe Operating Area

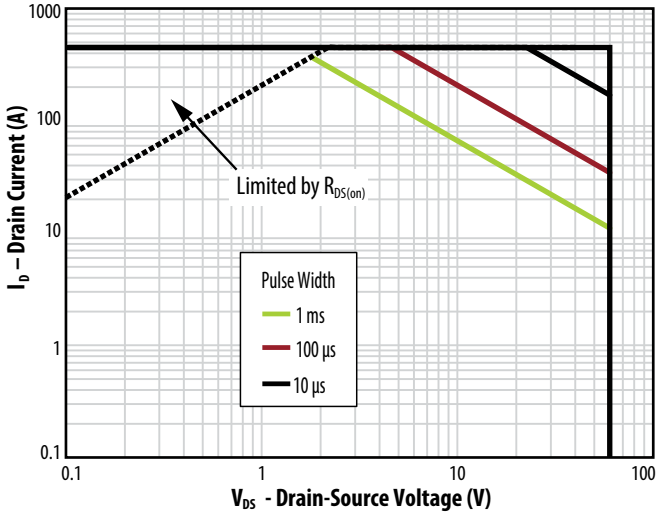
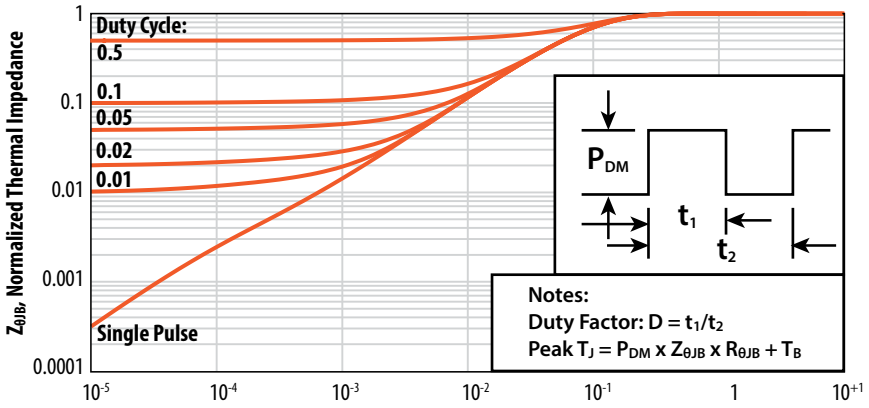
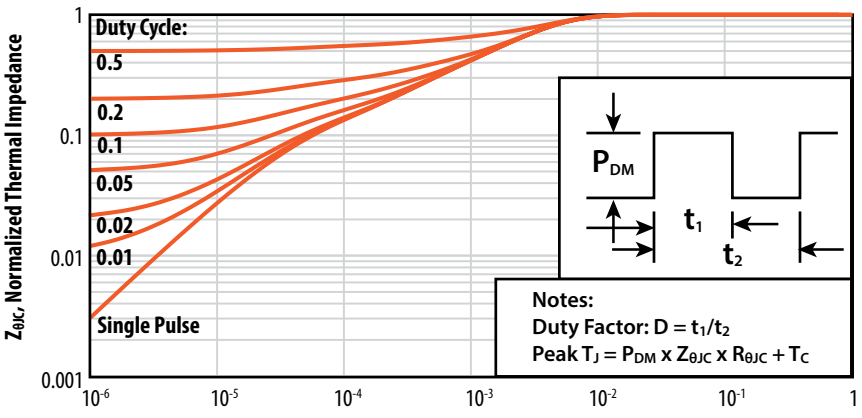


Figure 12: Typical Transient Thermal Response Curves

Junction-to-Board

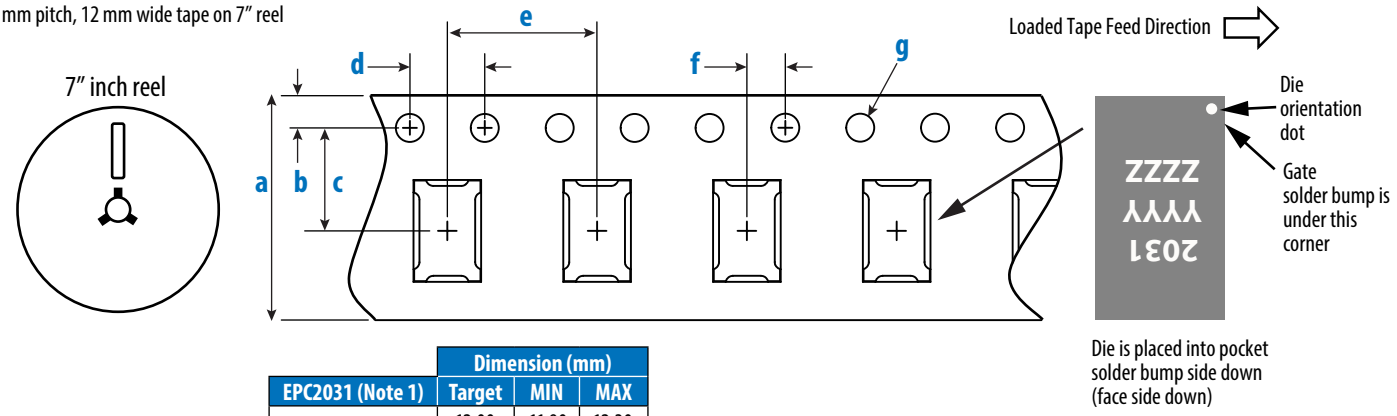


Junction-to-Case



TAPE AND REEL CONFIGURATION

8 mm pitch, 12 mm wide tape on 7" reel

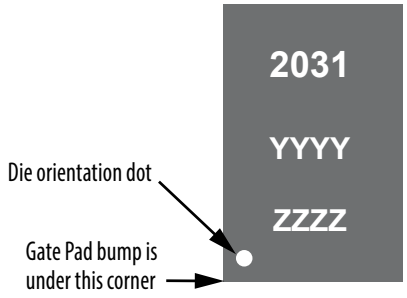


EPC2031 (Note 1)	Dimension (mm) Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

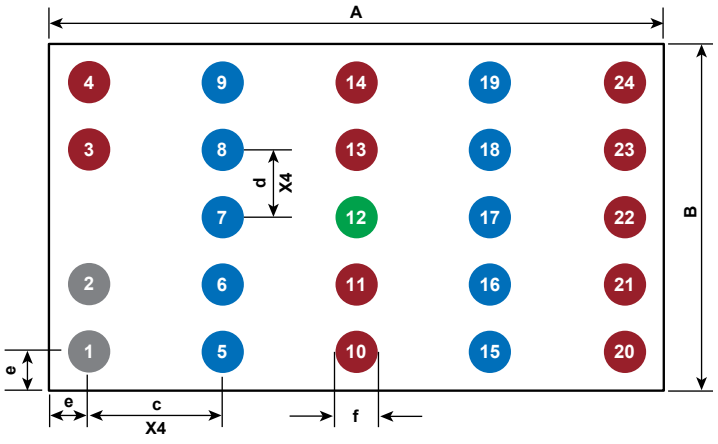
DIE MARKINGS



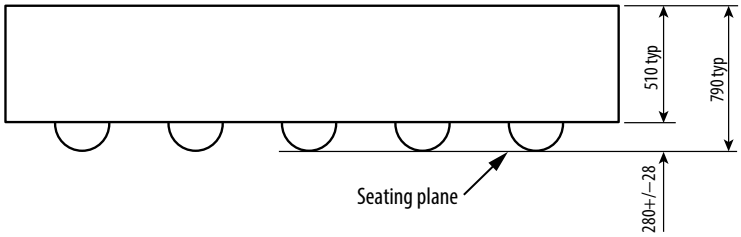
Part Number	Laser Markings Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2031	2031	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



Side View



DIM	Micrometers MIN	Nominal	MAX
A	4570	4600	4630
B	2570	2600	2630
c	1000	1000	1000
d	500	500	500
e	285	300	315
f	332	369	406

Pads 1 and 2 are Gate;

Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;

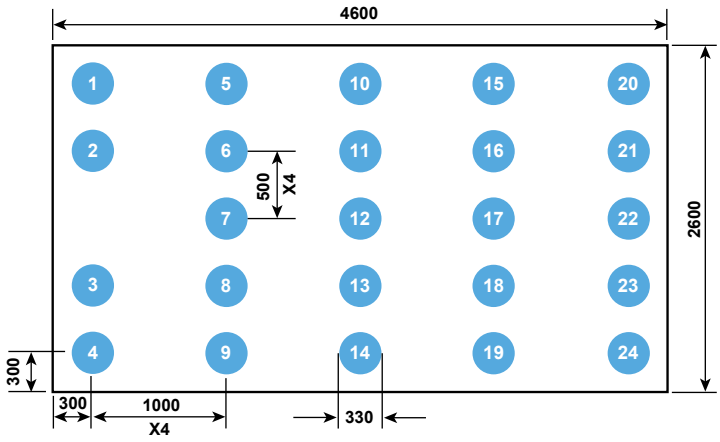
Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;

Pad 12 is Substrate*

*Substrate pin should be connected to Source

RECOMMENDED LAND PATTERN

(units in µm)



Land pattern is solder mask defined.

Pads 1 and 2 are Gate;

Pads 5, 6, 7, 8, 9, 15, 16, 17, 18, 19 are Drain;

Pads 3, 4, 10, 11, 13, 14, 20, 21, 22, 23, 24 are Source;

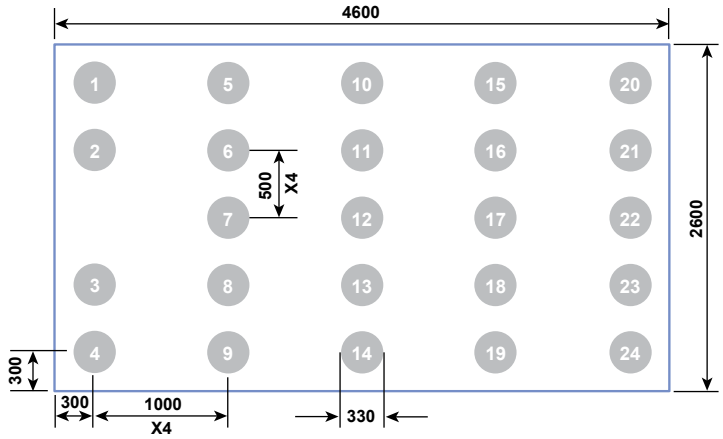
Pad 12 is Substrate*

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING

(units in µm)

Option 1 : Intended for use with SAC305 Type 4 solder.

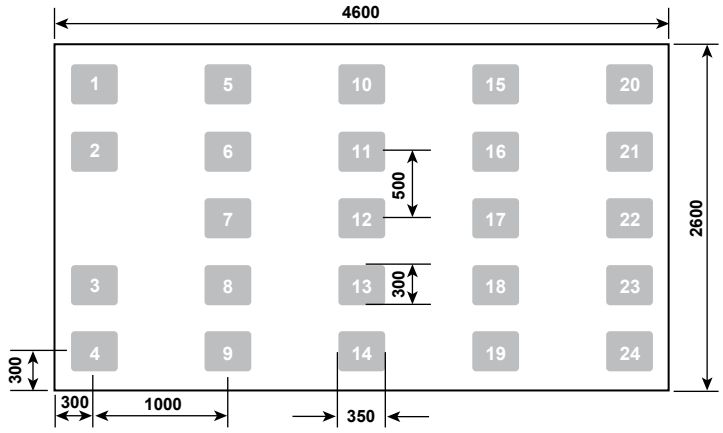


Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

RECOMMENDED STENCIL DRAWING

(units in µm)

Option 2 : Intended for use with SAC305 Type 3 solder.



Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Additional assembly resources available at https://epc-co.com/epc/design-support