IS32LT3126

150MA DUAL CHANNEL LED DRIVER WITH FAULT DETECTION

April 2024

GENERAL DESCRIPTION

The IS32LT3126 is a dual linear programmable current regulator consisting of 2 independently controlled output channels; each channel is capable of sourcing 150mA. Both channels can be combined to provide a total of 300mA. It supports PWM dimming of both channels via power supply modulation (PSM). It also features ENx pins to individually PWM dim and independently adjust the average output current for each channel. The max current for each channel is set with its corresponding external resistor.

The UVx pins set the VCC under voltage lockout of each channel to match the LED stack for high side PWM dimming operation. In addition, the IC integrates fault protection for LED open/short, ISETx pin open/short and over temperature condition for robust operation. Detection of these failures is reported by FAULTB pin. When a fault is detected the device will disable itself and output an open drain low signal. Multiple devices can have their FAULTB pins connected to create a “one-fail-all-fail” condition. For multiple LED string applications, the device can detect a single LED short. The single LED short detection is set by a resistor divider on the STx pins. A single LED short failure is reported by the separate FAULTB_S pin.

The IS32LT3126 is targeted at the automotive market with end applications to include interior and exterior lighting. For 12V automotive applications the low dropout driver can support one to several LEDs on the output channels. It is offered in a small thermally enhanced eTSSOP-16 package.

FEATURES

- Dual channel: each channel can source up to 150mA and the two channels combined to source up to 300mA
- External resistors individually set source current
- 4% channel to channel current matching
- Individually programmable VCC under voltage lockout to match the LED stack for PSM operation
- Individual PWM dimming
- Shared fault flag for multiple devices operation
- Fault protection with flag reporting:
  - Single LED short (optional to turn off all LEDs)
  - LED string open/short
  - OUTx pins short to VCC/GND
  - ISETx pins open/short
  - Over temperature current rollback (no reporting)
  - Thermal shutdown
- External C_{STOR} capacitor keeps fault status during start/stop operation
- eTSSOP-16 package
- Operating temperature range from -40°C ~ +125°C
- RoHS & Halogen-Free Compliance
- TSCA Compliance
- AEC-Q100 Qualified with Temperature Grade 1: -40°C to 125°C

APPLICATIONS

- Automotive interior/exterior lighting:
  - Turn signal light

TYPICAL APPLICATION CIRCUIT

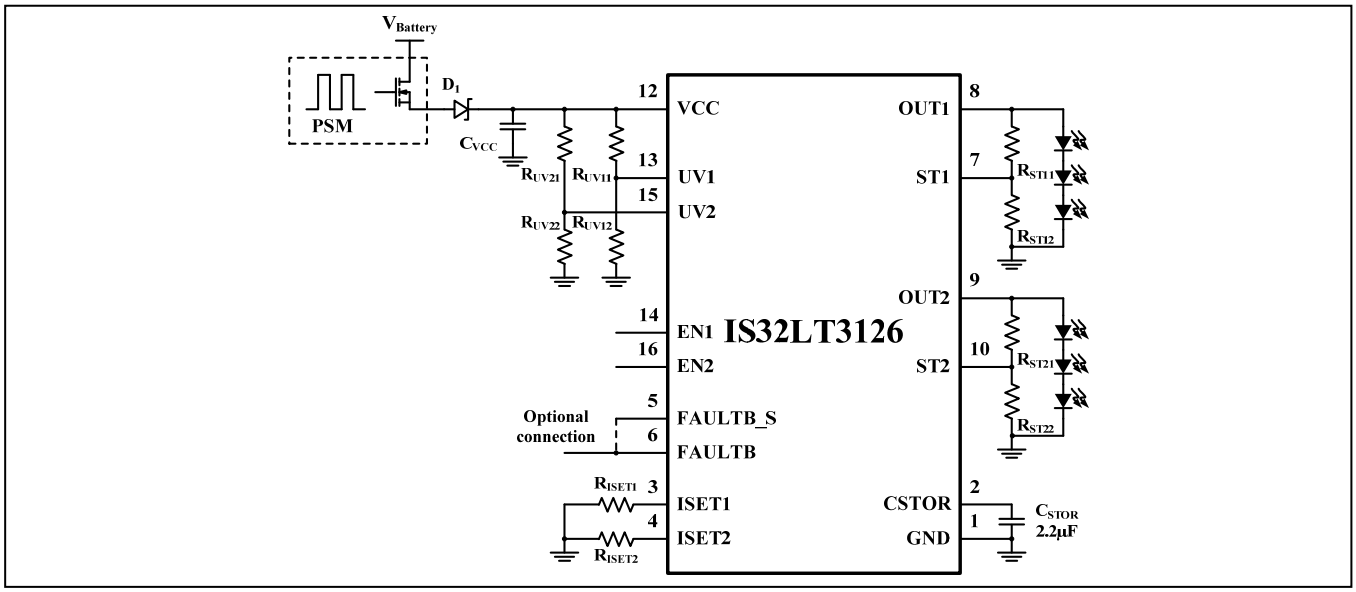


Figure 1 Typical Application Circuit

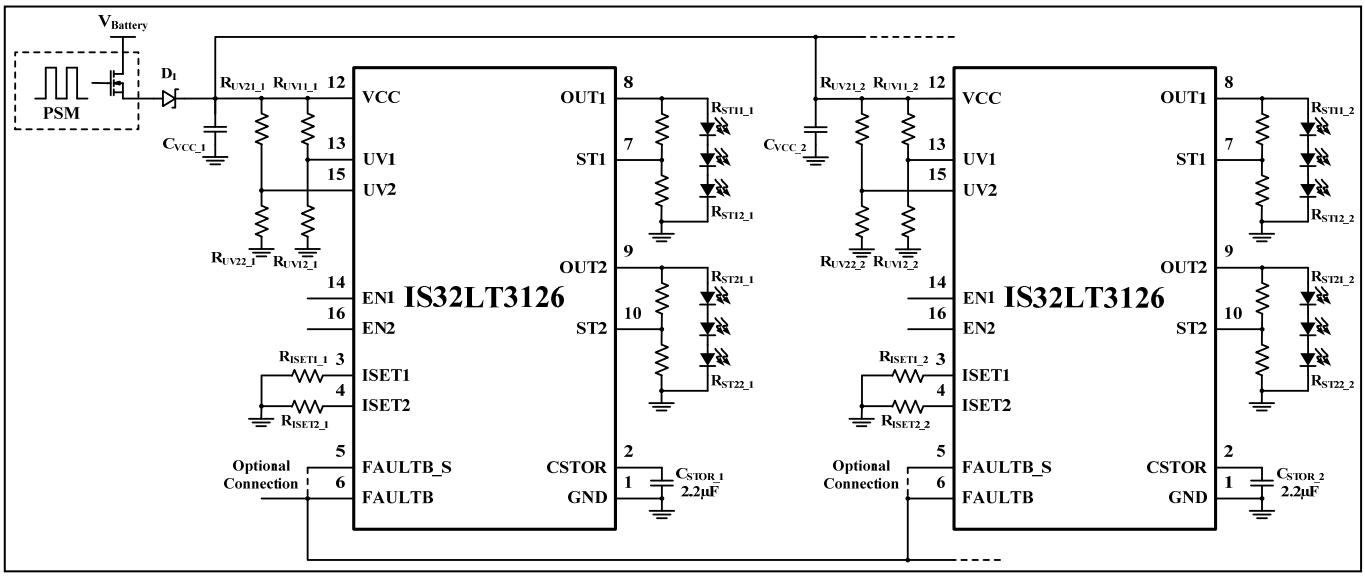
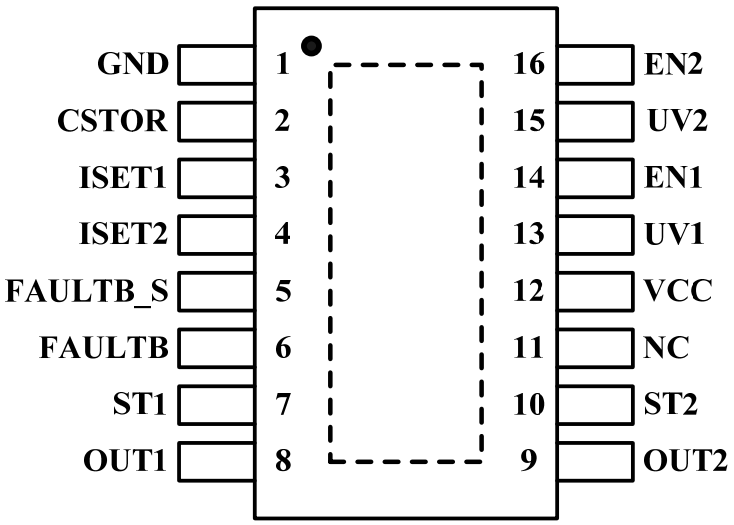


Figure 2 Typical Application Circuit (Several Devices In Parallel with FAULTB Interlinkage)

Note 1: For PSM dimming application, high C_{VCC} capacitor value will affect the dimming accuracy. To get better dimming performance, recommend 0.1μF for it.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-16	

PIN DESCRIPTION

No.	Pin	Description
1	GND	Ground.
2	CSTOR	Keep-alive capacitor to maintain the deglitch timer and fault latch status with collapsing VCC.
3	ISET1	Output current setting for channel 1. Connect a resistor between this pin and GND to set the maximum output current.
4	ISET2	Output current setting for channel 2. Connect a resistor between this pin and GND to set the maximum output current.
5	FAULTB_S	Open drain fault reporting output with internal pull up to 4.5V. Indicate the fault condition of single LED short.
6	FAULTB	Open drain fault reporting output with internal pull up to 4.5V. Indicate the fault conditions except single LED short. This pin is also an input pin. Pulling this pin low will shutdown the device.
7	ST1	LED string voltage monitor pin of OUT1 to achieve single LED short detection.
8	OUT1	Output current source channel 1.
9	OUT2	Output current source channel 2.
10	ST2	LED string voltage monitor pin of OUT2 to achieve single LED short detection.
11	NC	Not connect.
12	VCC	Power supply input pin.
13	UV1	External under voltage lockout threshold detection pin for OUT1.
14	EN1	Enable pin of OUT1. It can be used to set OUT1 current by PWM.
15	UV2	External under voltage lockout threshold detection pin for OUT2.
16	EN2	Enable pin of OUT2. It can be used to set OUT2 current by PWM.
	Thermal Pad	Must be electrically connected to GND plane for better thermal dissipation.

ORDERING INFORMATION

Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3126-ZLA3-TR	eTSSOP-16, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS

VCC, OUT1, OUT2, EN1, EN2, UV1, UV2, ST1, ST2	-0.3V ~ +45V
ISET1, ISET2, CTSOR, FAULTB, FAULTB_S	-0.3V ~ +7.0V
Ambient operating temperature, T_A=T_J	-40°C ~ +125°C
Maximum continuous junction temperature, $T_{J(MAX)}$	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Maximum power dissipation, P_{DMAX}	2.15W
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JEDEC standard), θ_{JA}	46.5°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JEDEC standard), θ_{JP}	1.617°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_J = -40°C ~ +125°C, V_{CC}=12V, the detail refers to each condition description. Typical values are at T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Power Up Parameter						
V_{CC}	Supply voltage range		5		42	V
V_{UVLO}	VCC under voltage lockout threshold voltage	Voltage falling	4.2	4.5	4.8	V
V_{UVLO_HY}	VCC under voltage lockout voltage hysteresis			200		mV
I_{CC}	VCC supply current	V_{ENx}= High, R_{ISETx}= 20kΩ	3		5.5	mA
I_{SD}	Shutdown current in normal mode	V_{ENx}= Low, T_J= 25°C		1	2	mA
I_{SD_FLT}	Shutdown current in fault mode	V_{ENx}= High, FAULTB= Low T_J= 25°C		1	2	mA
t_{SD}	Both of EN pins low time for IC power shutdown		40	48	55	ms
t_{ON}	EN high time for IC power up	I_{OUT}= -150mA, V_{CC}= 12V V_{ENx}= High (Note 3)			40	μs
Channel Parameter						
V_{ISETx}	The ISETx voltage			1		V
I_{OUT}	Output current per channel (Note 4)	R_{ISETx}= 80kΩ, V_{HR}= 1V	-27.5	-25	-22.5	mA
		R_{ISETx}= 20kΩ, V_{HR}= 1V	-106	-100	-94	
		R_{ISETx}= 13.3kΩ, V_{HR}= 1V	-159	-150	-141	
V_{HR}	Minimum headroom voltage	V_{CC} - V_{OUT}, I_{OUT}= -150mA			1100	mV
		V_{CC} - V_{OUT}, I_{OUT}= -100mA			800	

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_J = -40°C ~ +125°C, V_{CC}=12V, the detail refers to each condition description. Typical values are at T_J = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_{OUT_R}	Output current per channel range	R_{ISETx}= 80kΩ, I_{OUT}=-25mA R_{ISETx}= 13.33kΩ, I_{OUT}=-150mA	-150		-25	mA
I_{OUT_L}	Output limit current per channel	R_{ISETx}=5kΩ	-290	-230	-170	mA
ΔI_{OUT}	Current matching	R_{ISETx}=20kΩ	-4		4	%
t_{SL}	Current slew time	Enable by ENx pin, current rise/fall between 0%~100%		4		μs
I_{LEAK}	Leakage current per channel	V_{ENx}=Low, V_{OUT}=0V, V_{CC}=42V			1	μA
Fault Protect Parameter						
t_{FD}	Fault deglitch time	Fault must be present at least this long to trigger the fault detect		25		μs
V_{FAULTB}	FAULTB pin voltage	Sink current=20mA		0.2	0.4	V
R_{FAULTB}	FAULTB pin internal pull up			210	300	KΩ
V_{FAULTB_IH}	FAULTB pin input high enable threshold				2	V
V_{FAULTB_IL}	FAULTB pin input low disable threshold		0.8			V
V_{FAULTB_S}	FAULTB_S pin voltage	Sink current=20mA		0.2	0.4	V
V_{SCD}	OUTx pin short to GND threshold	Measured at OUTx	1.0	1.2	1.5	V
V_{SCD_HY}	OUTx pin short to GND hysteresis	Measured at OUTx		220		mV
V_{OCD}	OUTx pin open threshold	Measured at (V_{CC}-V_{OUTx})	150	225	300	mV
V_{OCD_HY}	OUTx pin open hysteresis	Measured at (V_{CC}-V_{OUTx})		100		mV
I_{CST}	CSTOR pin leakage current	V_{CSTOR}=5.5V		5	10	μA
T_{RO}	Thermal rollback threshold	(Note 3)		145		°C
T_{SD}	Thermal shutdown threshold	(Note 3)		165		°C
T_{HY}	Over-temperature hysteresis	(Note 3)		25		°C
Logic Input						
V_{EN}	ENx input voltage threshold	Voltage rising	1.18	1.23	1.28	V
V_{ENHY}	ENx input hysteresis	(Note 3)		40		mV
f_{PWM}	PWM frequency to ENx	(Note 3)			1	kHz
V_{UV}	UVx input voltage threshold	Voltage rising	1.18	1.23	1.28	V
V_{UVHY}	UVx input hysteresis			40		mV
V_{ST}	STx input voltage threshold	Voltage falling	1.12	1.16	1.20	V
V_{STHY}	STx Input hysteresis			40		mV
R_{STPL}	STx pull up resistor	V_{ST}=1V		500		kΩ

Note 3: Guaranteed by design.

Note 4: Output current accuracy is not intended to be guaranteed at output voltages less than 1.5V.

TYPICAL PERFORMANCE CHARACTERISTICS

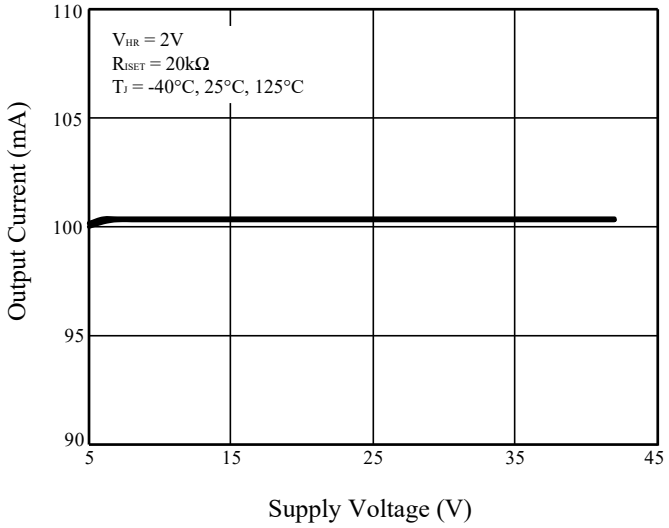


Figure 3 I_{OUT} vs. V_{CC}

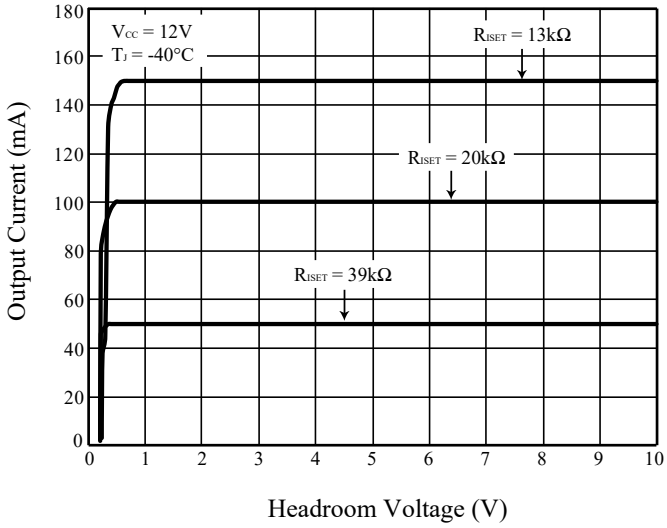


Figure 4 I_{OUT} vs. V_{HR}

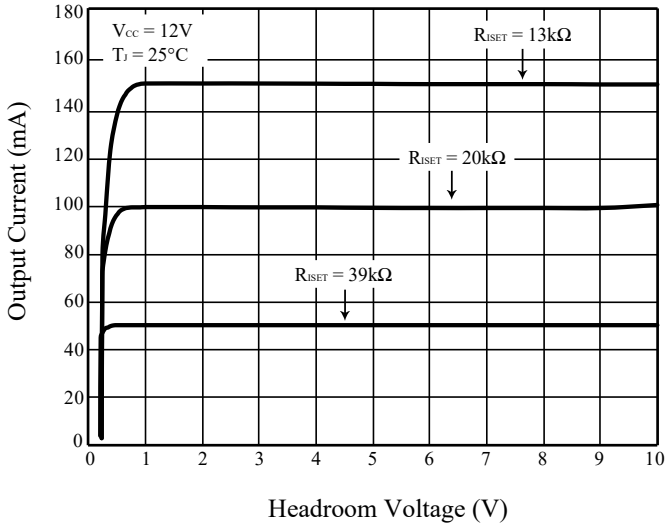


Figure 5 I_{OUT} vs. V_{HR}

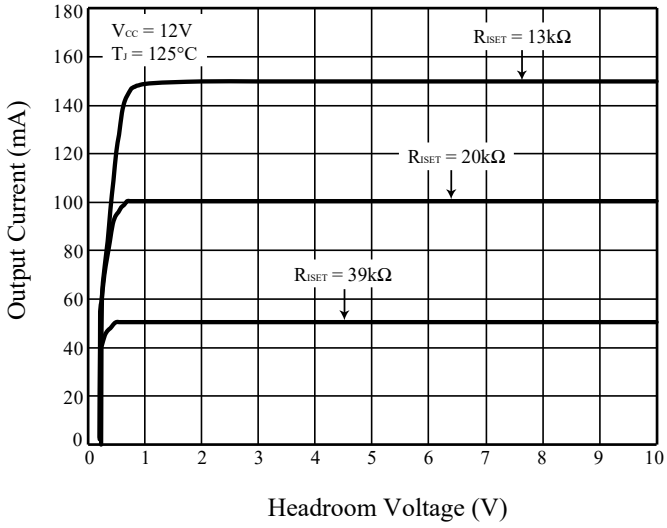


Figure 6 I_{OUT} vs. V_{HR}

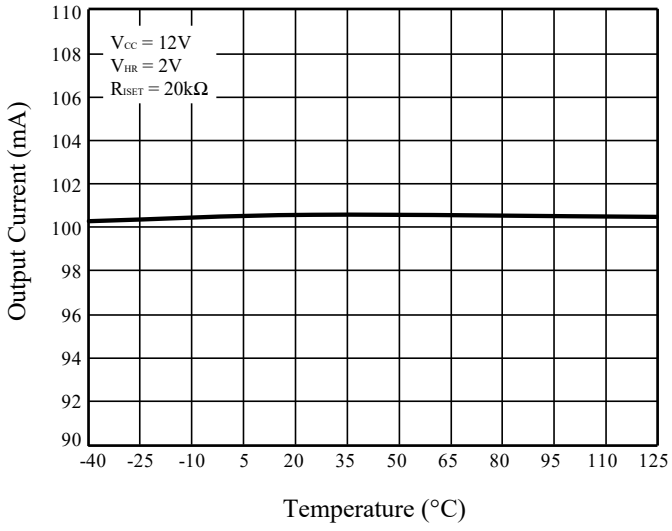


Figure 7 I_{OUT} vs. T_J

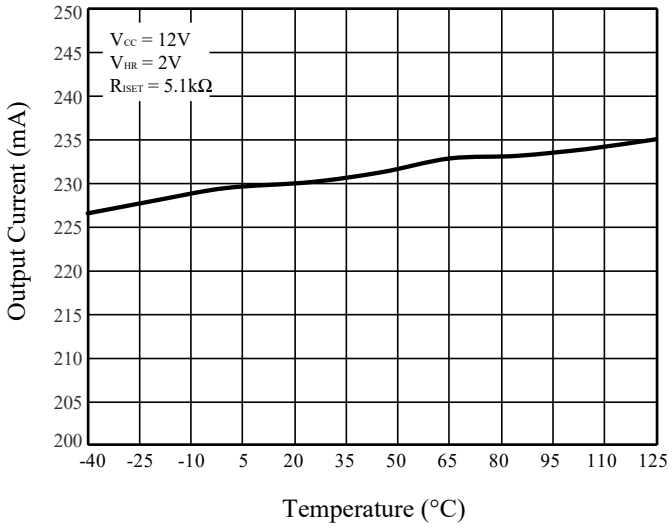


Figure 8 I_{OUT_L} vs. T_J

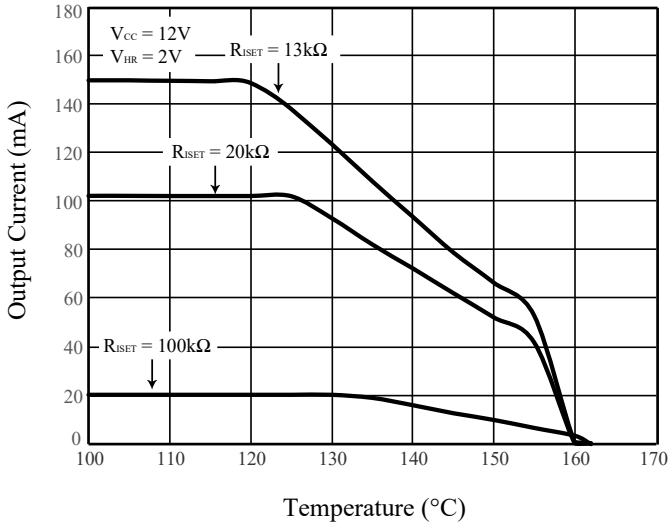


Figure 9 I_{OUT} vs. T_A (Thermal Rolloff)

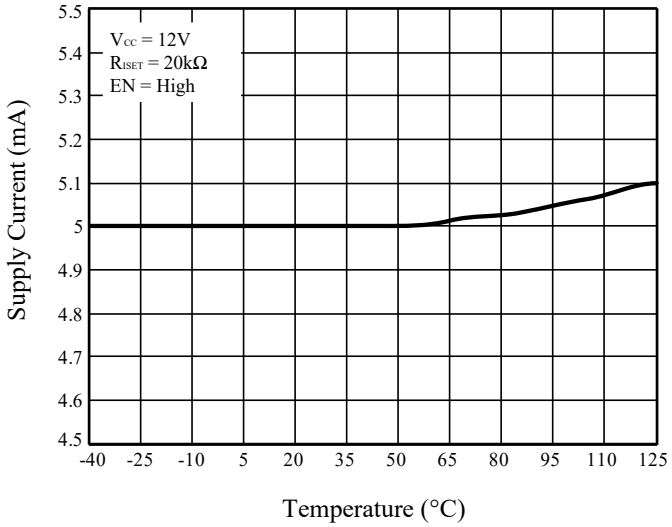


Figure 10 I_{CC} vs. T_J

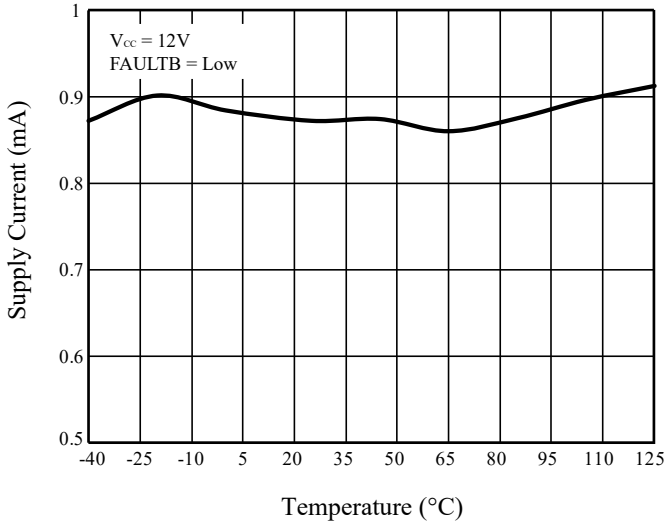


Figure 11 I_{SD_FLT} vs. T_J

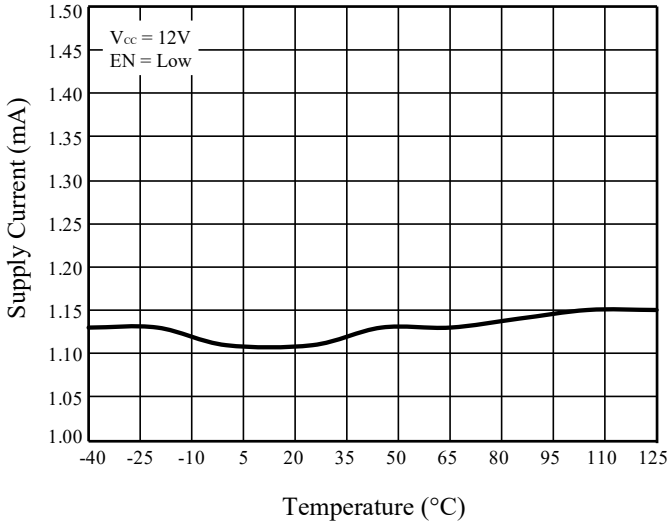


Figure 12 I_{SD} vs. T_J

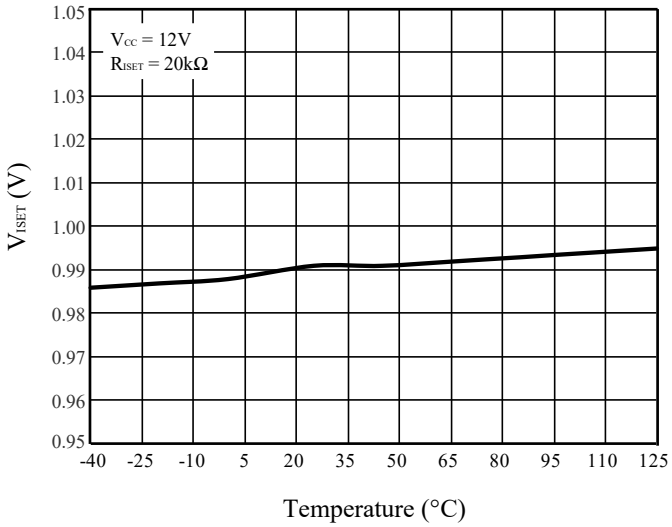


Figure 13 V_{ISET} vs. T_J

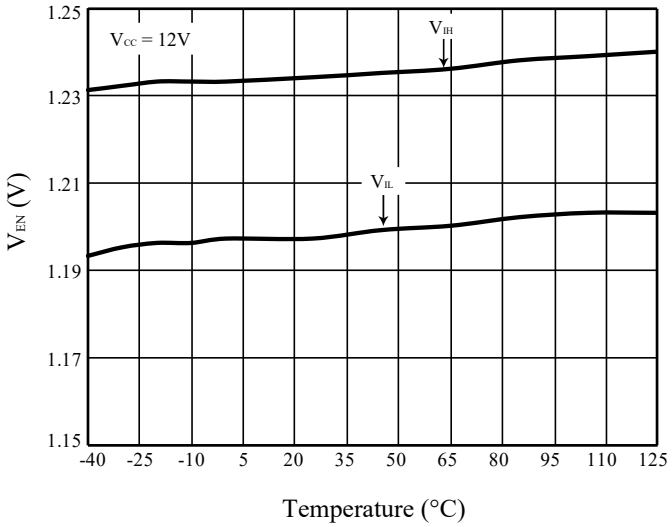


Figure 14 V_{EN} vs. T_J

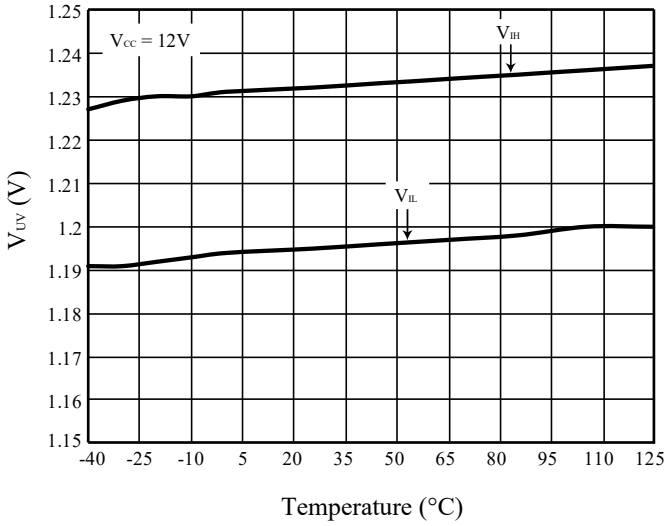


Figure 15 V_{UV} vs. T_J

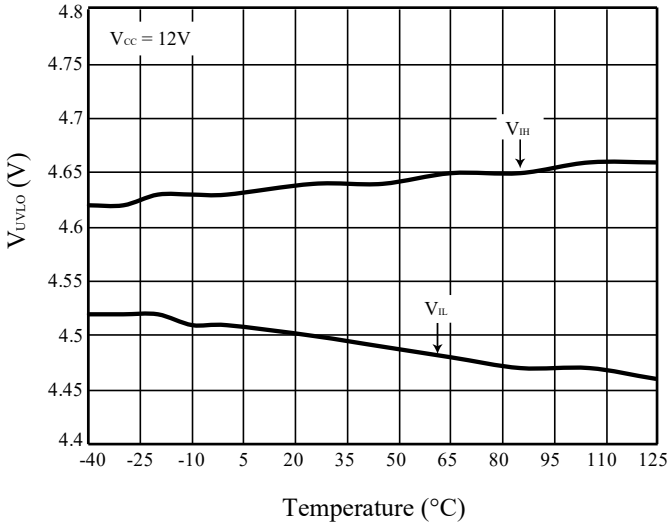


Figure 16 V_{UVLO} vs. T_J

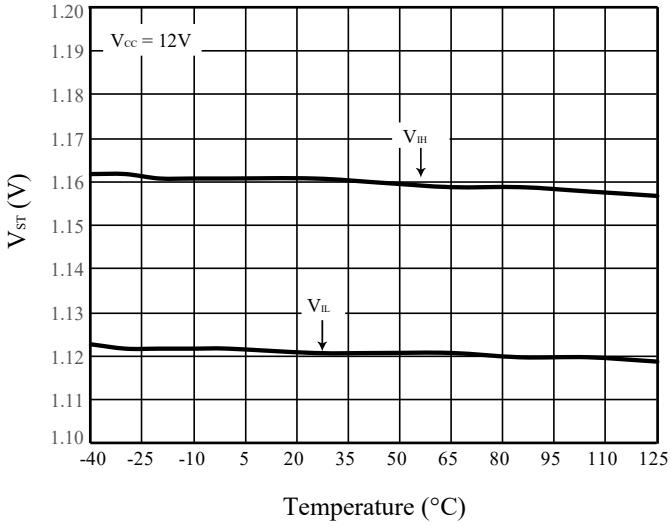


Figure 17 V_{ST} vs. T_J

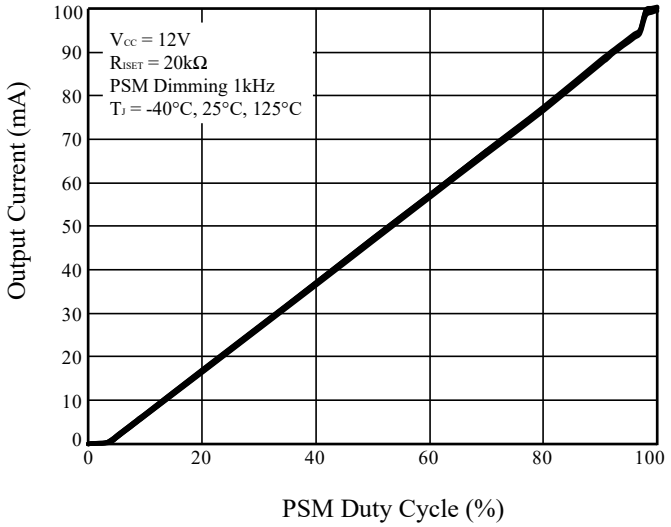


Figure 18 PSM Dimming at 1kHz

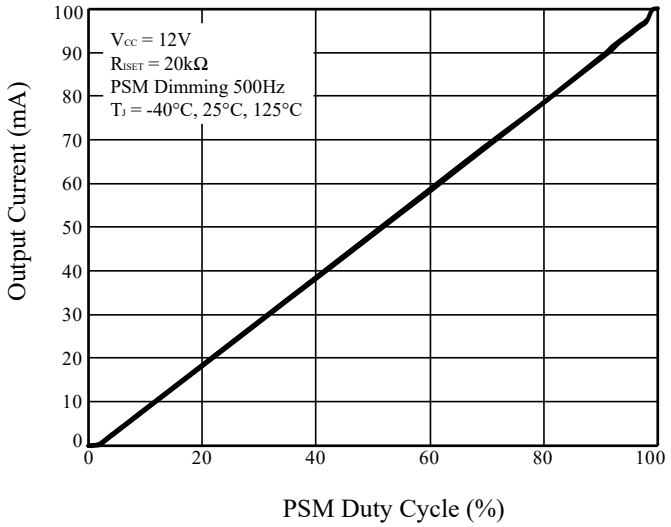


Figure 19 PSM Dimming at 500Hz

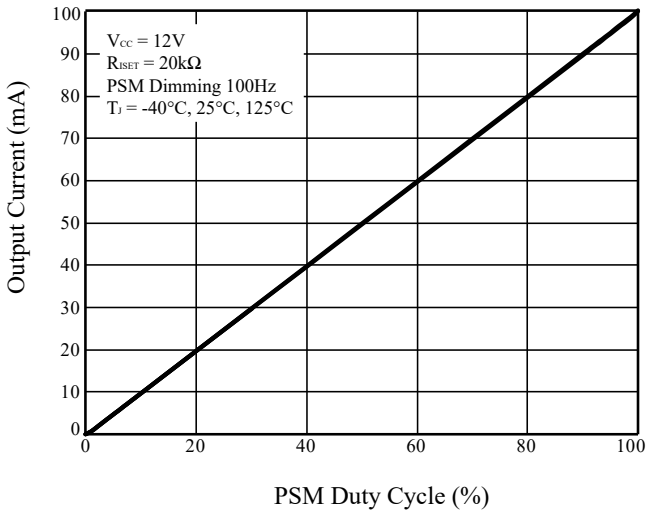


Figure 20 PSM Dimming at 100Hz

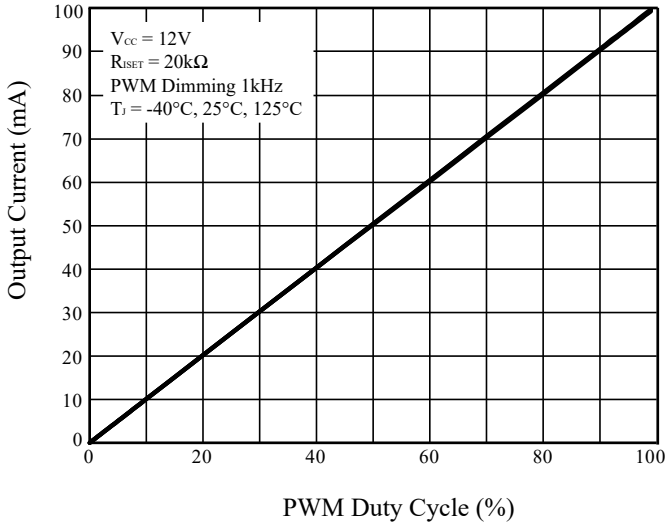


Figure 21 PWM Dimming at 1kHz

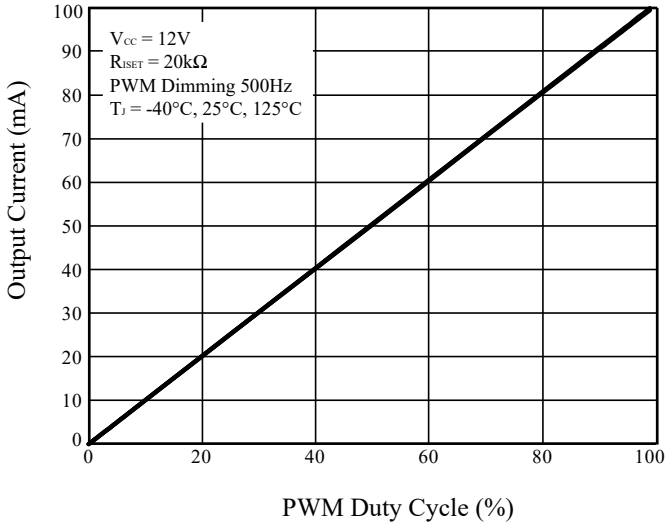


Figure 22 PWM Dimming at 500Hz

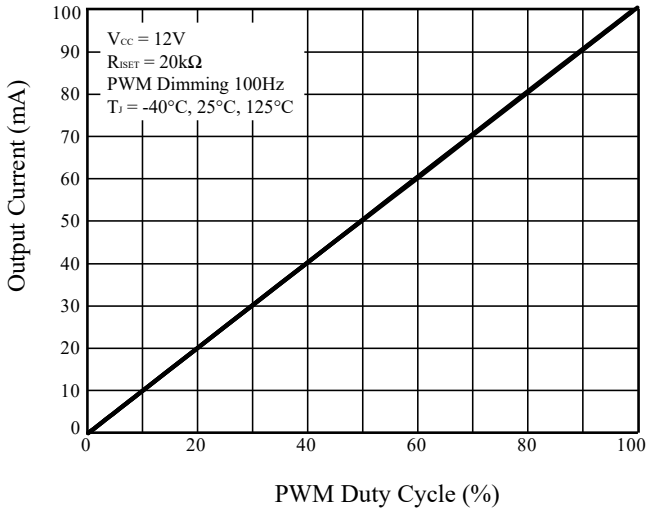


Figure 23 PWM Dimming at 100Hz

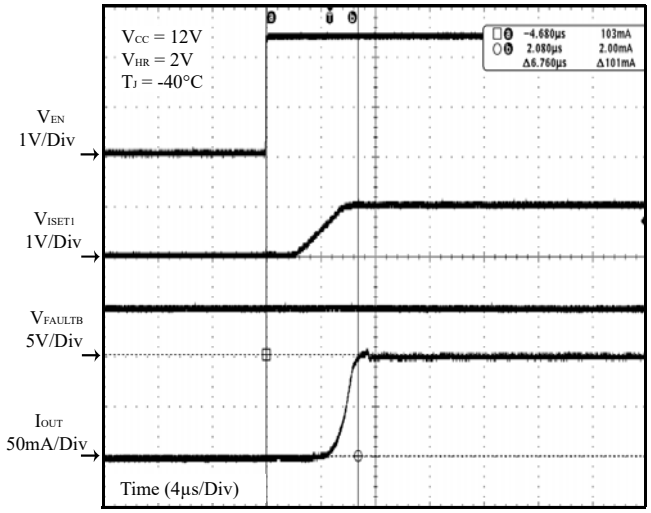


Figure 24 EN On

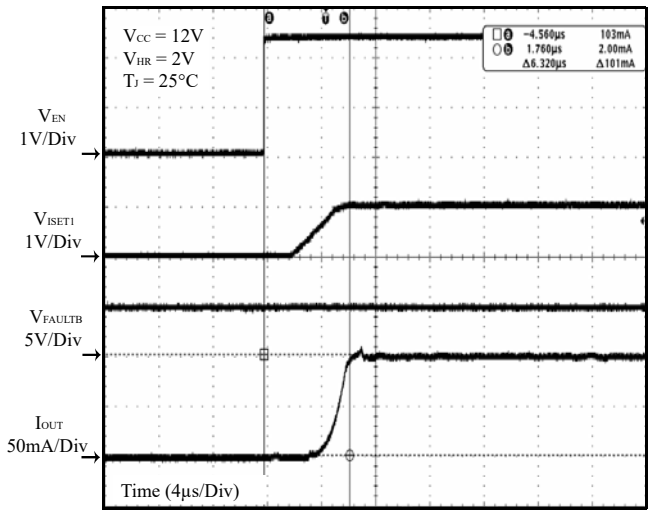


Figure 25 EN On

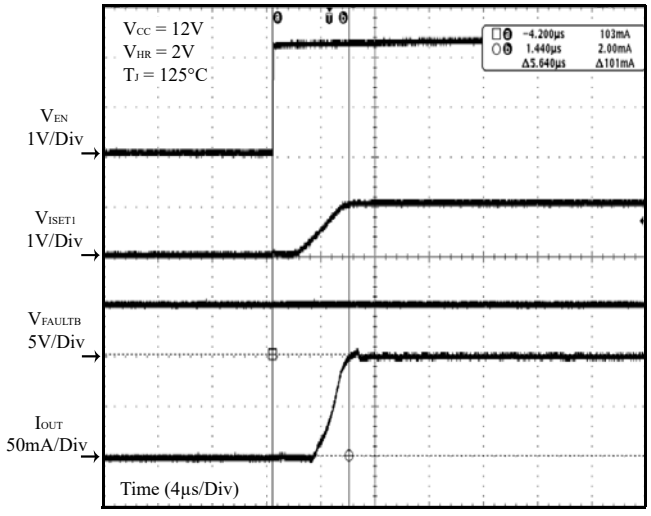


Figure 26 EN On

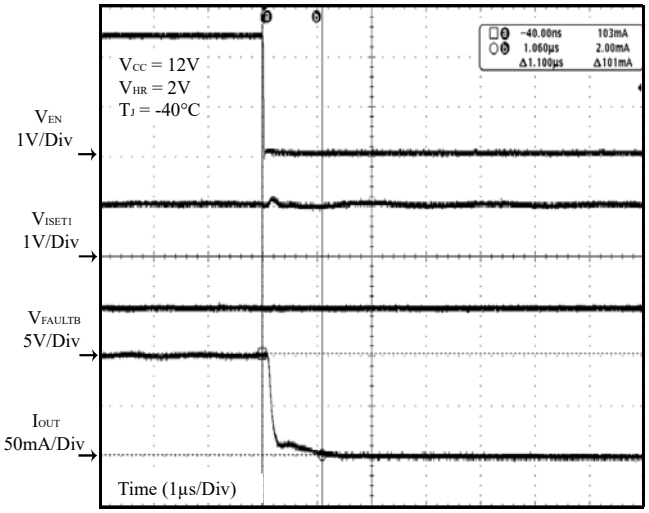


Figure 27 EN Off

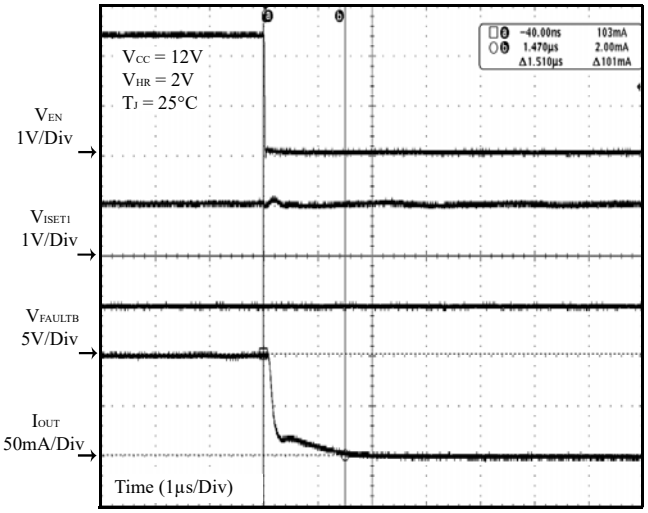


Figure 28 EN Off

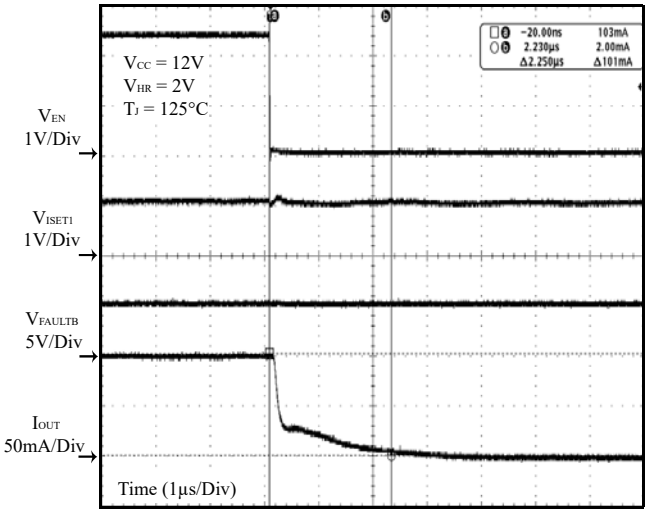


Figure 29 EN Off

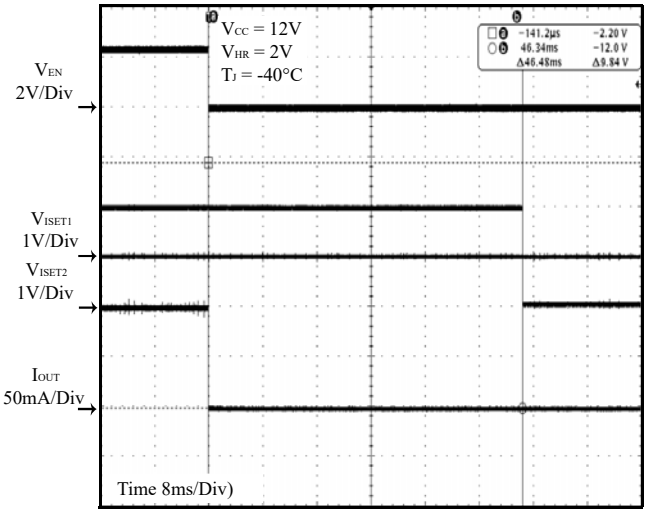


Figure 30 t_{SD}

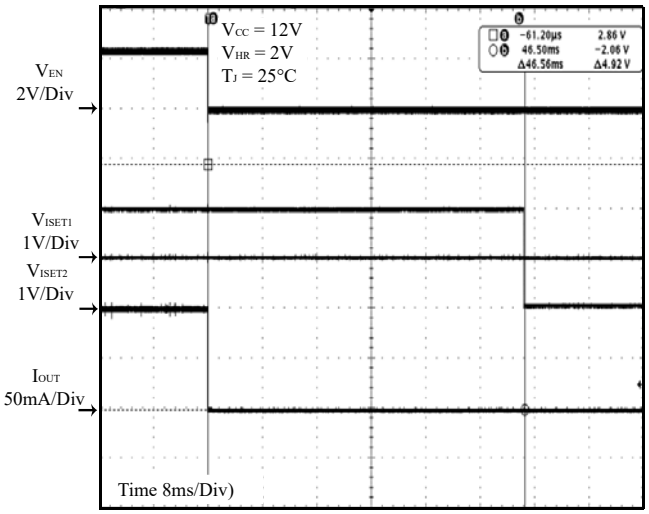


Figure 31 t_{SD}

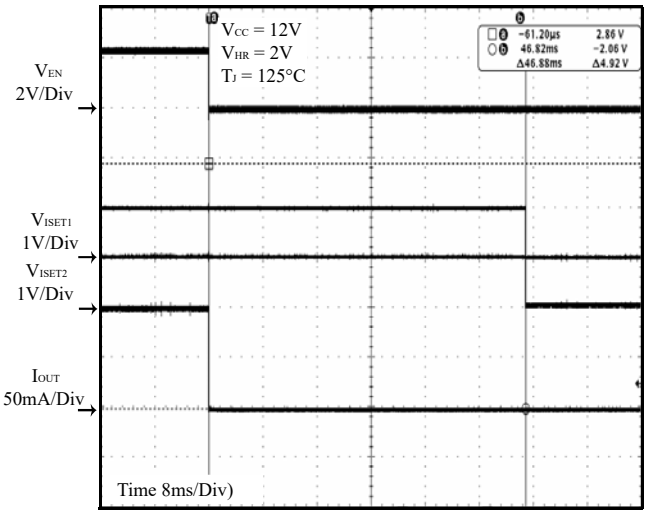
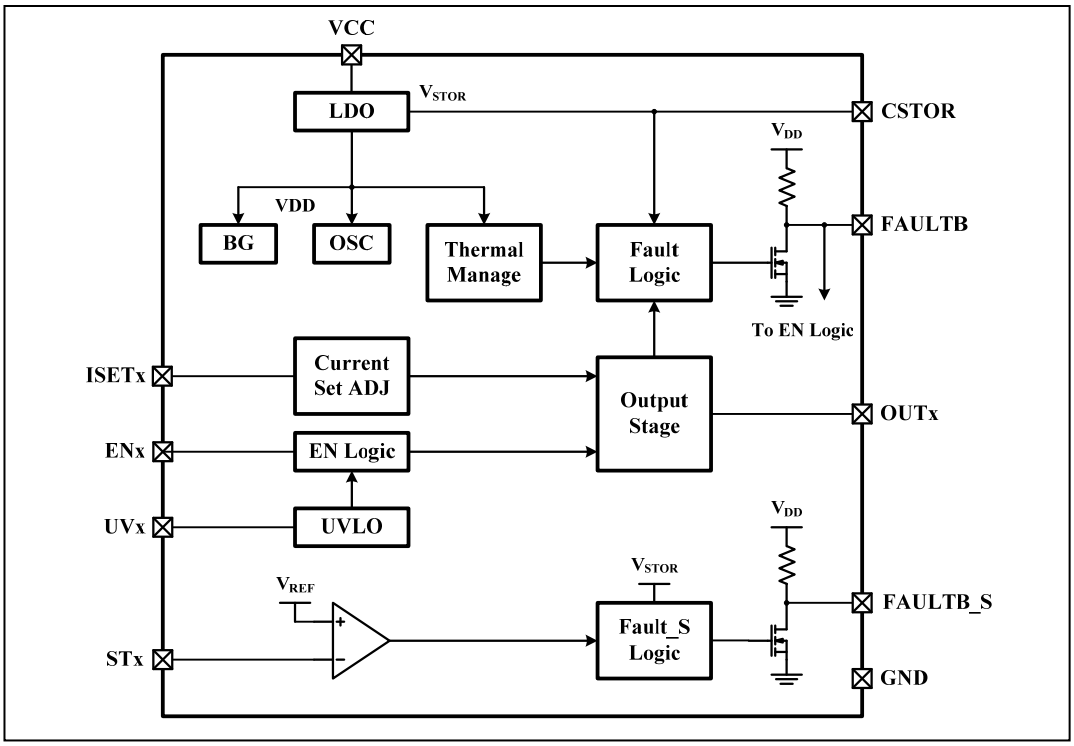


Figure 32 t_{SD}

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS32LT3126 is a 2-channel linear LED current source optimized to drive automotive interior or exterior LED light which can be dimmed via Power Supply Modulation (PSM) or by digitally driving the EN pin.

Each of the 2 output channels is capable of 150mA. The output current is set by two reference resistors (R_{ISETx}); one for each channel.

OUTPUT CURRENT SETTING

A single resistor (R_{ISETx}) controls the maximum output current for each channel. The resistor value for a specific current level is calculated using the following Equation (1):

$$R_{ISET} = \frac{2000}{I_{SET}} \qquad (1)$$

(13.33kΩ≤R_{ISET}≤80kΩ)

R_{ISET} need to be chosen 1% accuracy resistor with good temperature characteristic to ensure stable output current.

The device is protected from an output overcurrent condition caused by a too low value R_{ISETx}, by internally limiting the maximum current to I_{OUT_L}.

If only one channel is used, the EN pin of the unused channel should be tied to GND to prevent unwanted fault reporting.

POWER SUPPLY MODULATION DIMMING

The IS32LT3126 can operate with Power Supply Modulation (PSM) where the device's power supply is pulse width modulated to achieve LED dimming. The IS32LT3126 stability is not affected by operation with PSM. To get better dimming linearity, the recommended PSM frequency can be in the range of 100Hz to 300Hz, (200Hz Typ.) and input capacitor, C_{VCC}, should be low value (0.1μF Typ.) to ensure rapid discharge during PSM low period.

CSTOR OPERATION

To keep the IC operating normally during condition of PSM when V_{CC} goes to zero, C_{STOR} capacitor provides the keep-alive current needed to power the digital counter and the fault flag circuits. A capacitor value of 2.2μF is recommended. The keep-alive time could be roughly calculated by the following Equation (2):

$$t_{alive} = \frac{2.5V \times C_{STOR}}{I_{CST}} \qquad (2)$$

ENx PINS OPERATION

The voltage at the ENx pins must be higher than V_{EN} to enable the channel and below (V_{EN}-V_{ENHY}) to disable the channel. The ENx pins of the IS32LT3126 can accept a PWM signal to implement LED dimming. LED average current may be computed using the following Equation (3).

$$I_{LED} = I_{MAX} \times D_{PWM} \qquad (3)$$

I_{MAX} is computed using Equation (1) and D_{PWM} is the duty cycle. To guarantee a reasonably good dimming effect, recommend PWM frequency in the range of 100Hz ~ 1kHz. Driving the ENx pins with a PWM signal can effectively adjust the LED intensity. The PWM signal voltage levels must meet the ENx pins input voltage levels, V_{EN}. Tie them to VCC pin via a 10KΩ resistor when ENx pins are unused; do not leave them floating.

UVx PINS OPERATION

The IC has an internal VCC UVLO set at V_{UVLO}. However, it may be desirable to externally set an UVLO to track the number of LED's used in the string. For PSM dimming application, the higher UVLO will track the PSM off time to a pre-determined VCC level. In addition, it is necessary to prevent false LED open detection due to the LED string losing its headroom voltage, such as when VCC rises up from zero during power up or PSM dimming. The UVx pin can be used to independently set a VCC under voltage lockout threshold via a resistor divider for each channel.

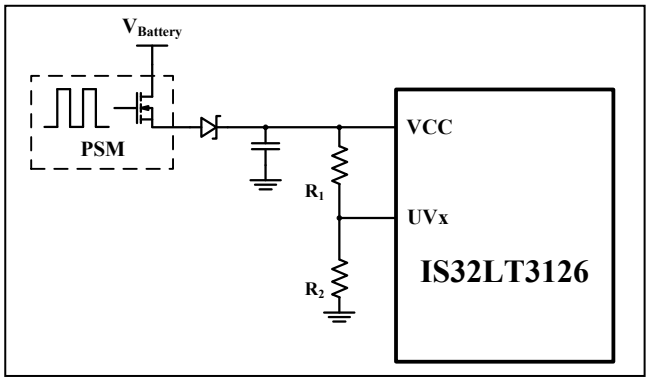


Figure 33 UVx Pins Operation

This external UVLO threshold voltage can be computed using the following Equation (4):

$$V_{CC\_UVLO} = V_{UV} \times \frac{R_1 + R_2}{R_2} \qquad (4)$$

Any unused UVLO pin must be tied to VCC pin via a 10kΩ resistor; do not leave it floating.

To prevent false open detection, the external UVLO threshold voltage should be set at Equation (5):

$$V_{CC\_UVLO} > V_{LED\_MAX} + V_{OCD} \qquad (5)$$

Where V_{LED_MAX} is the maximum LED string forward voltage on the output channel.

STx PINS OPERATION

IS32LT3126 device features single LED short detection using a resistor divider on the STx pins. In the case of any single LED short will result in that the STx pin voltage to drop below the threshold voltage V_{ST} and remains for t_{FD}, the FAULTB_S pin pulls low to report the failure to host and all channels continue sourcing current. If FAULTB_S pin is tied to FAULTB pin, the FAULTB_S pin pulls down the FAULTB pin together that turns off the no fault condition channel but keep 4mA sourcing on fault channel for recovery detection. In multiple LEDs per string application, set the detection threshold voltage V_{DT} into below voltage range:

$$(N-1)\times V_{F\_max} < V_{DT} < N\times V_{F\_min} \qquad (6)$$

Where, N is the number of LEDs in the string. V_{F_max} and V_{F_min} are the maximum and minimum forward voltage of a single LED.

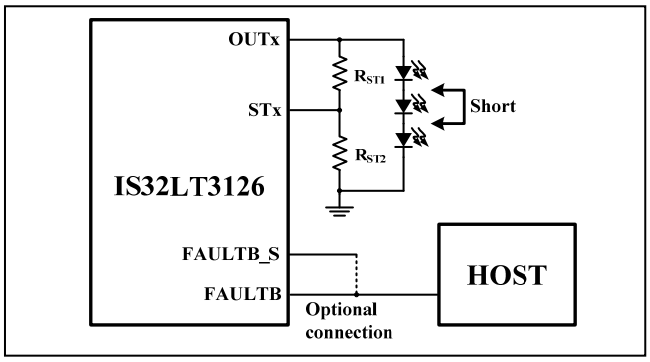


Figure 34 STx Pins Operation

The detection threshold voltage V_{DT} is calculated by the following Equation (7):

$$V_{DT} = V_{ST} \times \frac{R_{ST1} + R_{ST2}}{R_{ST2}} \qquad (7)$$

If single LED short detection is unused, the unused STx pin should be tied to its corresponding OUTx pin.

OUTPUT STATE DETECTION AND FAULT DIAGNOSTIC

IS32LT3126 offers a fault diagnostic function. Output short to GND/VCC, LED string open/short, ISET pins short/open and over temperature shutdown will trigger this function.

An output short to GND or VCC is detected as a fault if the OUTx pin voltage drops below the short detect voltage threshold V_{SCD} or VCC to OUTx drop voltage is lower than V_{OCD} and remains below the threshold for t_{FD}. Then the fault channel will change to source a 4mA current for recovery detection and the other channel will turn off. The FAULTB pin will be pulled low to indicate the fault condition. This state will recover after the fault condition is removed.

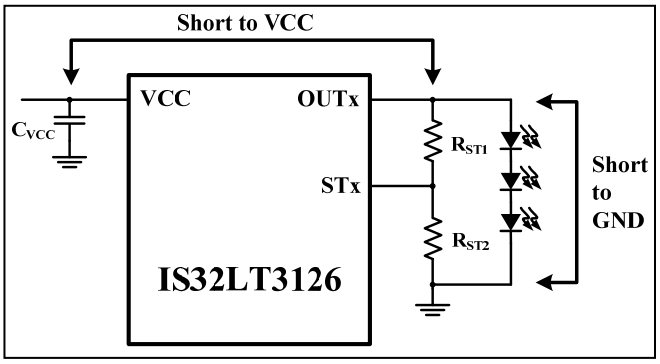


Figure 35 OUTx Pins Short Operation

In the event the LED channel is open circuited, the OUTx pin voltage will go up close to V_{CC}. If VCC to OUTx drop voltage remains below the threshold V_{OCD} for t_{FD}, the fault channel will change to source a 4mA current for recovery detection and another channel will turn off. The FAULTB pin will be pulled low to indicate the fault condition. The state will recover after the open condition is removed.

If the ISETx pin is either short or open, the FAULTB pin will pull low to assert the fault and the both channels will turn off. The state will recover after the fault condition is removed.

FAULTB PARALLEL INTERCONNECTION

For LED lighting systems which require the complete lighting system be shut down when a fault is detected, the FAULTB pin can be used in a parallel connection with multiple IS32LT3126 devices as shown in Figure 2. A detected fault output by one device will pull low the FAULTB pins of the other parallel connected devices and simultaneously turn them off. This satisfies the “One-Fail-All-Fail” operating requirement.

THERMAL ROLLBACK OF OUTPUT CURRENT

To protect the IC from damage due to high power dissipation, the temperature of the die is monitored. When the temperature of the die is below the thermal rollback start threshold of 145°C (Typ.), the dual output current maximum is the value set by the selection of R_{ISETx}. When the die temperature is between the thermal rollback start threshold 145°C (Typ.) and the over temperature shutdown threshold 165°C (Typ.), the output current decreases linearly from the maximum value. During the rollback, the FAULTB pin will not assert this as a fault.

The rollback is related to R_{ISET} value:

$$I_{OUT\_RO} = I_{OUT} - \frac{K\times(T_J - 145°C)}{R_{ISET}} \qquad (8)$$

Where 145°C ≤T_J≤165°C and K= 49.

THERMAL SHUTDOWN

In the event that the die temperature exceeds 165°C, the device will go into shutdown mode. Both channels (OUTx) will turn off. The FAULTB pin will pull low to indicate the fault. At this point, the IC begins to cool off.

Any attempt to enable one or both of the channels back to the source condition before the IC cooled to T_J<140°C will be blocked and the IC will not be allowed to restart. The device will not resume operation until the junction temperature goes below 140°C.

Table 1 Fault Table

Fault Type	Fault Condition	Fault Channel	Another Channel	FAULTB	FAULTB_S	Recovery
ISETx open	ISETx pin current close to zero	Off	Off	Low	High	ISETx pin current goes back normal
ISETx short	ISETx pin voltage close to zero	Off	Off	Low	High	ISETx pin voltage goes back normal
LED string open (OUTx short to VCC)	$(V_{CC}-V_{OUTx})<V_{OCD}$	4mA for recovery detection	Off	Low	High	$(V_{CC}-V_{OUTx})>(V_{OCD}+V_{OCD\_HY})$
LED string short (OUTx short to GND)	$V_{OUTx}<V_{SCD}$	4mA for recovery detection	Off	Low	High	$V_{OUTx}>(V_{SCD}+V_{SCD\_HY})$
One LED short	STx pin voltage drops below V_{ST}	Keep normal sourcing		High	Low	STx pin voltage rises above $(V_{ST+}V_{STHY})$
	FAULTB_S tied to FAULTB and STx pin voltage drops below V_{ST}	4mA for recovery detection	Off	Pulled low by FAULTB_S	Low	STx pin voltage rises above $(V_{ST+}V_{STHY})$
Thermal rollback	$T_J>T_{RO}$	Output current linearly decreases following T_J		High	High	$T_J<T_{RO}$
Thermal shutdown	$T_J>T_{SD}$	Off		Low	High	$T_J<(T_{SD}-T_{HY})$

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation, P_D, and the package thermal resistance, θ_{JA}, as in Equation (9) and (10):

$$P_D = V_{CC} \times I_{CC} + \sum_{x=1}^{2}(V_{CC} - V_{OUTx}) \times I_{OUTx} \qquad (9)$$

and,

$$T_J = T_A + \Delta T = T_A + P_D \times \theta_{JA} \qquad (10)$$

Where V_{CC} is the supply voltage, V_{OUTx} is the OUTx voltage and T_A is the ambient temperature.

When operating the chip at high ambient temperatures, or when driving maximum load current, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation can be calculated using the following Equation (11):

$$P_{D(MAX)} = \frac{125°C - 25°C}{\theta_{JA}} \qquad (11)$$

So,

$$P_{D(MAX)} = \frac{125°C - 25°C}{46.5°C/W} \approx 2.15W$$

Figure 36, show the power derating of the IS32LT3126 on a JEDEC boards (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

The thermal resistance is achieved by mounting the IS32LT3126 on a standard FR4 double-sided printed circuit board (PCB) with a copper area of a few square inches on each side of the board under the IS32LT3126. Multiple thermal vias, as shown in Figure 37, help to conduct the heat from the exposed pad of the IS32LT3126 to the copper on each side of the board. The thermal resistance can be reduced by using a metal substrate or by adding a heatsink.

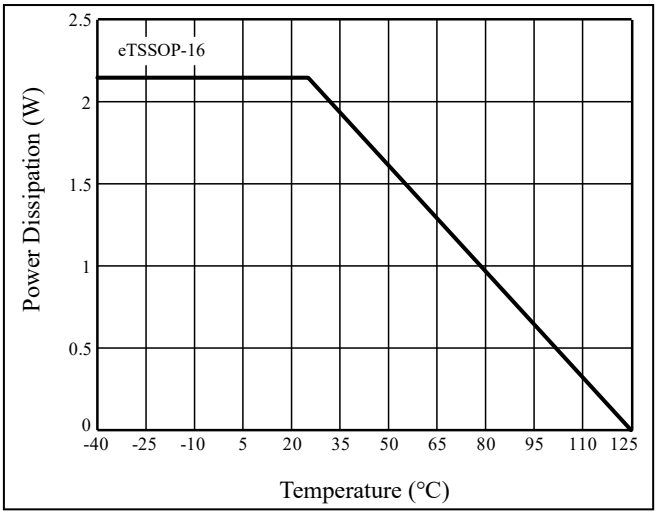


Figure 36 Dissipation Curve

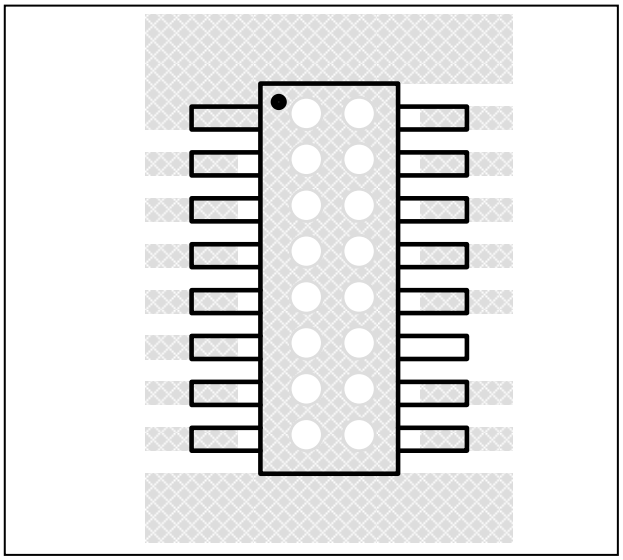


Figure 37 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

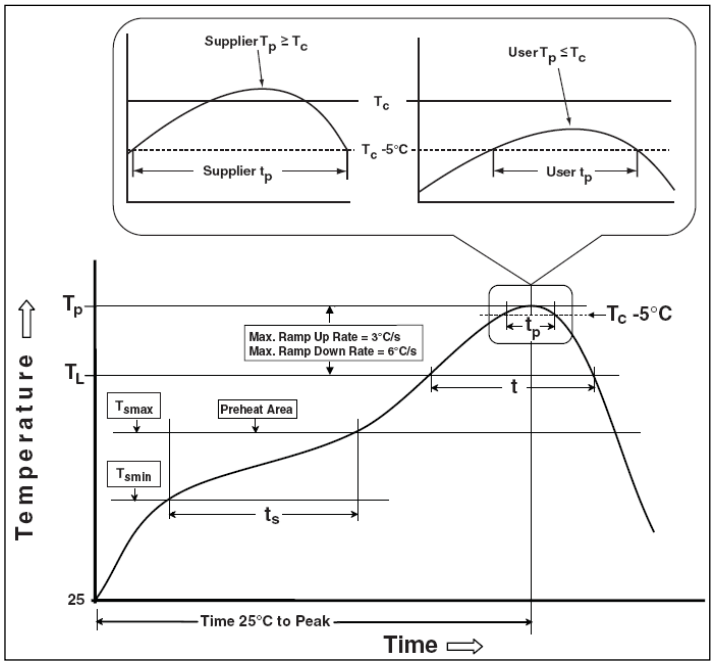
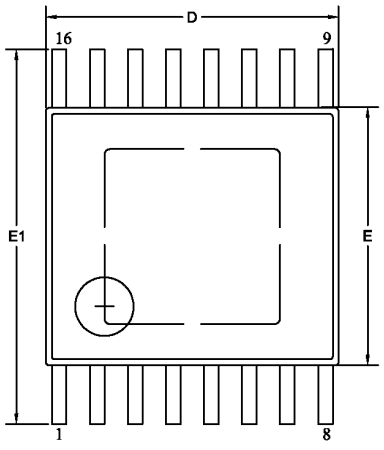


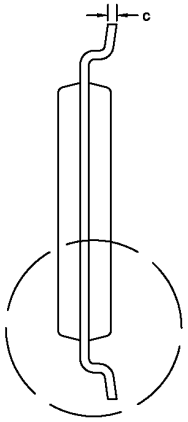
Figure 38 Classification Profile

PACKAGE INFORMATION

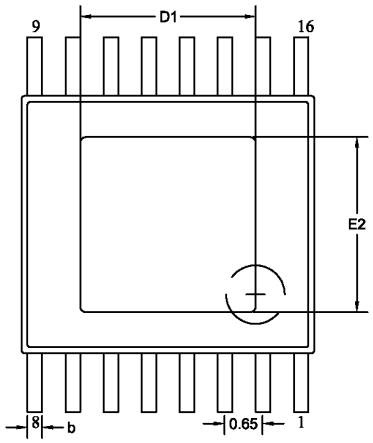
eTSSOP-16



TOP VIEW



END VIEW



BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70	—	—
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50	—	—
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

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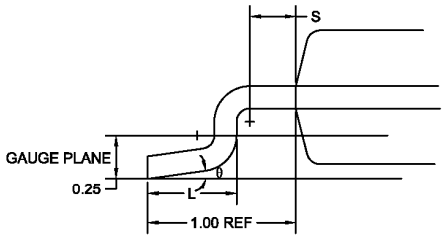
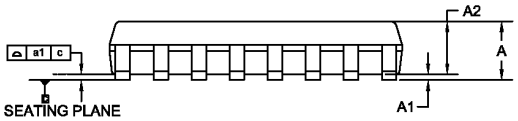


DETAIL 'A'



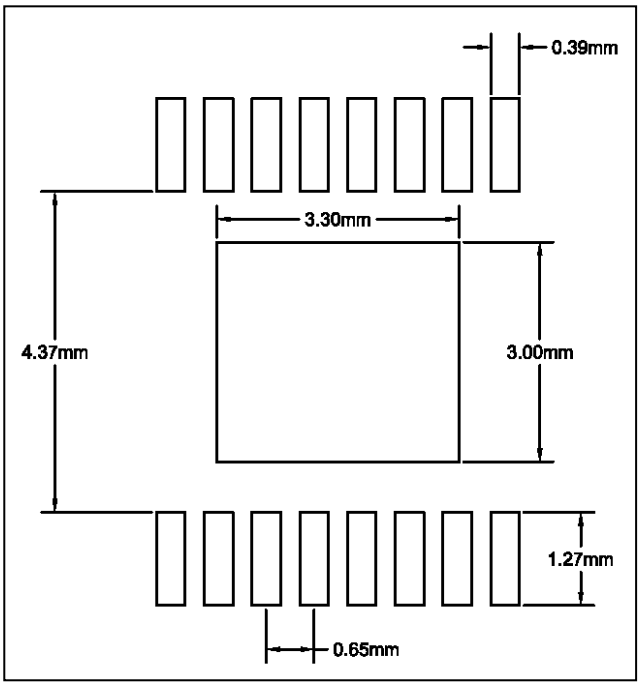
SIDE VIEW

NOTES:

1)The thermal pad shows different shape among different factories.
2)Controlling dimension:mm
3)Reference document:JEDEC MO-153

RECOMMENDED LAND PATTERN

eTSSOP-16



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release	2017.09.09
0B	Update curves and detail description	2018.01.05
A	Release to final version	2018.04.10
B	1.Update to new Lumissil logo 2.Add RoHS, update AECQ information in Features 3.Update POD and LP	2024.04.23