

## DUAL 150mA LOW QUIESCENT CURRENT FAST TRANSIENT LOW DROPOUT LINEAR REGULATOR

### Description

The AP7312 is 150mA, dual fixed output voltage, low dropout linear regulator. The AP7312 include the pass element, error amplifier, band-gap, current limit and thermal shutdown circuitry which protect the IC from damage in fault conditions. The AP7312 has two enable pins (EN1 and EN2) to independently turn the respective channel on when a logic high level is applied.

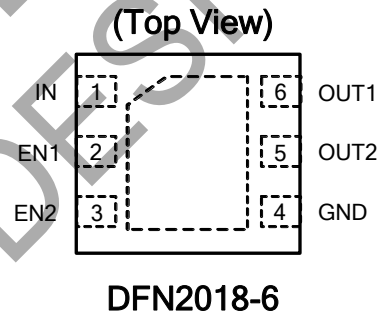
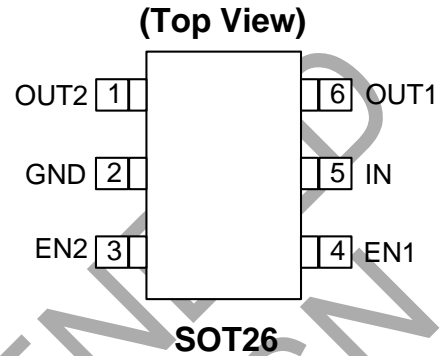
The characteristics of low dropout voltage and low quiescent current make it suitable for low power applications. The typical quiescent current is approximately 60µA.

This device is available with fixed output options of 1.2V/1.8V, 1.2V/3.3V, 1.5V/2.5V, 1.5V/3.3V, 1.8V/2.8V, 1.8V/3.0V, 1.8V/3.3V and 3.3V/3.3V.

For other output options please contact our local sales representative directly or through our distributor located in your area.

The AP7312 is available in SOT26 and DFN2018-6 packages.

### Pin Assignments



### Features

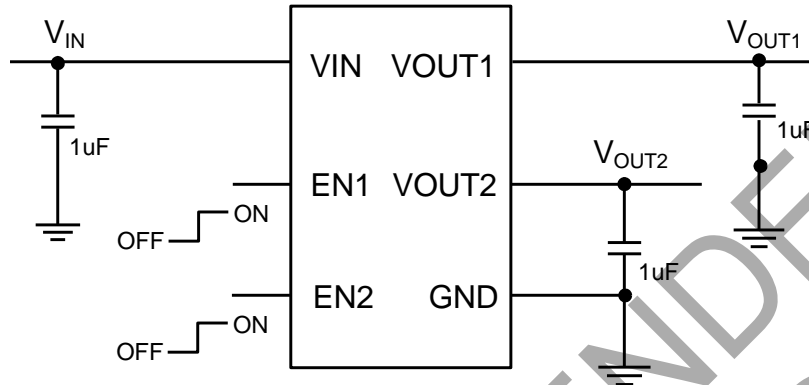
- 150mA Low Dropout Regulator with EN
- Very low IQ: 60µA
- Wide input voltage range: 2V to 6V
- Fixed output options: 1.2V to 3.3V
- High PSRR: 65dB at 1kHz
- Fast start-up time: 60µs
- Stable with low ESR, 1µF ceramic output capacitor
- Excellent Load/Line Transient Response
- Low dropout: 150mV at 150mA
- Current limit protection
- Short circuit protection
- Thermal shutdown protection
- Ambient temperature range: -40°C to 85°C
- SOT26 and DFN2018-6: Available in “Green” Molding Compound (No Br, Sb)
- Lead Free Finish/RoHS Compliant (Note 1)

### Applications

- Cellular Phones
- Smart Phones, PDAs
- MP3/MP4
- Bluetooth head set
- Low power application

Note: 1. EU Directive 2002/95/EC (RoHS). All applicable RoHS exemptions applied. Please visit our website at [http://www.diodes.com/products/lead\\_free.html](http://www.diodes.com/products/lead_free.html).

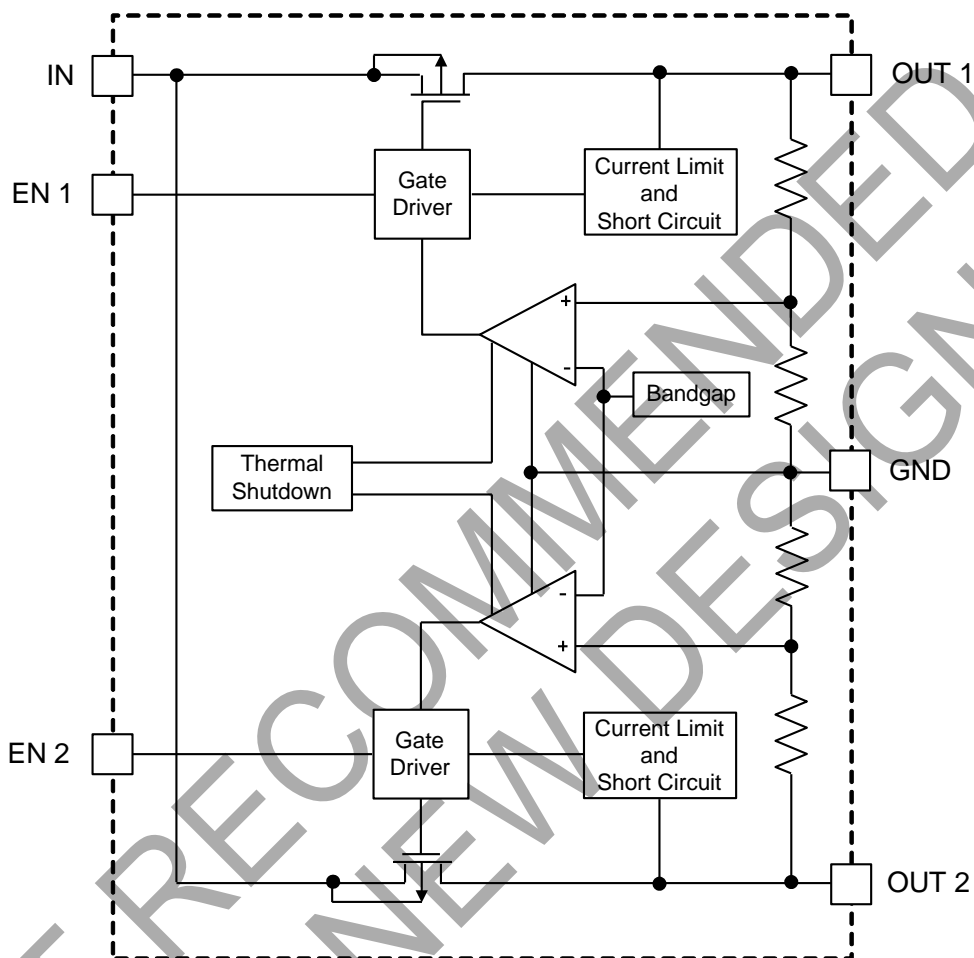
**Typical Application Circuit**



**Pin Descriptions**

Pin Name	Pin Number		Description
	SOT26	DFN2018-6	
OUT2	1	5	Voltage output 2. Bypass to ground through 1µF ceramic capacitor
GND	2	4	Ground
EN2	3	3	Enable input 2, active high
EN1	4	2	Enable input 1, active high
IN	5	1	Voltage input. Bypass to ground through at least 1µF capacitor
OUT1	6	6	Voltage output 1. Bypass to ground through 1µF ceramic capacitor

**Functional Block Diagram**



## DUAL 150mA LOW QUIESCENT CURRENT FAST TRANSIENT LOW DROPOUT LINEAR REGULATOR

### Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit	
ESD HBM	Human Body Model ESD Protection	8	kV	
ESD MM	Machine Model ESD Protection	400	V	
$V_{IN}$	Input Voltage	6.5	V	
	OUT, EN Voltage	$V_{IN} + 0.3$	V	
	Continuous Load Current	Internal Limited		
$T_{OP}$	Operating Junction Temperature Range	-40 ~ 125	°C	
$T_{ST}$	Storage Temperature Range	-65 ~ 150	°C	
$P_D$	Power Dissipation (Note 3)	SOT26	950	mW
		DFN2018-6	2200	mW
$T_J$	Maximum Junction Temperature	150	°C	

### Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
$V_{IN}$	Input voltage	2	6	V
$I_{OUT}$	Output Current (Note 3)	0	150	mA
$T_A$	Operating Ambient Temperature	-40	85	°C

Notes: 2. Ratings apply to ambient temperature at 25°C.  
3. The device maintains a stable, regulated output voltage without a load current.

## DUAL 150mA LOW QUIESCENT CURRENT FAST TRANSIENT LOW DROPOUT LINEAR REGULATOR

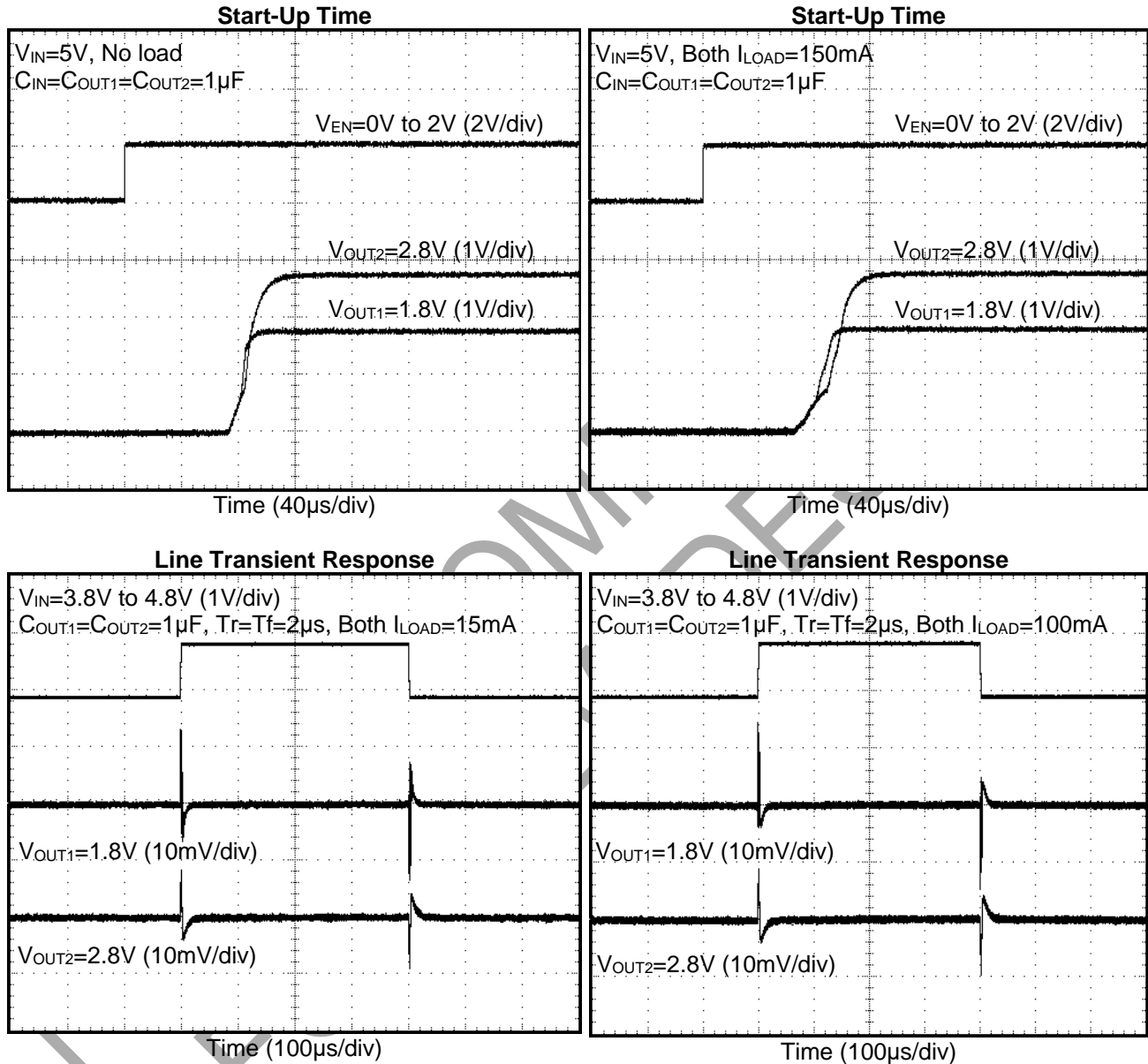
### Electrical Characteristics

( $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT} + 1\text{V}$ ,  $C_{IN} = 1\mu\text{F}$ ,  $C_{OUT} = 1\mu\text{F}$ ,  $V_{EN} = V_{IN}$ , unless otherwise stated)

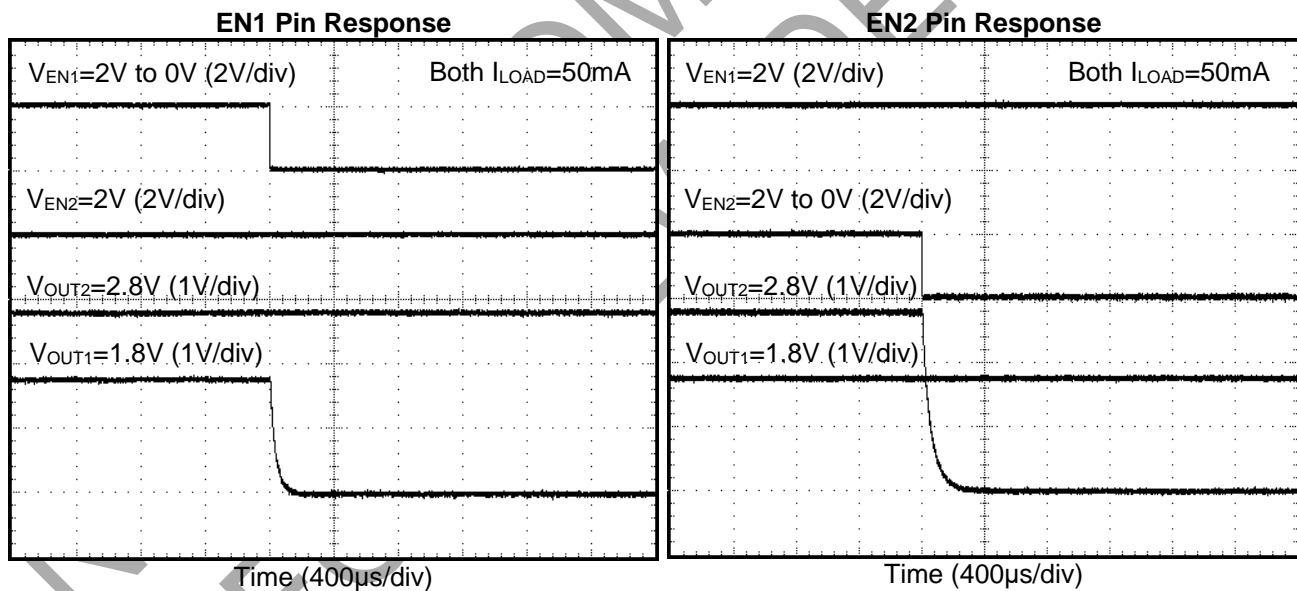
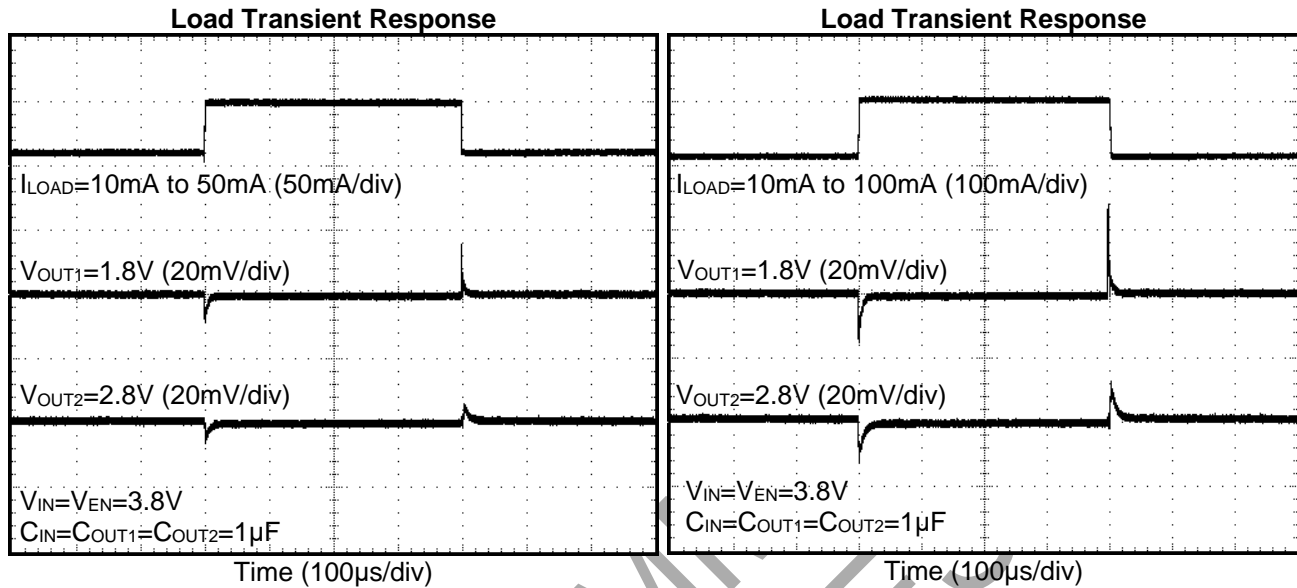
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{REF}$	ADJ Reference Voltage (Adjustable version)	$I_{OUT} = 0\text{mA}$		0.8		V
$I_{ADJ}$	ADJ Leakage (Adjustable version)			0.1	1	$\mu\text{A}$
$V_{OUT}$	Output Voltage Accuracy	$T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $I_{OUT} = 10\%$ of $I_{OUT-Max}$	-2		2	%
$\Delta V_{OUT} / \Delta V_{IN} / V$	Line Regulation	$V_{IN} = (V_{OUT} + 1\text{V})$ to $V_{IN-Max}$ , $V_{EN} = V_{IN}$ , $I_{OUT} = 1\text{mA}$		0.01	0.20	%/V
$\Delta V_{OUT} / I_{OUT}$	Load Regulation	$V_{IN} = (V_{OUT} + 1\text{V})$ to $V_{IN-Max}$ , $I_{OUT} = 1\text{mA}$ to $150\text{mA}$	-0.6		0.6	%
$V_{Dropout}$	Dropout Voltage (Note 4)	$V_{OUT} < 2.5\text{V}$ , $I_{OUT} = 150\text{mA}$		200	300	mV
		$V_{OUT} \geq 2.5\text{V}$ , $I_{OUT} = 150\text{mA}$		150	200	
$I_Q$	Input Quiescent Current (2 channels)	$V_{EN} = V_{IN}$ , $I_{OUT} = 0\text{mA}$		60	80	$\mu\text{A}$
$I_{SHDN}$	Input Shutdown Current	$V_{EN} = 0\text{V}$ , $I_{OUT} = 0\text{mA}$		0.1	1	$\mu\text{A}$
$I_{LEAK}$	Input Leakage Current	$V_{EN} = 0\text{V}$ , OUT grounded		0.1	1	$\mu\text{A}$
$t_{ST}$	Start-up Time	$V_{EN} = 0\text{V}$ to $2.0\text{V}$ in $1\mu\text{s}$ , $I_{OUT} = 150\text{mA}$		150		$\mu\text{s}$
PSRR	PSRR (Note 5)	$V_{IN} = [V_{OUT} + 1\text{V}]_{V_{DC}} + 0.5\text{V}_{ppAC}$ , $f = 1\text{kHz}$ , $I_{OUT} = 50\text{mA}$	60	65		dB
$I_{SHORT}$	Short-circuit Current	$V_{IN} = V_{IN-Min}$ to $V_{IN-Max}$ , $V_{OUT} = 1/4$ target $V_{OUT}$		60		mA
$I_{LIMIT}$	Current limit	$V_{IN} = V_{IN-Min}$ to $V_{IN-Max}$ , $V_{OUT}/R_{OUT} = 0.6\text{A}$	200	300		mA
$V_{IL}$	EN Input Logic Low Voltage	$V_{IN} = V_{IN-Min}$ to $V_{IN-Max}$			0.4	V
$V_{IH}$	EN Input Logic High Voltage	$V_{IN} = V_{IN-Min}$ to $V_{IN-Max}$	1.4			V
$I_{EN}$	EN Input Current	$V_{IN} = 0\text{V}$ or $V_{IN-Max}$	-1		1	$\mu\text{A}$
$T_{SHDN}$	Thermal shutdown threshold			165		$^\circ\text{C}$
$T_{HYS}$	Thermal shutdown hysteresis			30		$^\circ\text{C}$
$\theta_{JA}$	Thermal Resistance Junction-to-Ambient	SOT26 (Note 6)		140		$^\circ\text{C}/\text{W}$
		DFN2018-6 (Note 7)		60		

- Notes:
- Dropout voltage is the voltage difference between the input and the output at which the output voltage drops 2% below its nominal value.
  - This specification is guaranteed by design.
  - Test condition for SOT26: Device mounted on FR-4 substrate PC board, with minimum recommended pad layout
  - Test condition for DFN2018-6: Device mounted on FR-4 2-layer board, 2oz copper, with minimum recommended pad on top layer and 3 vias to bottom layer.

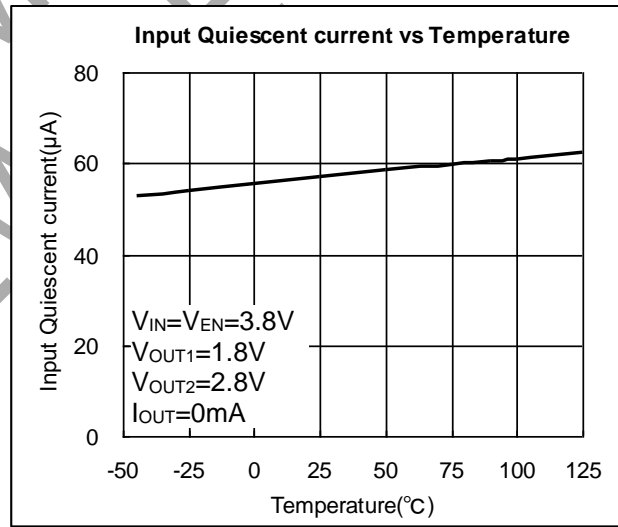
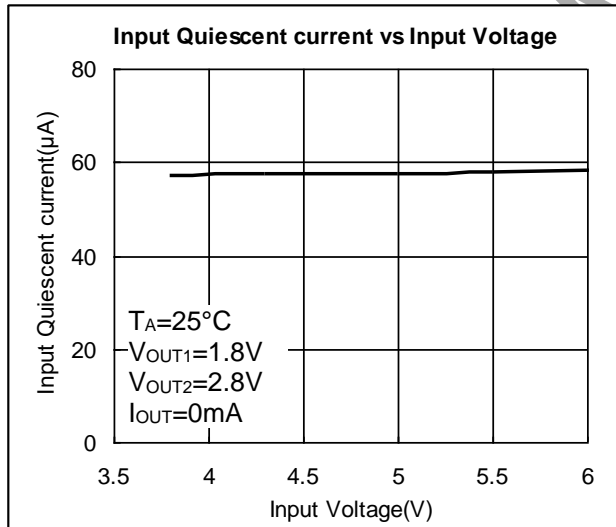
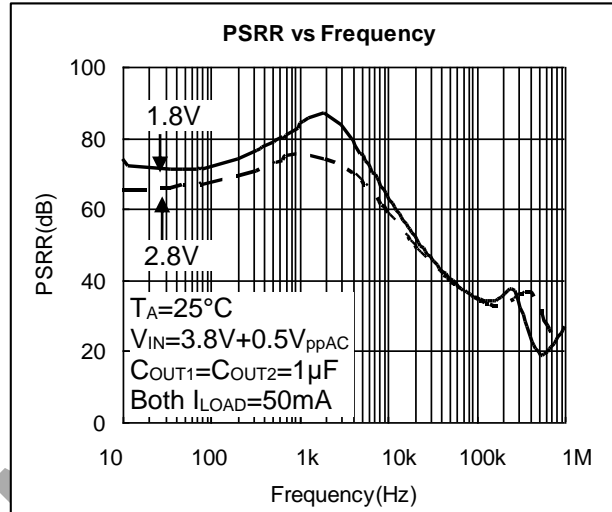
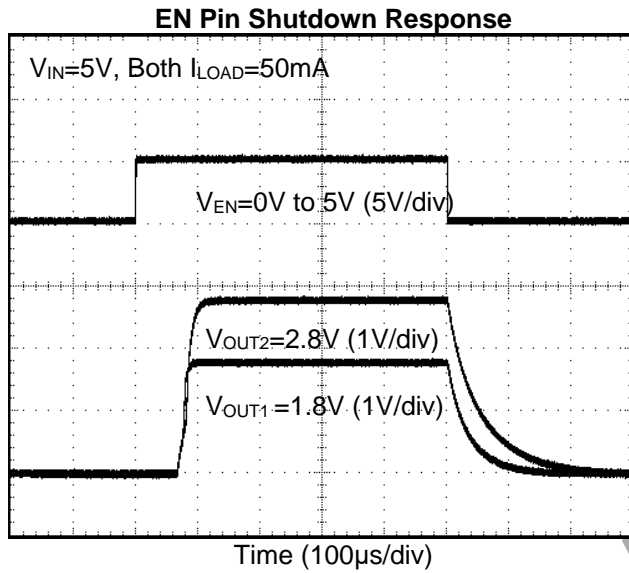
**Typical Performance Characteristics**



**Typical Performance Characteristics (Continued)**

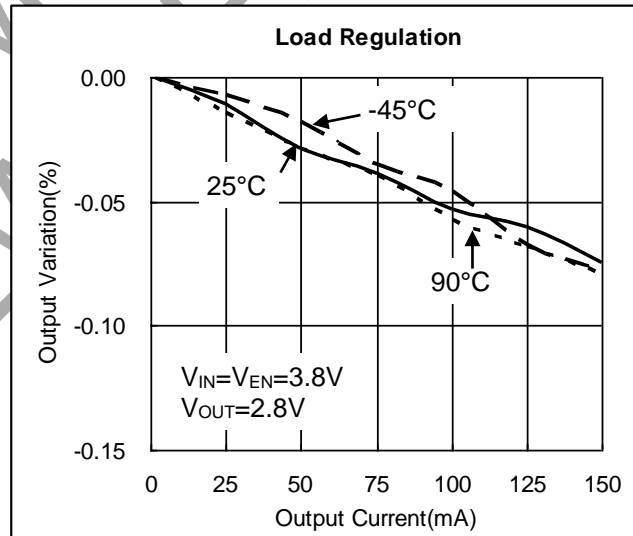
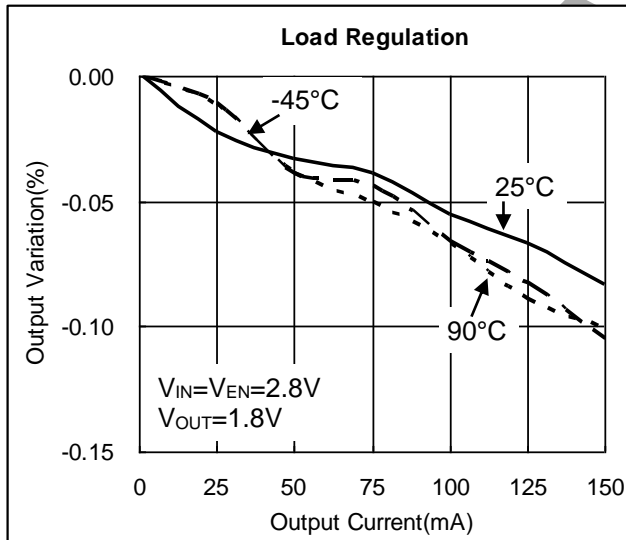
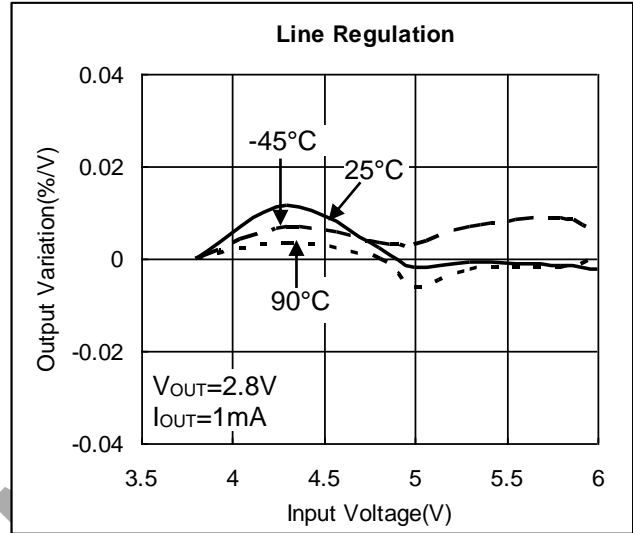
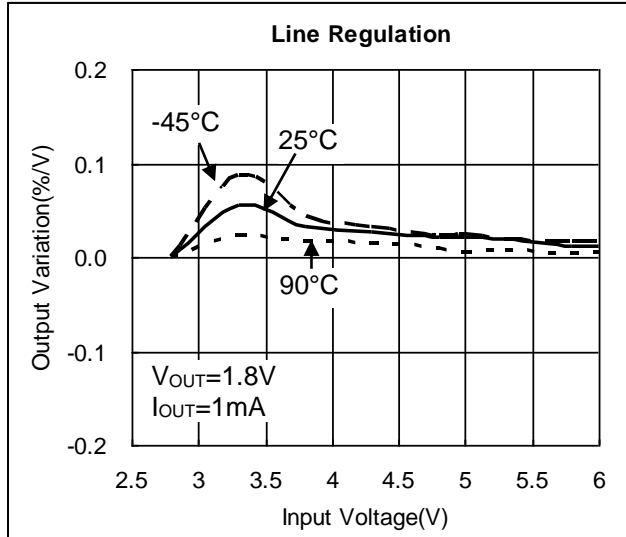


**Typical Performance Characteristics (Continued)**

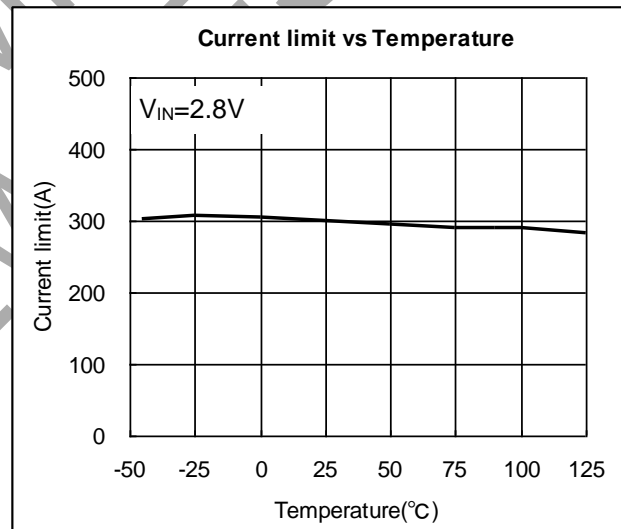
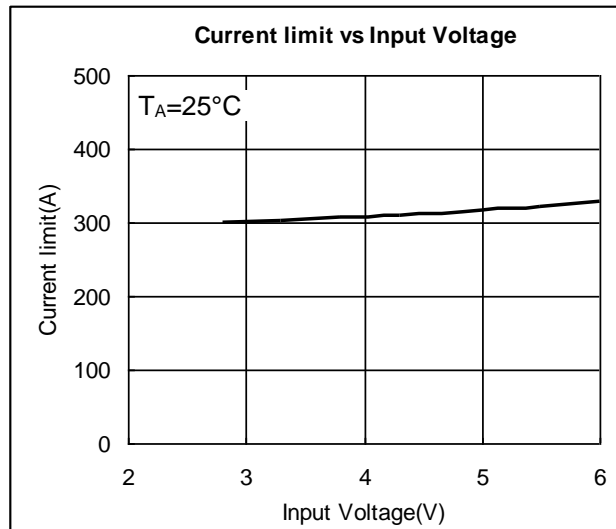
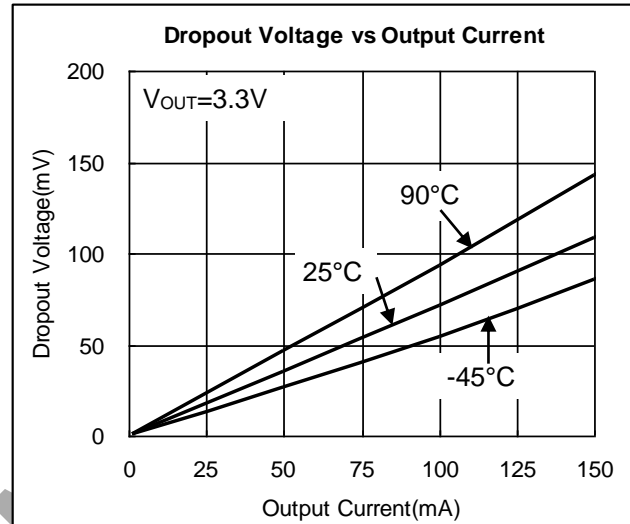
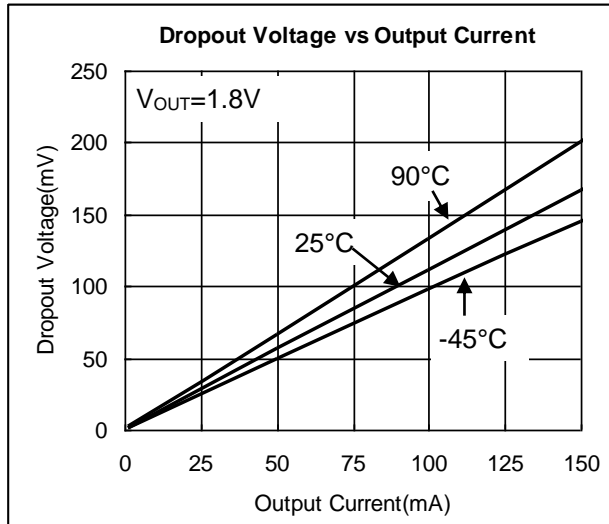




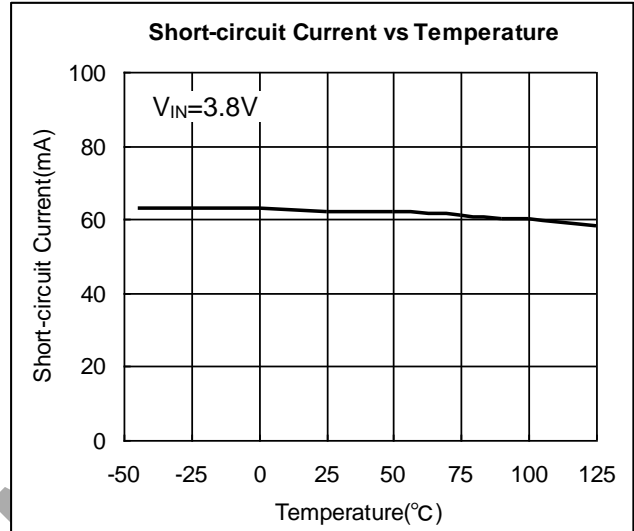
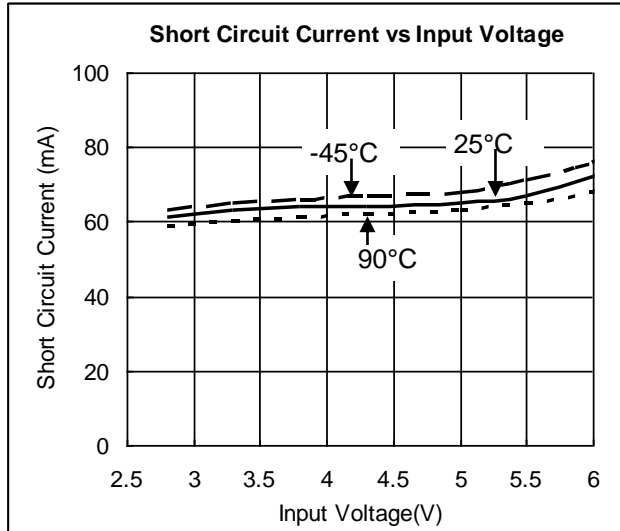
**Typical Performance Characteristics (Continued)**



**Typical Performance Characteristics (Continued)**



**Typical Performance Characteristics (Continued)**



NOT RECOMMENDED FOR NEW DESIGNS

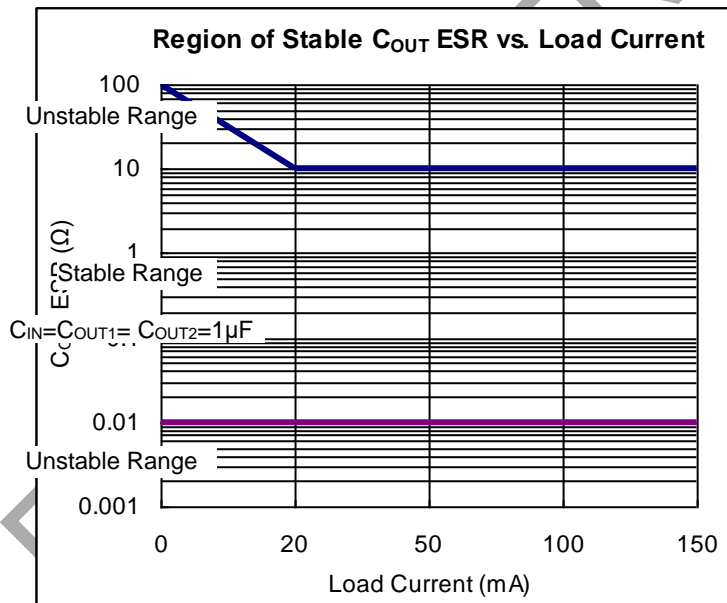
**Application Note**

**Input Capacitor**

A 1µF ceramic capacitor is recommended between IN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and reduce noise. For PCB layout, a wide copper trace is required for both IN and GND pins. A lower ESR capacitor type allows the use of less capacitance, while higher ESR type requires more capacitance.

**Output Capacitor**

The output capacitor is required to stabilize and improve the transient response of the LDO. The AP7312 is stable with very small ceramic output capacitors. Using a ceramic capacitor value that is at least 1µF with  $ESR \geq 10m\Omega$  on the output ensures stability. Higher capacitance values help to improve line and load transient response. The output capacitance may be increased to keep low undershoot and overshoot. Output capacitor must be placed as close as possible to OUT and GND pins.



**No Load Stability**

Other than external resistor divider, no minimum load is required to keep the device stable. The device will remain stable and regulated in no load condition.

**ON/OFF Input Operation**

The AP7312 is turned on by setting the EN pin high, and is turned off by pulling it low. If this feature is not used, the EN pin should be tied to IN pin to keep the regulator output on at all time. To ensure proper operation, the signal source used to drive the EN pin must be able to swing above and below the specified turn-on/off voltage thresholds listed in the Electrical Characteristics section under  $V_{IL}$  and  $V_{IH}$ .

---

**Application Note (Continued)**

---

**Current Limit Protection**

When output current at OUT pin is higher than current limit threshold, the current limit protection will be triggered and clamp the output current to approximately 300mA to prevent over-current and to protect the regulator from damage due to overheating.

**Short Circuit Protection**

When OUT pin is short-circuit to GND, short circuit protection will be triggered and clamp the output current to approximately 60mA. This feature protects the regulator from over-current and damage due to overheating.

**Thermal Shutdown Protection**

Thermal protection disables the output when the junction temperature rises to approximately +165°C, allowing the device to cool down. When the junction temperature reduces to approximately +135°C the output circuitry is enabled again. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the heat dissipation of the regulator, protecting it from damage due to overheating.

**Ultra Fast Start-up**

After enabled, the AP7312 is able to provide full power in as little as tens of microseconds, typically 150µs, without sacrificing low ground current. This feature will help load circuitry move in and out of standby mode in real time, eventually extend battery life for mobile phones and other portable devices.

**Fast Transient Response**

Fast transient response LDO can extend battery life. TDMA-based cell phone protocols such as Global System for Mobile Communications (GSM) have a transmit/receive duty factor of only 12.5 percent, enabling power savings by putting much of the baseband circuitry into standby mode in between transmit cycles. In baseband circuits, the load often transitions virtually instantaneously from 100µA to 100mA. To meet this load requirement, the LDO must react very quickly without a large voltage drop or overshoot — a requirement that cannot be met with conventional, general-purpose LDO.

The AP7312's fast transient response from 0 to 150mA provides stable voltage supply for fast DSP and GSM chipset with fast changing load.

**Low Quiescent Current**

The AP7312, consuming only around 60µA for all input range, provides great power saving in portable and low power applications.

**Power Dissipation**

The device power dissipation and proper sizing of the thermal plane that is connected to the thermal pad is critical to avoid thermal shutdown and ensure reliable operation. Power dissipation of the device depends on input voltage and load conditions and can be calculated by:

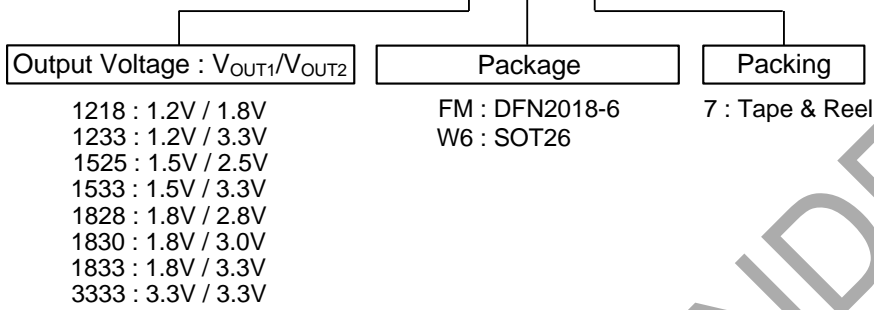
$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

The maximum power dissipation, handled by the device, depends on the maximum junction to ambient thermal resistance, maximum ambient temperature, and maximum device junction temperature, which can be calculated by the equation in the following:

$$P_D (\text{max}@T_A) = \frac{(+150^\circ\text{C} - T_A)}{R_{\theta JA}}$$

**Ordering Information**

**AP7312- XXYY XX - 7**



Device	Package Code	Packaging (Note 8)	7" Tape and Reel	
			Quantity	Part Number Suffix
AP7312-XXYY W6-7	W6	SOT26	3000/Tape & Reel	-7
AP7312-XXYY FM-7	FM	DFN2018-6	3000/Tape & Reel	-7

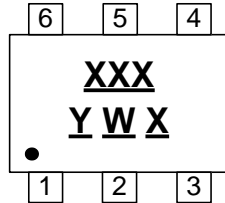
Note: 8. Pad layout as shown on Diodes Inc. suggested pad layout document AP02001, which can be found on our website at <http://www.diodes.com/datasheets/ap02001.pdf>.

NOT RECOMMENDED FOR NEW DESIGN

**Marking Information**

**(1) SOT26**

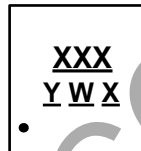
**( Top View )**



XXX : Identification code  
Y : Year 0~9  
W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents 52 and 53 week  
X : A~Z : Internal Code

**(2) DFN2018-6**

**( Top View )**

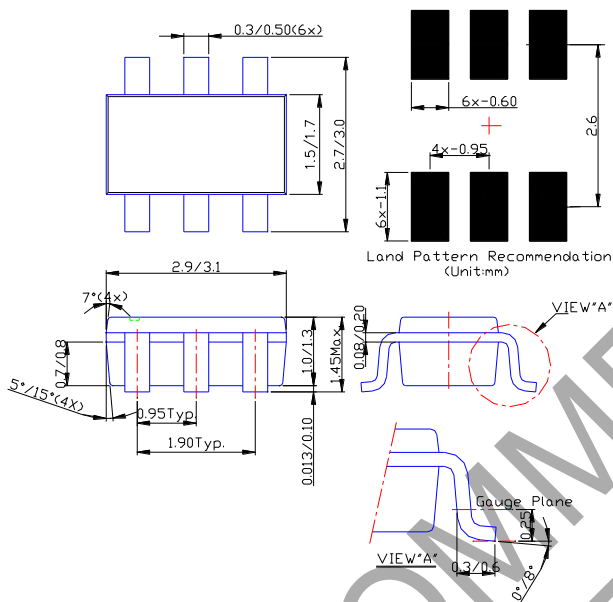


XXX : Identification code  
Y : Year : 0~9  
W : Week : A~Z : 1~26 week;  
a~z : 27~52 week; z represents 52 and 53 week  
X : A~Z : Internal Code

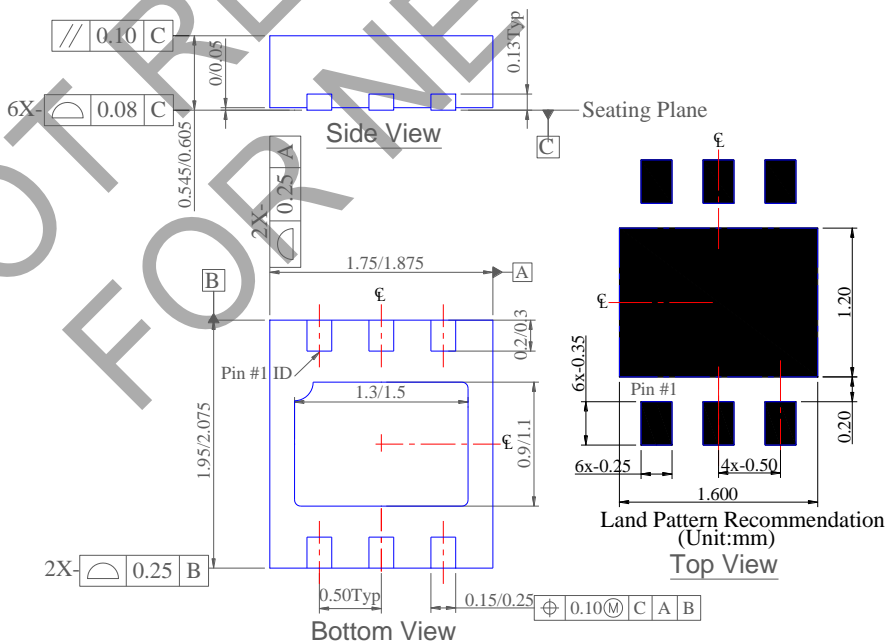
Device	Package	Package	Identification Code
AP7312-1218	SOT26	DFN2018-6	CAS
AP7312-1233	SOT26	DFN2018-6	CAZ
AP7312-1525	SOT26	DFN2018-6	CA6
AP7312-1533	SOT26	DFN2018-6	CBC
AP7312-1828	SOT26	DFN2018-6	CBK
AP7312-1830	SOT26	DFN2018-6	CBN
AP7312-1833	SOT26	DFN2018-6	CBR
AP7312-3333	SOT26	DFN2018-6	CEA

**Package Outline Dimensions (All Dimensions in mm)**

**(1) SOT26**



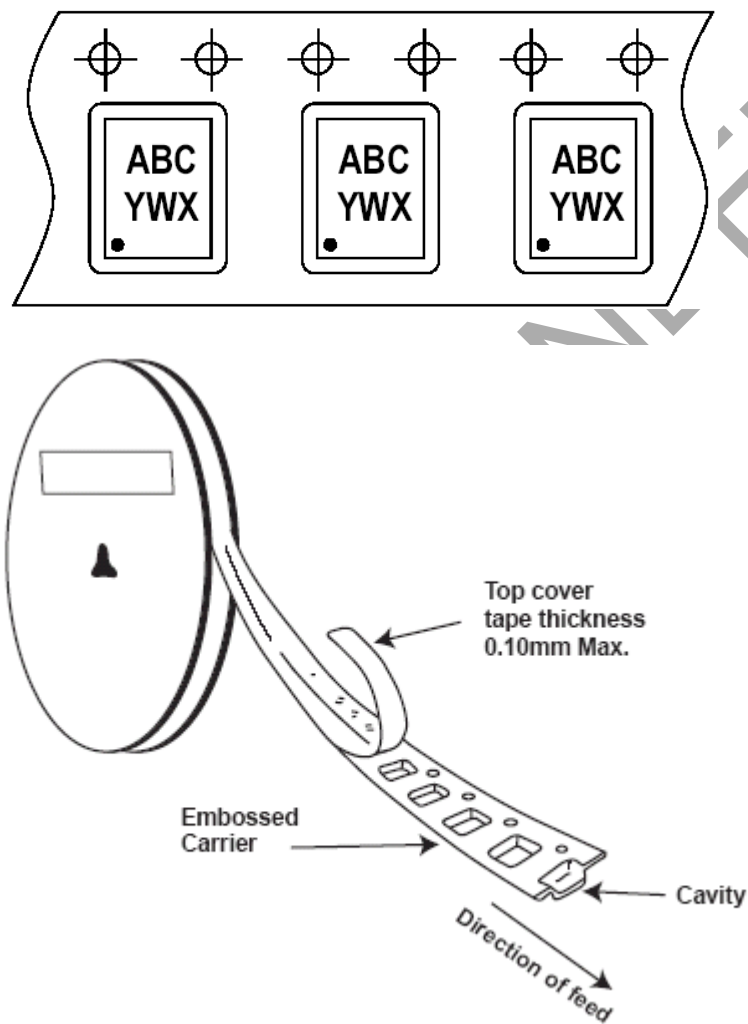
**(2) DFN2018-6**





**Taping Orientation (Note 9)**

For DFN2018-6



Note: 9. The taping orientation of the other package type can be found on our website at <http://www.diodes.com/datasheets/ap02007.pdf>

**DUAL 150mA LOW QUIESCENT CURRENT FAST  
TRANSIENT LOW DROPOUT LINEAR REGULATOR****IMPORTANT NOTICE**

1. DIODES INCORPORATED (Diodes) AND ITS SUBSIDIARIES MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO ANY INFORMATION CONTAINED IN THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).
2. The Information contained herein is for informational purpose only and is provided only to illustrate the operation of Diodes' products described herein and application examples. Diodes does not assume any liability arising out of the application or use of this document or any product described herein. This document is intended for skilled and technically trained engineering customers and users who design with Diodes' products. Diodes' products may be used to facilitate safety-related applications; however, in all instances customers and users are responsible for (a) selecting the appropriate Diodes products for their applications, (b) evaluating the suitability of Diodes' products for their intended applications, (c) ensuring their applications, which incorporate Diodes' products, comply the applicable legal and regulatory requirements as well as safety and functional-safety related standards, and (d) ensuring they design with appropriate safeguards (including testing, validation, quality control techniques, redundancy, malfunction prevention, and appropriate treatment for aging degradation) to minimize the risks associated with their applications.
3. Diodes assumes no liability for any application-related information, support, assistance or feedback that may be provided by Diodes from time to time. Any customer or user of this document or products described herein will assume all risks and liabilities associated with such use, and will hold Diodes and all companies whose products are represented herein or on Diodes' websites, harmless against all damages and liabilities.
4. Products described herein may be covered by one or more United States, international or foreign patents and pending patent applications. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks and trademark applications. Diodes does not convey any license under any of its intellectual property rights or the rights of any third parties (including third parties whose products and services may be described in this document or on Diodes' website) under this document.
5. Diodes' products are provided subject to Diodes' Standard Terms and Conditions of Sale (<https://www.diodes.com/about/company/terms-and-conditions/terms-and-conditions-of-sales/>) or other applicable terms. This document does not alter or expand the applicable warranties provided by Diodes. Diodes does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.
6. Diodes' products and technology may not be used for or incorporated into any products or systems whose manufacture, use or sale is prohibited under any applicable laws and regulations. Should customers or users use Diodes' products in contravention of any applicable laws or regulations, or for any unintended or unauthorized application, customers and users will (a) be solely responsible for any damages, losses or penalties arising in connection therewith or as a result thereof, and (b) indemnify and hold Diodes and its representatives and agents harmless against any and all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim relating to any noncompliance with the applicable laws and regulations, as well as any unintended or unauthorized application.
7. While efforts have been made to ensure the information contained in this document is accurate, complete and current, it may contain technical inaccuracies, omissions and typographical errors. Diodes does not warrant that information contained in this document is error-free and Diodes is under no obligation to update or otherwise correct this information. Notwithstanding the foregoing, Diodes reserves the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes.
8. Any unauthorized copying, modification, distribution, transmission, display or other use of this document (or any portion hereof) is prohibited. Diodes assumes no responsibility for any losses incurred by the customers or users or any third parties arising from any such unauthorized use.
9. This Notice may be periodically updated with the most recent version available at <https://www.diodes.com/about/company/terms-and-conditions/important-notice>

The Diodes logo is a registered trademark of Diodes Incorporated in the United States and other countries.  
All other trademarks are the property of their respective owners.  
© 2024 Diodes Incorporated. All Rights Reserved.

[www.diodes.com](http://www.diodes.com)