



2N7002BKV

60 V, 340 mA dual N-channel Trench MOSFET

17 October 2024

Product data sheet

1. General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in an ultra small SOT666 Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Logic-level compatible
- Very fast switching
- Trench MOSFET technology
- ESD protection up to 2 kV

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

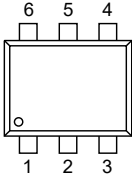
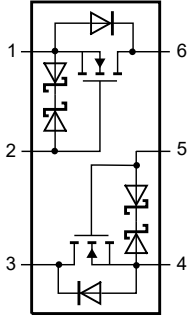
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
V_{DS}	drain-source voltage	$T_{amb} = 25\text{ °C}$		-	-	60	V
V_{GS}	gate-source voltage			-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-	340	mA
Static characteristics (per transistor)							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 500\text{ mA}; \text{pulsed}; t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.01; T_j = 25\text{ °C}$		-	1	1.6	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>SOT666</p>	 <p>017aaa055</p>
2	G1	gate1		
3	D2	drain2		
4	S2	source2		
5	G2	gate2		
6	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
2N7002BKV	SOT666	plastic, surface-mounted package; 6 leads; 0.5 mm pitch; 1.6 mm x 1.2 mm x 0.55 mm body	SOT666

7. Marking

Table 4. Marking codes

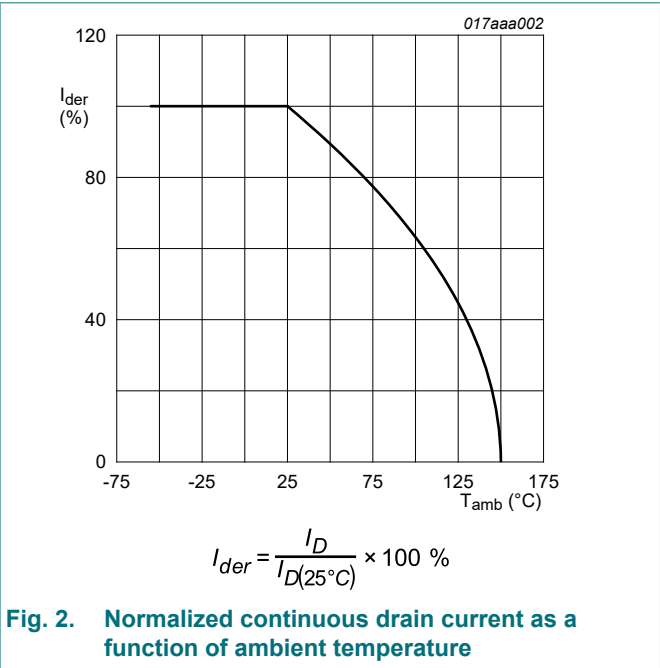
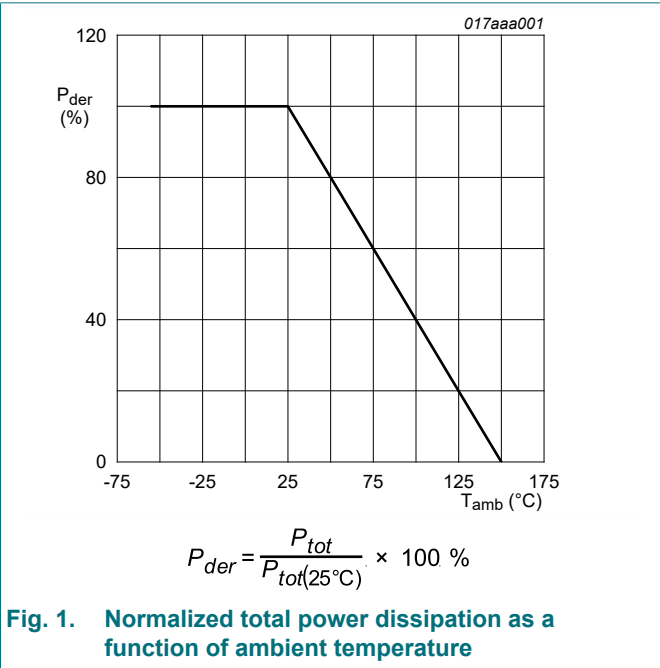
Type number	Marking code
2N7002BKV	ZG

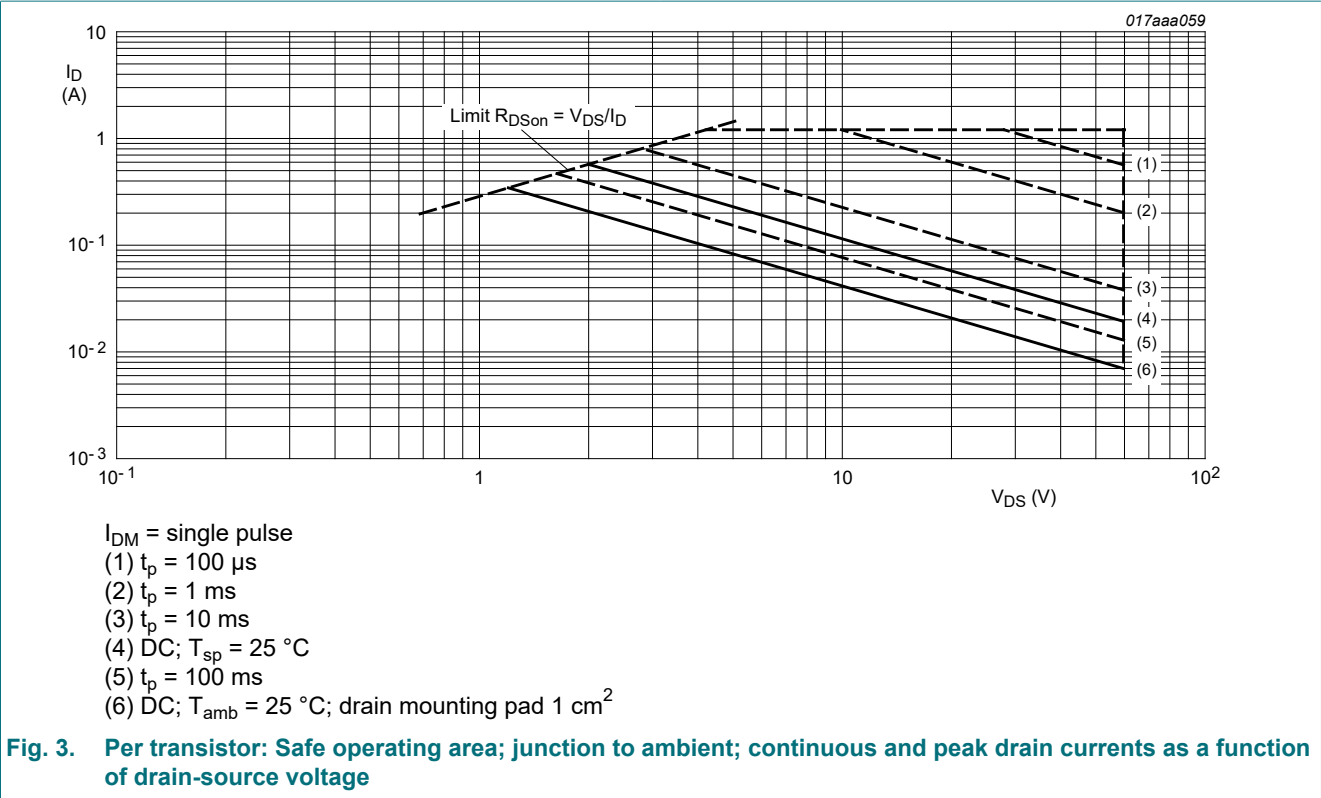
8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor						
V _{DS}	drain-source voltage	T _{amb} = 25 °C		-	60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	340	mA
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	240	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	1.2	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	350	mW
			[1]	-	410	mW
		T _{sp} = 25 °C		-	1140	mW
Per device						
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	525	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	340	mA
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[3]	-	2	kV

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².
[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
[3] Measured between all pins.



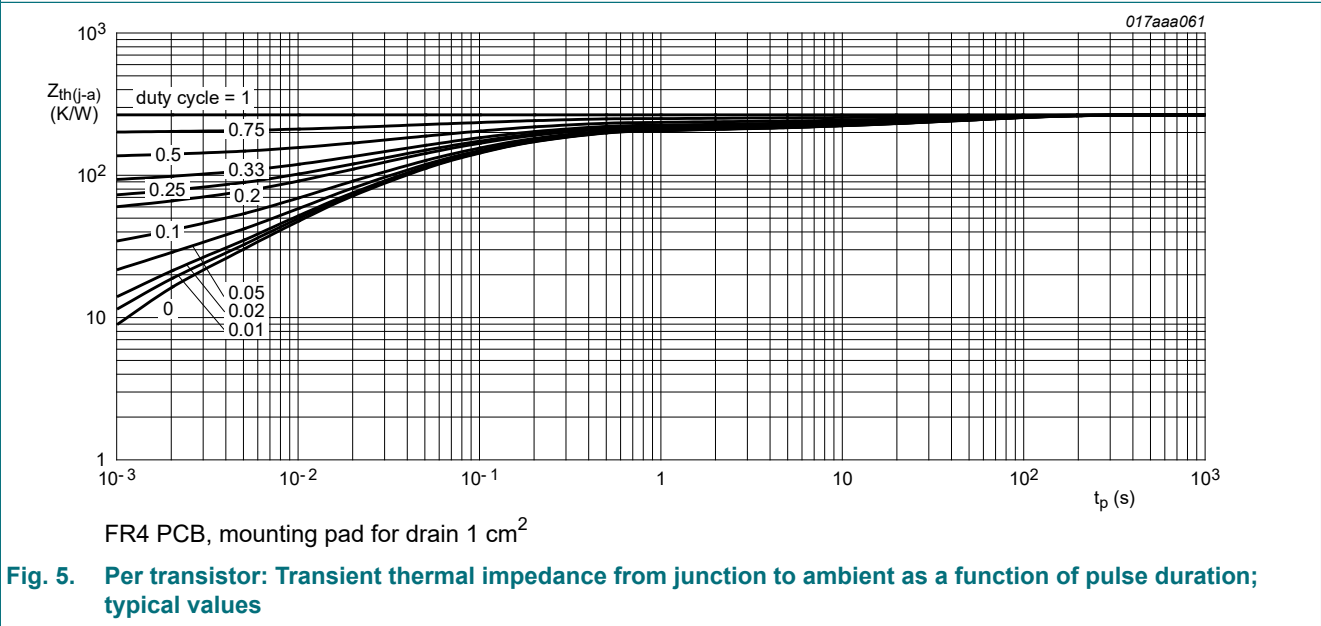
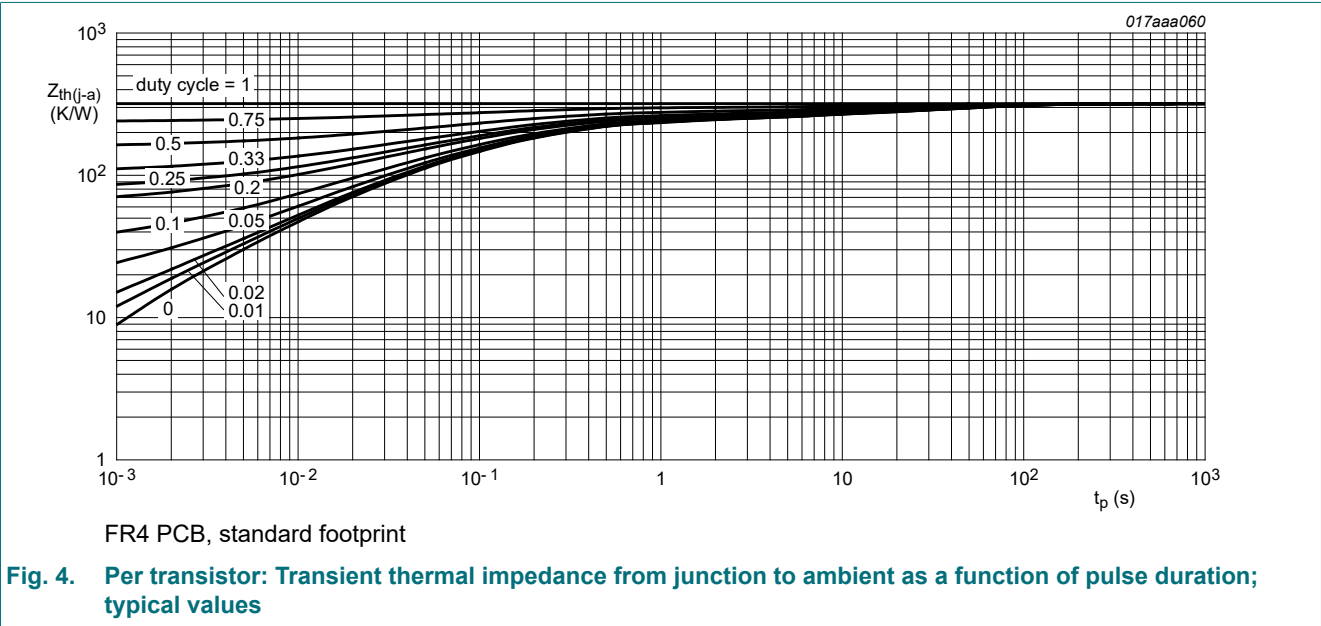


9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	240	K/W
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	315	360	K/W
			[2]	-	265	305	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	110	K/W

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm².



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics (per transistor)							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 10 μA; V _{GS} = 0 V; T _j = 25 °C		60	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = 250 μA; V _{DS} = V _{GS} ; T _j = 25 °C		1.1	1.6	2.1	V
I _{DSS}	drain leakage current	V _{DS} = 60 V; V _{GS} = 0 V; T _j = 25 °C		-	-	1	μA
		V _{DS} = 60 V; V _{GS} = 0 V; T _j = 150 °C		-	-	10	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	10	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 50 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.01; T _j = 25 °C		-	1.3	2	Ω
		V _{GS} = 10 V; I _D = 500 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.01; T _j = 25 °C		-	1	1.6	Ω
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 200 mA; pulsed; t _p ≤ 300 μs; δ ≤ 0.01; T _j = 25 °C		-	550	-	mS
Dynamic characteristics (per transistor)							
Q _{G(tot)}	total gate charge	V _{DS} = 30 V; I _D = 300 mA; V _{GS} = 4.5 V; T _j = 25 °C		-	0.5	0.6	nC
Q _{GS}	gate-source charge			-	0.2	-	nC
Q _{GD}	gate-drain charge			-	0.1	-	nC
C _{iss}	input capacitance	V _{DS} = 10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	33	50	pF
C _{oss}	output capacitance			-	7	-	pF
C _{rss}	reverse transfer capacitance			-	4	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 50 V; R _L = 250 Ω; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	5	10	ns
t _r	rise time			-	6	-	ns
t _{d(off)}	turn-off delay time			-	12	24	ns
t _f	fall time			-	7	-	ns
Source-drain diode (per transistor)							
V _{SD}	source-drain voltage	I _S = 115 mA; V _{GS} = 0 V; T _j = 25 °C		0.47	0.75	1.1	V

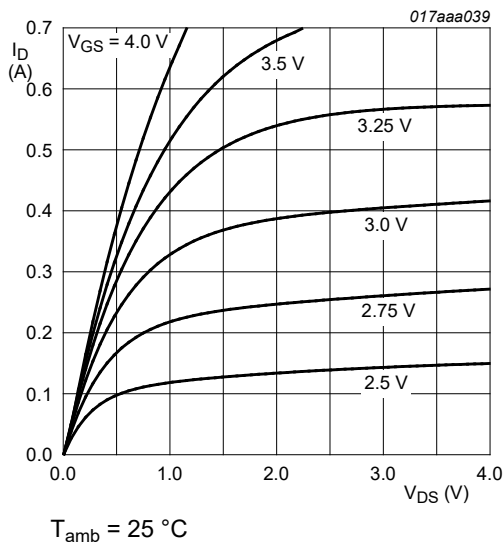


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

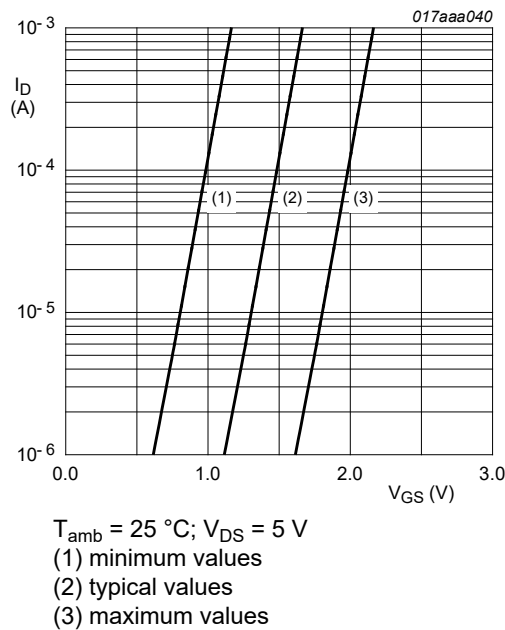


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

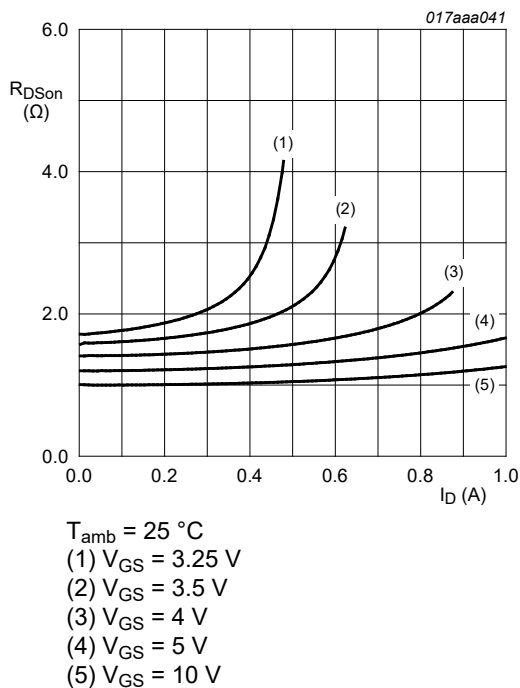


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

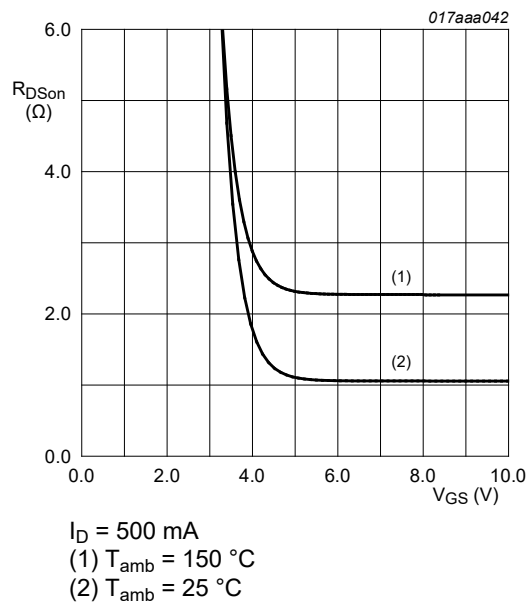


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

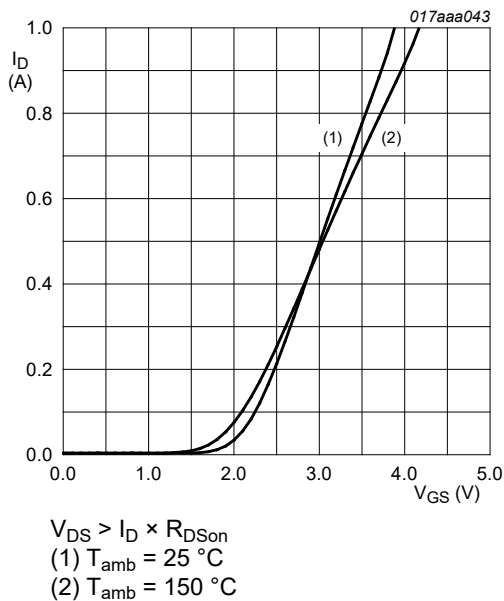


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

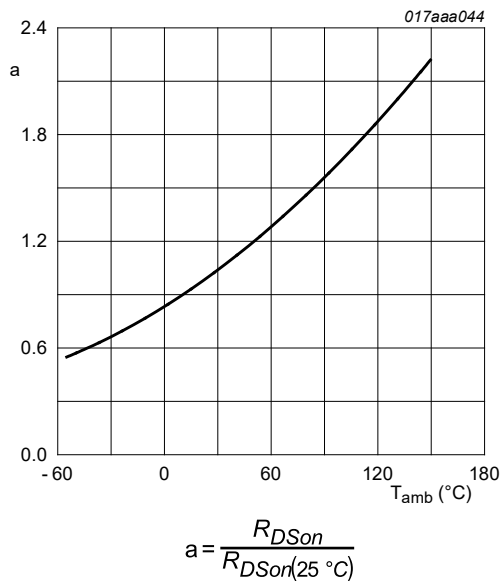


Fig. 11. Normalized drain-source on-state resistance as a function of ambient temperature; typical values

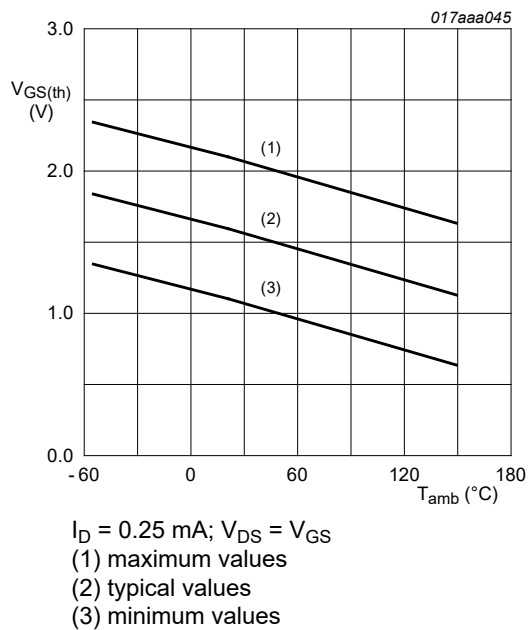


Fig. 12. Gate-source threshold voltage as a function of ambient temperature

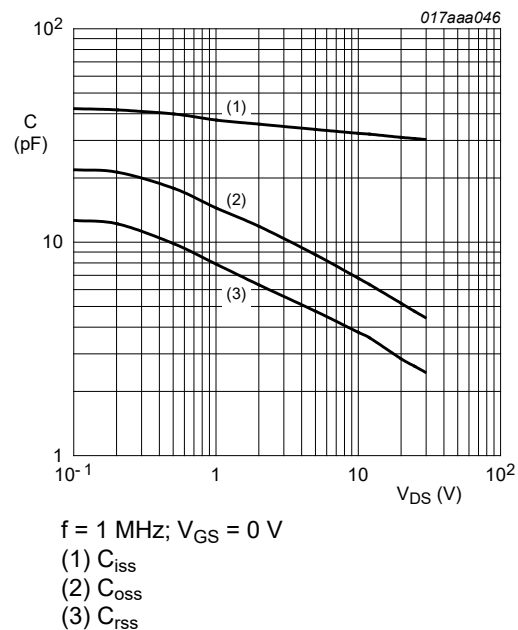


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

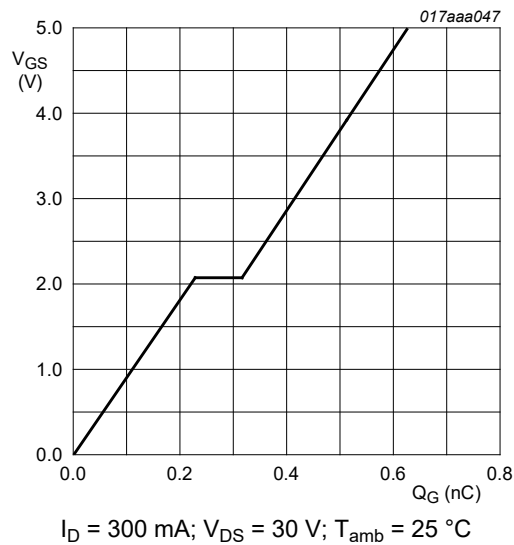


Fig. 14. Gate-source voltage as a function of gate charge; typical values

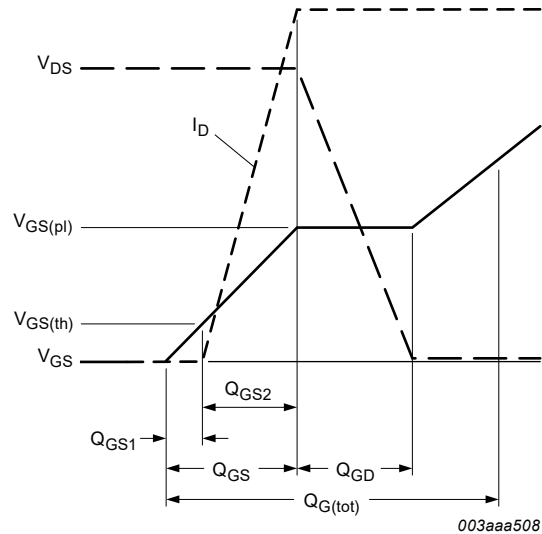


Fig. 15. Gate charge waveform definitions

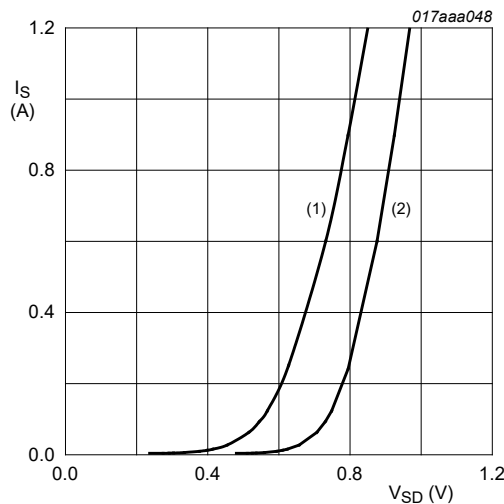


Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

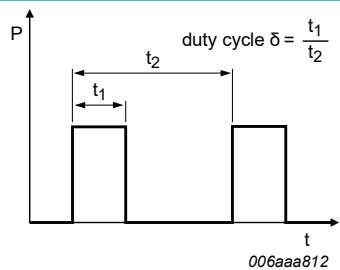


Fig. 17. Duty cycle definition

12. Package outline

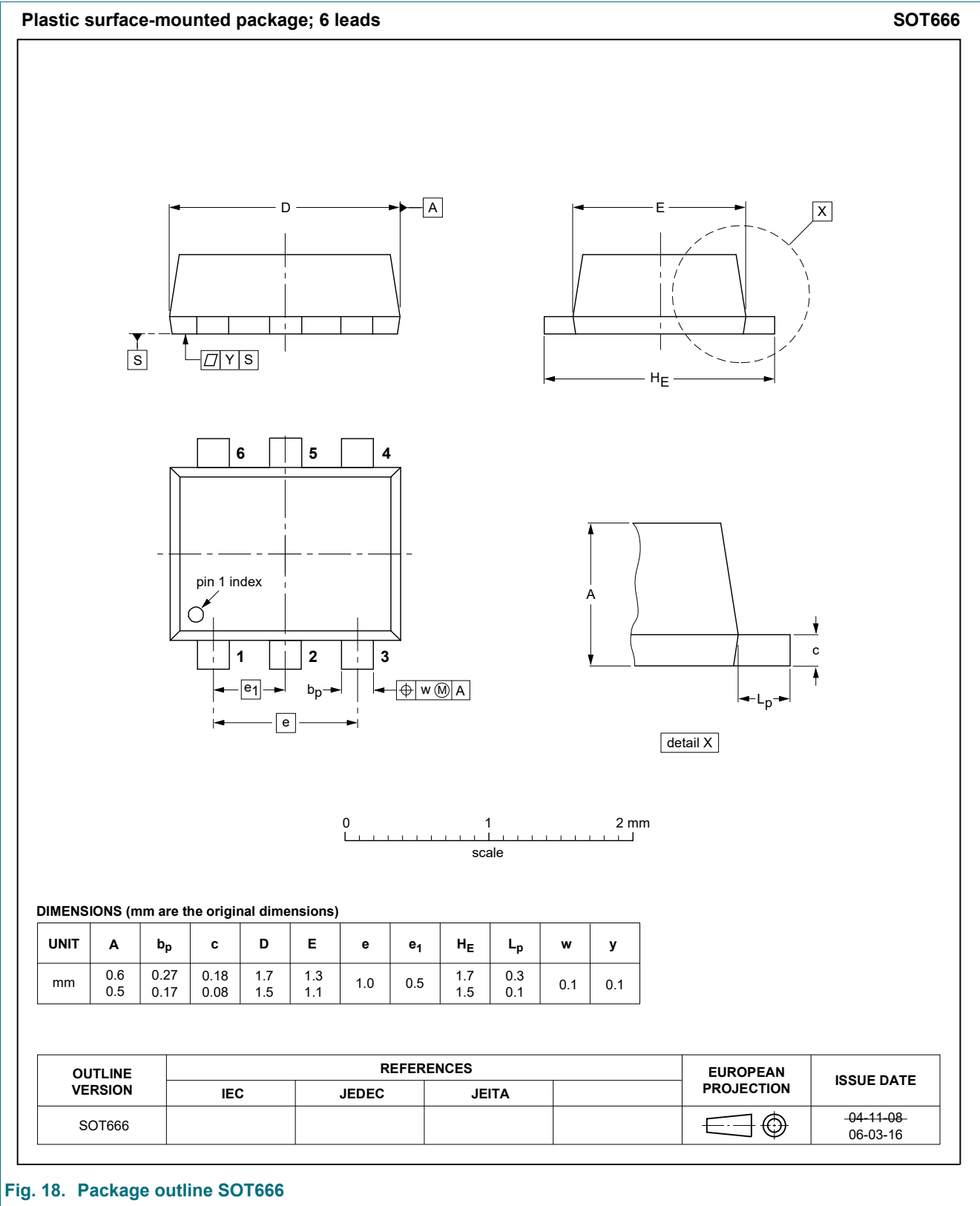


Fig. 18. Package outline SOT666

13. Soldering

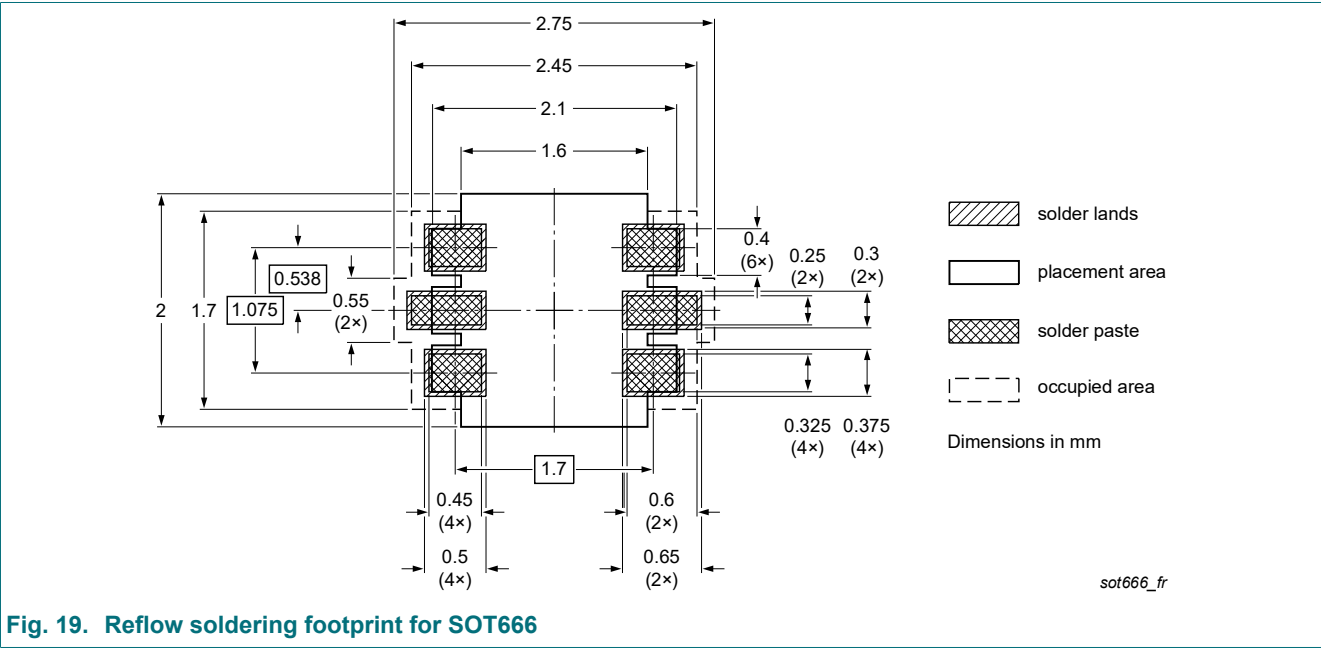


Fig. 19. Reflow soldering footprint for SOT666

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
2N7002BKV v.4	20241017	Product data sheet	-	2N7002BKV v.3
Modifications:	• Chapter "Characteristics": Conditions corrected for Fig. 14			
2N7002BKV v.3	20221228	Product data sheet	-	2N7002BKV v.2
2N7002BKV v.2	20100922	Product data sheet	-	2N7002BKV v.1
2N7002BKV v.1	20100610	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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