

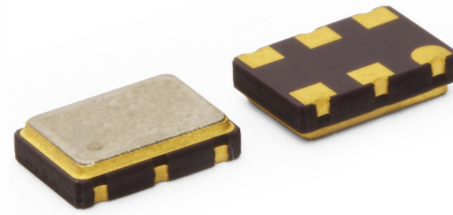


# Model 635

## Low Jitter LVPECL or LVDS Clock

### Features

- Ceramic Surface Mount Package
- Low Phase Jitter Performance, 700fs Maximum
- Fundamental or 3<sup>rd</sup> Overtone Crystal Design
- Frequency Range 10 – 320MHz \*
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-481



Part Dimensions:  
7.0 × 5.0 × 2.0mm • 178.462mg

### Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

#### Standard Frequencies

- 25.00MHz	- 125.00MHz	- 187.50MHz
- 50.00MHz	- 150.00MHz	- 200.00MHz
- 74.1758MHz	- 155.52MHz	- 212.50MHz
- 74.25MHz	- 156.25MHz	- 250.00MHz
- 100.00MHz	- 161.1328MHz	- 312.50MHz

\* See Page 9 for additional developed frequencies.  
Check with factory for availability of frequencies not listed.

### Description

CTS Model 635 is a low cost, high performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M635 has excellent stability and low jitter/phase noise performance.

### Ordering Information

Model	Output Type	Frequency Stability	Temperature Range	Supply Voltage	Frequency Code [MHz]
635	P	3	I	3	XXXMXXXX

Code	Output
P	LVPECL - Pin 1 Enable
L	LVDS - Pin 1 Enable
E	LVPECL - Pin 2 Enable
V	LVDS - Pin 2 Enable

Code	Temp. Range
A	-10°C to +60°C
C	-20°C to +70°C
I	-40°C to +85°C

Code	Frequency
Product Frequency Code <sup>2</sup>	

Code	Stability
6	±20ppm <sup>1</sup>
5	±25ppm
3	±50ppm
2	±100ppm

Code	Voltage
2	+2.5Vdc
3	+3.3Vdc

Notes:

- 1] Consult factory for availability of 6I Stability/Temperature combination.
- 2] Frequency is recorded with 3 significant digits before the 'M' and 4 significant digits after the 'M', including zeros. See Table I for frequency codes that exceed 4 significant digits.

**Not all performance combinations and frequencies may be available.  
Contact your local CTS Representative or CTS Customer Service for availability.**

Table I

Nominal Frequency [MHz]	Part Number Frequency Code
025.000625	025M0006
074.175824	074M175B
101.575694	101M5756
125.009375	125M0093
148.351648	148M351A
153.600770	153M6007
156.253906	156M2539
178.018970	178M0189

Example: P/N Frequency = Actual Frequency.  
148M351A = 148.351648MHz

This product is specified for use only in standard commercial applications. Supplier disclaims all express and implied warranties and liability in connection with any use of this product in any non-commercial applications or in any application that may expose the product to conditions that are outside of the tolerances provided in its specification.

## Electrical Specifications

### Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	$V_{CC}$	-	-0.5	-	5.0	V
Supply Voltage	$V_{CC}$	±5%	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current						
LVPECL	$I_{CC}$	Maximum Load	-	55	88	mA
LVDS			-	45	66	
Operating Temperature	$T_A$	-	-20 -40	+25	+70 +85	°C
Storage Temperature	$T_{STG}$	-	-40	-	+125	°C

### Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range						
LVPECL	$f_0$	-		10 - 320		MHz
LVDS				80 - 320		
Frequency Stability [Note 1]	$\Delta f/f_0$	-		20, 25, 50 or 100		±ppm
Aging	$\Delta f/f_{25}$	First Year @ +25°C, nominal $V_{CC}$	-3	-	3	ppm

1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

### Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	$R_L$	Terminated to $V_{CC} - 2.0V$	-	50	-	Ohms
Output Voltage Levels	$V_{OH}$	PECL Load, -20°C to +70°C	$V_{CC} - 1.025$	-	$V_{CC} - 0.880$	V
	$V_{OL}$		$V_{CC} - 1.810$	-	$V_{CC} - 1.620$	
	$V_{OH}$	PECL Load, -40°C to +85°C	$V_{CC} - 1.085$	-	$V_{CC} - 0.880$	V
	$V_{OL}$		$V_{CC} - 1.830$	-	$V_{CC} - 1.555$	
Output Duty Cycle	SYM	@ $V_{CC} - 1.3V$	45	-	55	%
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $R_L = 50$ Ohms	-	0.3	0.7	ns
Output Type	-	-		LVDS		-
Output Load	$R_L$	Between Outputs	-	100	-	Ohms
Output Voltage Levels	$V_{OH}$	LVDS Load	-	1.43	1.60	V
	$V_{OL}$		0.90	1.10	-	
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	$V_{OD}$	$R_L = 100$ Ohms	247	330	454	mV
Offset Voltage	$V_{OS}$	LVDS Load	1.125	1.25	1.375	V
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $R_L = 100$ Ohms	-	0.4	0.7	ns

## Electrical Specifications

### Output Parameters

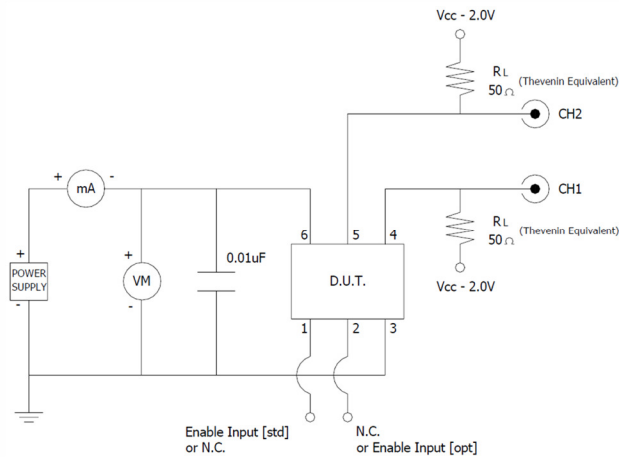
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Start Up Time	$T_S$	Application of $V_{CC}$	-	2	5	ms
<b>Enable Function [Standby]</b>						
Enable Input Voltage	$V_{IH}$	Pin 1 or 2 Logic '1', Output Enabled	$0.7V_{CC}$	-	-	V
Disable Input Voltage	$V_{IL}$	Pin 1 or 2 Logic '0', Output Disabled	-	-	$0.3V_{CC}$	V
Disable Time	$T_{PLZ}$	Pin 1 or 2 Logic '0', Output Disabled	-	-	200	ns
Enable Time	$T_{PLZ}$	Pin 1 or 2 Logic '1', Output Enabled	-	-	2	ms
Phase Jitter, RMS	$t_{jrms}$	Bandwidth 12 kHz - 20 MHz	-	300	700	fs
Period Jitter, RMS	$pj_{rms}$	-	-	2.6	-	ps
Period Jitter, pk-pk	$pj_{pk-pk}$	-	-	25	-	ps

### Enable Truth Table

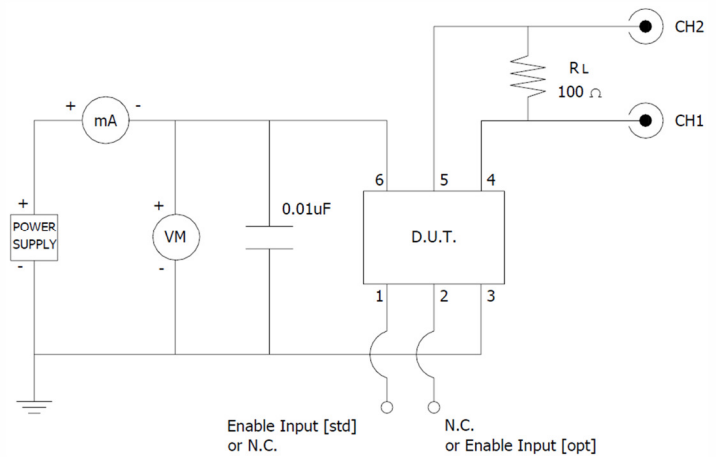
Pin 1 or Pin 2	Pin 4 & Pin 5
Logic '1'	Output Enabled
Open	Output Enabled
Logic '0'	Output Disabled, High Impedance

### Test Circuit

LVPECL

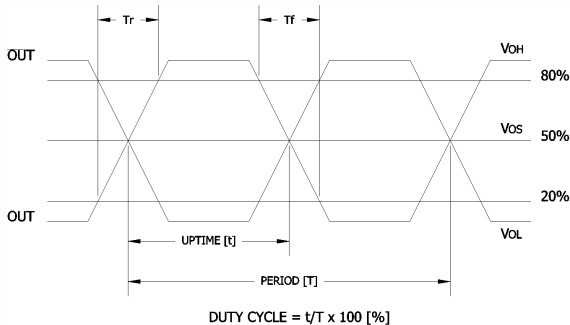


LVDS



### Output Waveform

LVPECL or LVDS

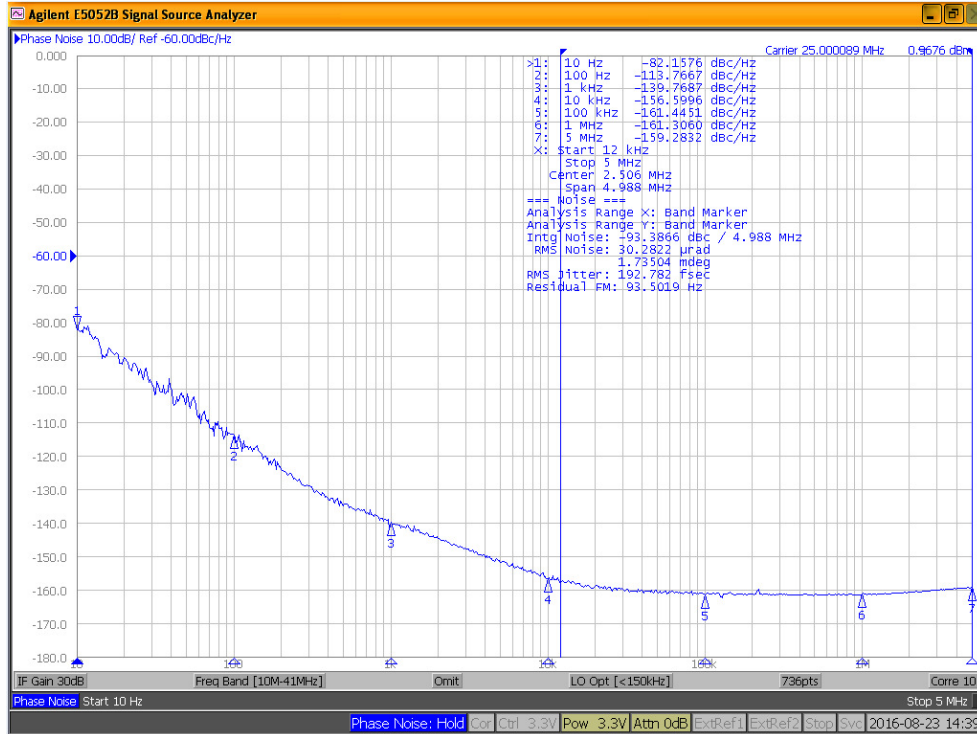


## Electrical Specifications

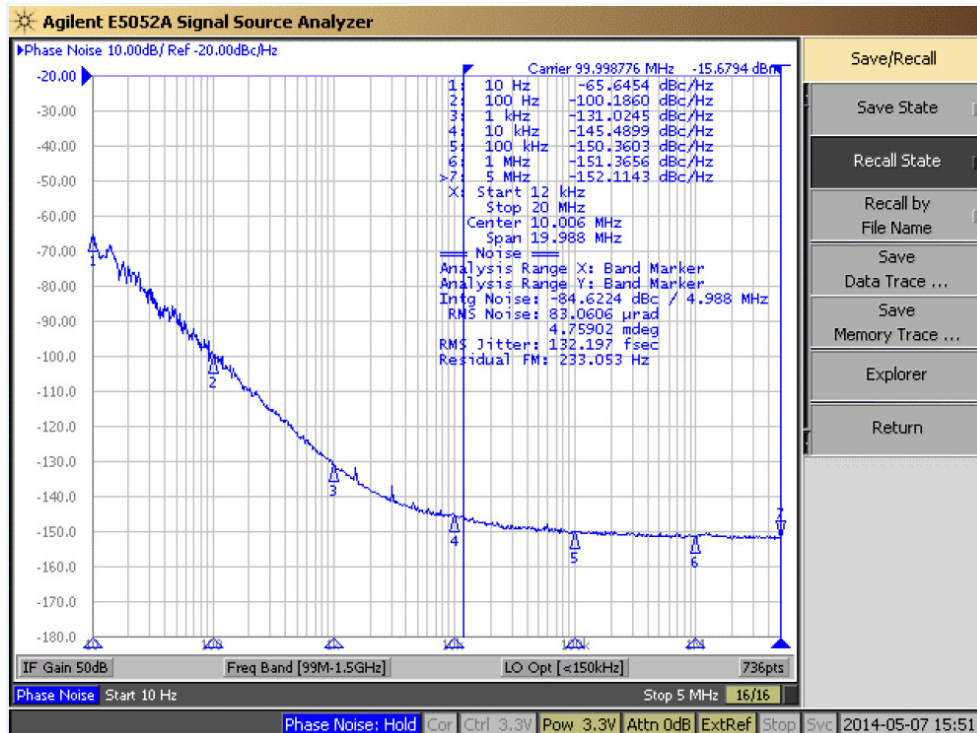
### Performance Data

#### Phase Noise [typical]

25MHz, LVPECL,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$



100MHz, LVPECL,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$

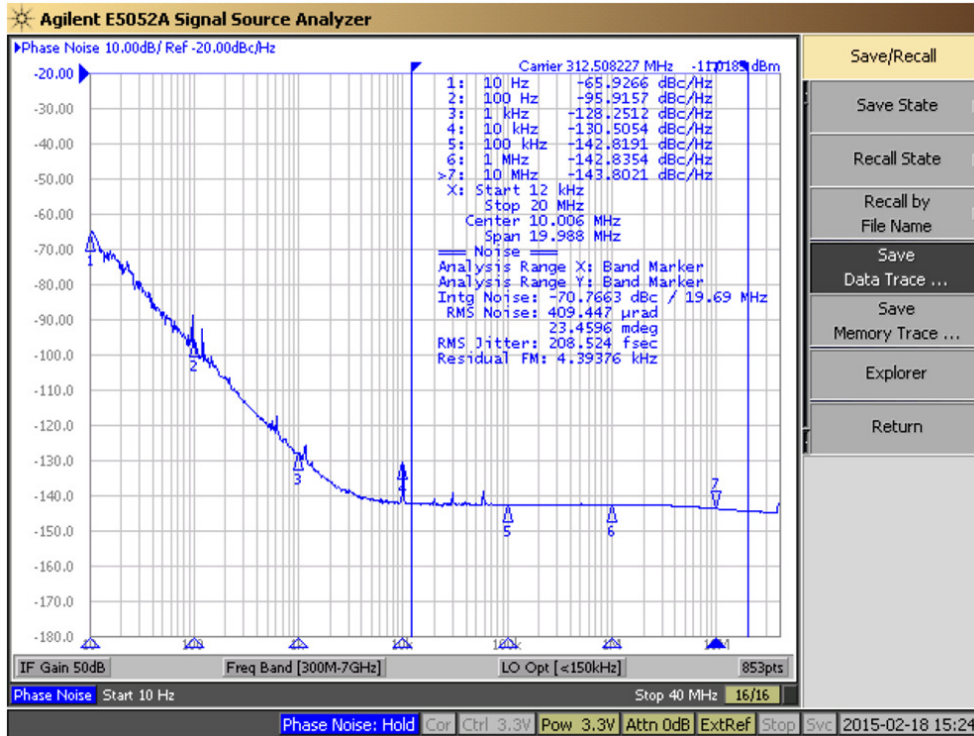


## Electrical Specifications

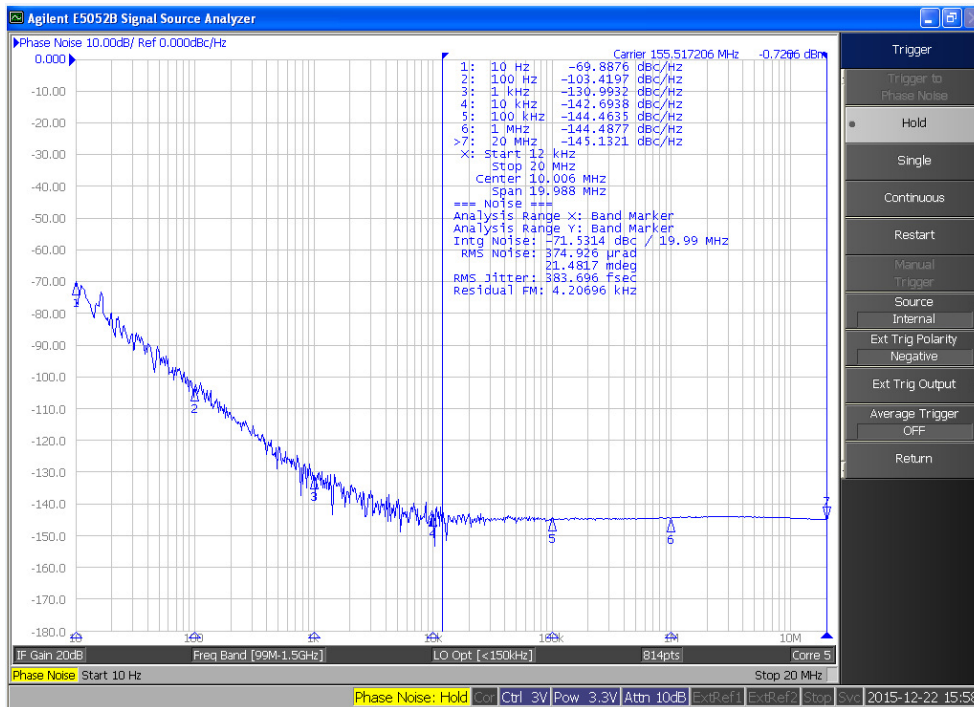
### Performance Data

#### Phase Noise [typical]

312.50MHz, LVPECL,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$



155.52MHz, LVDS,  $V_{CC} = 3.3V$ ,  $T_A = +25^\circ C$





## Electrical Specifications

### Phase Noise Tabulated

Typical,  $V_{CC} = 3.3V$ ,  $T_A = +25^{\circ}C$

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVPECL @ 25.00MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-82.16	
		@ 100Hz	-113.77	
		@ 1kHz	-139.77	dBc/Hz
		@ 10kHz	-156.60	
		@ 100kHz	-161.45	
		@ 1MHz	-161.31	
	@ 5MHz	-159.28		
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	192.78	fs

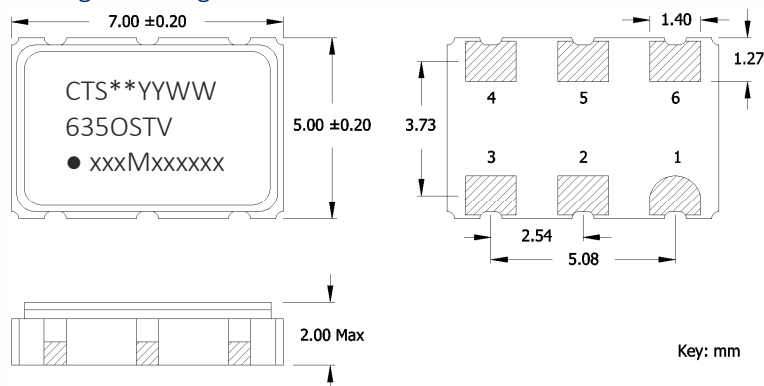
PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVPECL @ 312.20MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-65.93	
		@ 100Hz	-95.92	
		@ 1kHz	-128.25	dBc/Hz
		@ 10kHz	-130.51	
		@ 100kHz	-142.82	
		@ 1MHz	-142.84	
	@ 10MHz	-143.80		
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	208.52	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVPECL @ 100.00MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-65.65	
		@ 100Hz	-100.19	
		@ 1kHz	-131.02	dBc/Hz
		@ 10kHz	-145.49	
		@ 100kHz	-150.36	
		@ 1MHz	-151.37	
	@ 5MHz	-152.11		
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	132.20	fs

PARAMETER	SYMBOL	CONDITIONS	TYP	UNIT
<b>LVDS @ 155.52MHz</b>				
<b>Phase Noise</b>		Single Side Band		
		@ 10Hz	-69.89	
		@ 100Hz	-103.42	
		@ 1kHz	-130.99	dBc/Hz
		@ 10kHz	-142.69	
		@ 100kHz	-144.46	
		@ 1MHz	-144.49	
	@ 20MHz	-145.13		
<b>Phase Jitter, RMS</b>	tjrms	Integration Bandwidth 12kHz - 20MHz	383.70	fs

## Mechanical Specifications

### Package Drawing

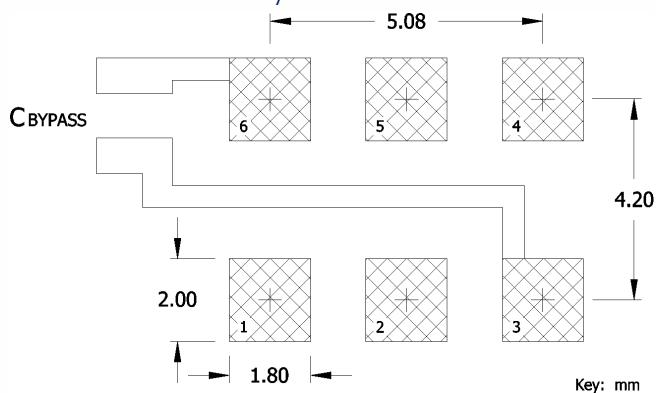


### Marking Information

- \*\* - Manufacturing Site Code.
- YYWW – Date Code; YY – year, WW – week.
- O – Output Type; P or E = LVPECL, L or V = LVDS.
- ST – Frequency Stability/Temperature Code. [Refer to Ordering Information]
- V – Voltage Code; 3 = 3.3V, 2 = 2.5V.
- xxxMxxxxxx – Frequency is marked with only leading significant digits before the “M” and 4 – 6 digits after the “M” [including zeros].

Ex.	Frequency	Marking
	19.44MHz	19M4400
	153.60077MHz	153M60077
	148.351648	148M351648

### Recommended Pad Layout



### Notes

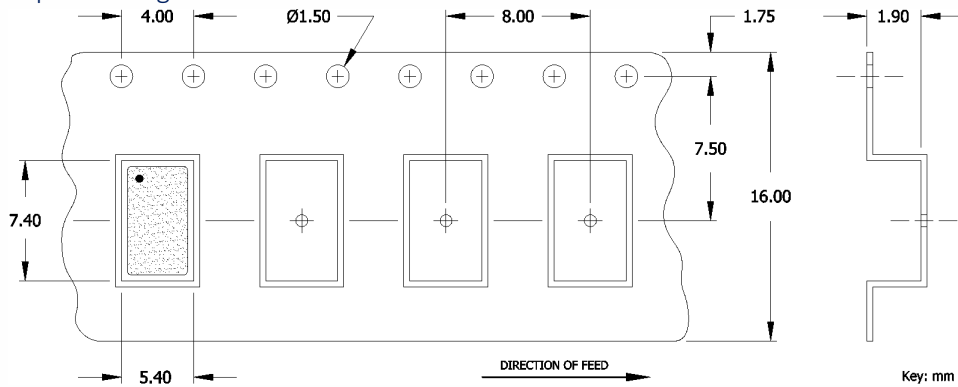
- JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- MSL = 1.

### Pin Assignments

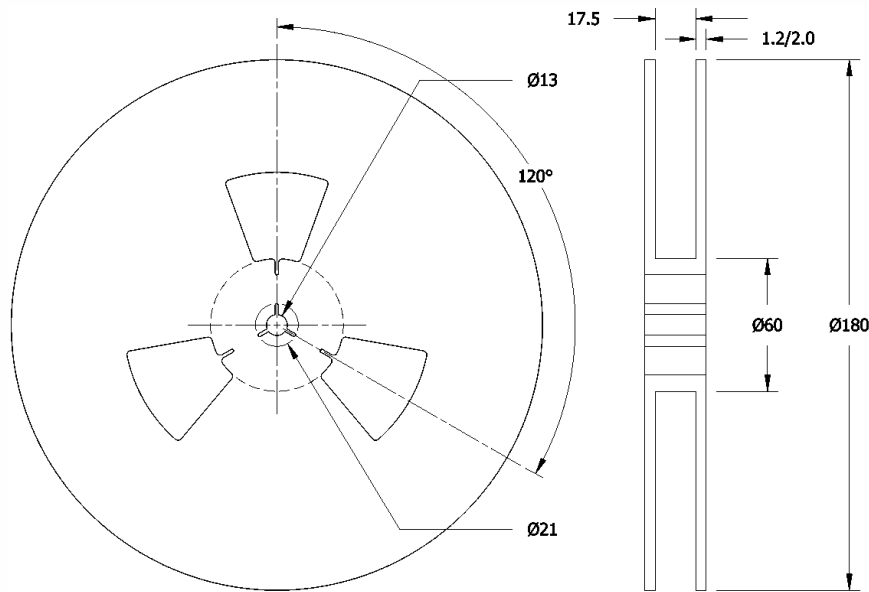
Pin	Symbol	Function
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V <sub>CC</sub>	Supply Voltage

### Packaging - Tape and Reel

#### Tape Drawing



#### Reel Drawing



#### Notes

1. Device quantity is 1k pieces maximum per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.





## Addendum

### Additional Developed Frequencies – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
10.000000	010M0000	125.009375	125M0093	175.000000	175M0000		
19.440000	019M4400	133.000000	133M0000	178.018970	178M0189		
25.000625	025M0006	148.351600	148M3516	178.500000	178M5000		
27.000000	027M0000	148.351648	148M351A	180.000000	180M0000		
40.000000	040M0000	148.500000	148M5000	184.320000	184M3200		
44.736000	044M7360	153.600000	153M6000	225.000000	225M0000		
74.175824	074M175B	153.600770	153M6007				
80.000000	080M0000	156.253906	156M2539				
101.575694	101M5756	167.372800	167M3728				
120.000000	120M0000	173.370800	173M3708				

### Frequency Codes for Cover Page Table – MHz

FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE	FREQUENCY	FREQUENCY CODE
25.000000	025M0000	100.000000	100M0000	156.250000	156M2500	212.500000	212M5000
50.000000	050M0000	125.000000	125M0000	161.132800	161M1328	250.000000	250M0000
74.175800	074M1758	150.000000	150M0000	187.500000	187M5000	312.500000	312M5000
74.250000	074M2500	155.520000	155M5200	200.000000	200M0000		