74LV07AT

Hex buffer with open-drain outputs

Rev. 2 — 8 April 2024 Product data sheet

1. General description

The 74LV07AT is a hex buffer with open-drain outputs. The outputs are open-drain and can be connected to other open-drain outputs to implement active-LOW wired-OR or active-HIGH wired-AND functions.

Designed to operate over a V_{CC} range from 4.5 V to 5.5 V, the inputs are TTL compatible, which allows the device to be used to translate from 3.3 V to 5 V.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial Power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Direct interface with TTL levels
- Supply voltage range from 4.5 V to 5.5 V
- Typical t_{PZL} of 3.5 ns at 5 V
- Typical $V_{OL(p)}$ < 0.8 V at V_{CC} = 5 V, T_{amb} = 25 °C
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 3000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV07ATPW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

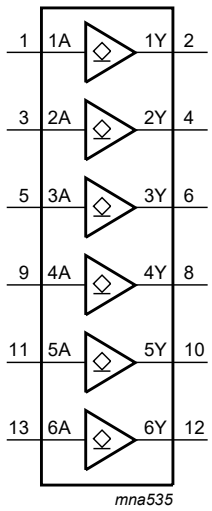


Fig. 1. Logic symbol

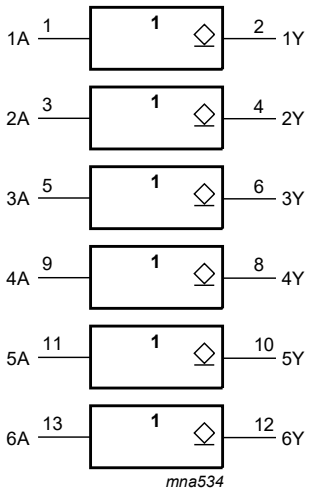


Fig. 2. IEC logic symbol

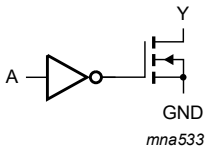


Fig. 3. Logic diagram for one gate

5. Pinning information

5.1. Pinning

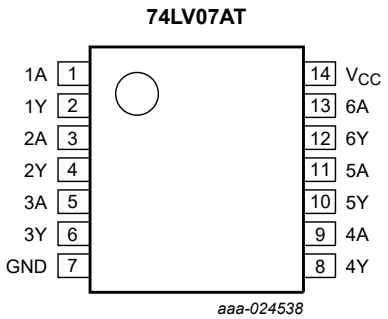


Fig. 4. Pin configuration SOT402-1 (TSSOP14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A, 5A, 6A	1, 3, 5, 9, 11, 13	data input
1Y, 2Y, 3Y, 4Y, 5Y, 6Y	2, 4, 6, 8, 10, 12	data output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state

Input	Output
nA	**nY**
L	L
H	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	+7.0	V
V_O	output voltage	output LOW state, power-down or 3-state mode [2]	-0.5	+7.0	V
I_{IK}	input clamping current	V_I < 0 V	-20	-	mA
I_{OK}	output clamping current	V_O < 0 V	-50	-	mA
I_O	output current	V_O = 0 V to V_{CC}	-	±35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [3]	-	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	5.0	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	output LOW state, power-down or 3-state mode	0	-	5.5	V
T_{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 5.0 V ± 0.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2	-	-	2	-	2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 16mA	-	-	0.44	-	0.55	-	0.55	V
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IH} or V_{IL}; V_O = GND to 5.5 V	-	-	±0.25	-	±2.5	-	±2.5	µA
I_{OFF}	power-off leakage current	V_I or V_O = GND to 5.5 V; V_{CC} = 0 V	-	-	0.5	-	5	-	5	µA
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 0 V to 5.5 V	-	-	±0.1	-	±1	-	±1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	2	-	20	-	20	µA
ΔI_{CC}	additional supply current	per input pin; V_I = 3.4 V; I_O = 0 A; other pins at V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.35	-	1.5	-	1.5	mA

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V. For test circuit see Fig. 6.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t_{PZL}	OFF-state to LOW propagation delay	nA to nY; see Fig. 5								
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3.5	5.3	1	6.6	1	7.7	ns
		C_L = 50 pF	-	5.2	7.7	1	9.5	1	11	ns
t_{PLZ}	LOW to OFF-state propagation delay	nA to nY; see Fig. 5								
		V_{CC} = 4.5 V to 5.5 V								
		C_L = 15 pF	-	3.2	4.3	1	5.1	1	5.7	ns
		C_L = 50 pF	-	5.4	7	1	8	1	8.9	ns
C_I	input capacitance	V_I = V_{CC} or GND; V_{CC} = 5 V	-	2	6	-	6	-	6	pF
C_O	output capacitance	V_O = V_{CC} or GND; V_{CC} = 5 V	-	5	-	-	-	-	-	pF
C_{PD}	power dissipation capacitance	per buffer; C_L = 50 pF; f = 10 MHz; V_I = GND to V_{CC} [2]	-	3	-	-	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 5 V.

[2] C_{PD} is used to determine the dynamic power dissipation P_D (µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

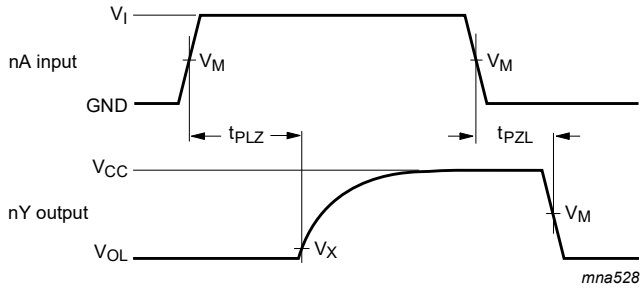
V_{CC} = supply voltage in V.

Table 8. Noise characteristics

GND = 0 V. For test circuit see Fig. 6.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			Unit
			Min	Typ	Max	
V_{CC} = 5 V; C_L = 50 pF						
$V_{OL(p)}$	LOW-level output voltage (peak)		-	0.6	-	V
$V_{OL(v)}$	LOW-level output voltage (valley)		-	-0.4	-	V
$V_{IH(AC)}$	AC HIGH-level input voltage (dynamic)		2	-	-	V
$V_{IL(AC)}$	AC LOW-level input voltage (dynamic)		-	-	0.8	V

10.1. Waveforms and test circuit



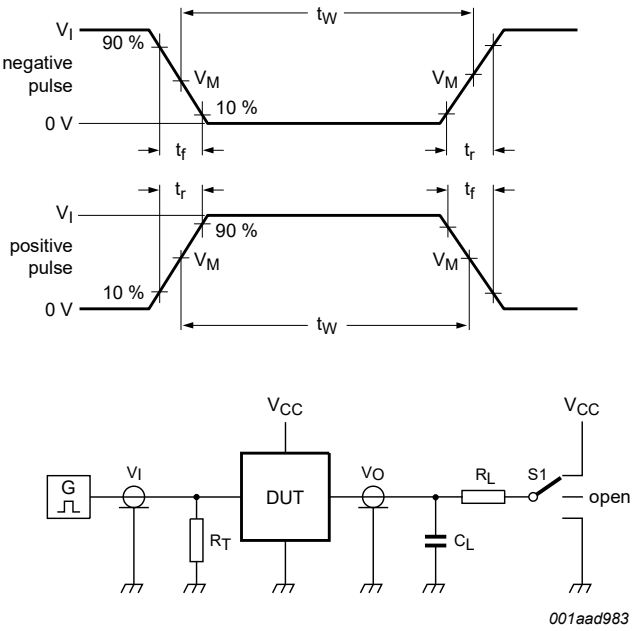
Measurement points are given in Table 9.

V_{OL} is the typical voltage output level that occurs with the output load.

Fig. 5. Propagation delay input (nA) to output (nY)

Table 9. Measurement points

Input	Output	
V_M	V_M	V_X
1.5 V	0.5 × V_{CC}	V_{OL} + 0.3 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistor;

S1 = Test selection switch.

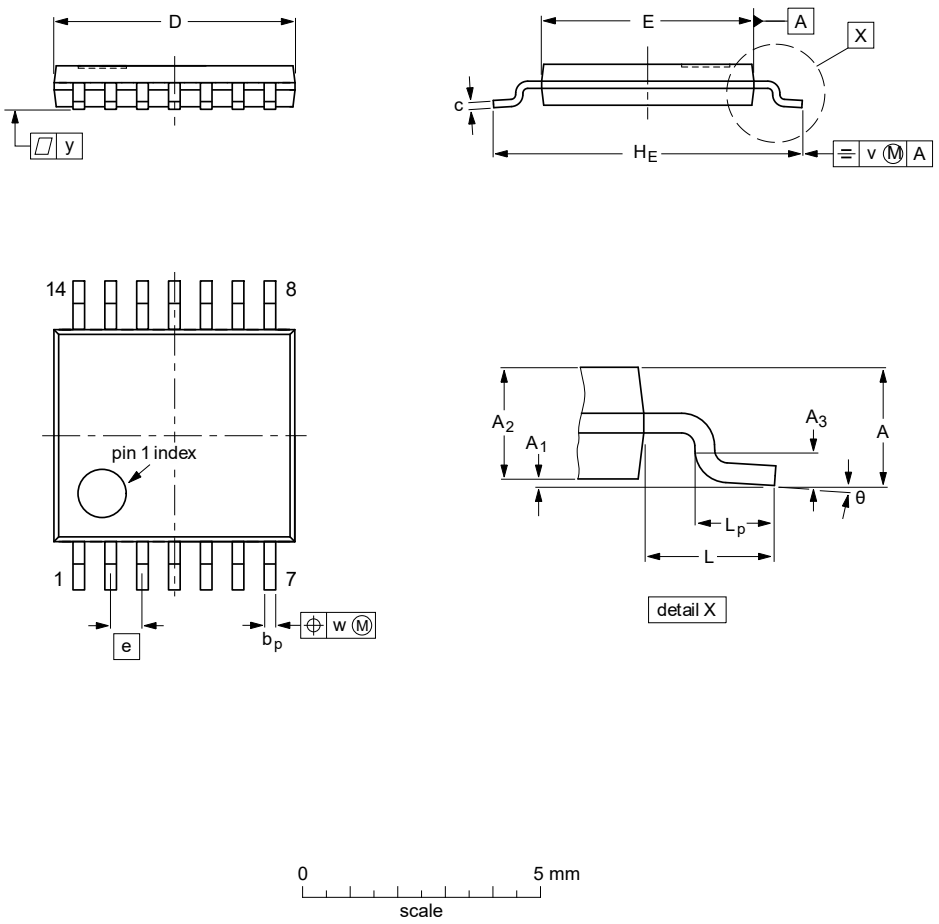
Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Input		Load		S1 position
V_I	t_r, t_f	C_L	R_L	t_{PLZ}, t_{PZL}
GND to 3.0 V	3.0 ns	15 pF, 50 pF	1 kΩ	V_{CC}

11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 7. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV07AT v.2	20240408	Product data sheet	-	74LV07AT v.1
Modifications	• Fig. 7: Aligned TSSOP package outline drawing to JEDEC MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard. • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Table 4: Derating values for P_{tot} total power dissipation updated.			
74LV07AT v.1	20161219	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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