ACT88329 Register Definitions – CMI 101

Abstract

This application note identifies and explains the ACT88329 and ACT88321 internal registers that help make these ICs flexible and configurable for many applications. It provides a short description of each register, its individual bits, their function, and default values. The default register settings in this application note are only valid for the ACT88329VU101. Refer to each datasheet for each specific IC's functional differences from the settings in this document.

The end of the application note provides the differences between the ACT88329 and ACT88321 registers.

Introduction

The ACT88329 is an ActivePMU™ power management unit from Qorvo. It is designed to power a wide range of processors, FPGA's, peripherals, microcontrollers, and solid-state drive applications. The ACT88329 core includes 3 DC/DC step down converters using integrated power FETs and 2 low-dropout regulators (LDOs). Each regulator can be configured for a wide range of output voltages through the I^2C interface.

Today's processors require more complexity in their startup and sequencing requirements. This is also true for entering and exiting sleep and low power modes. The ACT88329 is specifically designed to meet today's processors' stringent power system requirements. These processors include, but are not limited to SMI SM2258, SM2258XT, SM2259, SM2259XT, SM2262, SM2262XT, SM2263, SM2263XT, Marvell Dean and Eldora, STMicroelectronics STM32MP151, Realtek RTS5763, and Innogrit IG5208, IG5216, IG5520, IG5221.

Although the ACT88329 is programmed at the factory with a default configuration, these settings can be changed through the I^2C interface to provide customized configurations optimized for a specific processor and/or end application. IC configurability includes many options such as output voltage, startup sequencing, startup timing, slew rates, GPIO configuration, fault responses, and more. Qorvo identifies these configurations with a Code Matrix Index, CMI. An IC's CMI is identified by the last three digits at the end of the orderable part number. Note that this application note is specific to the ACT88329's CMI 101. Refer to the datasheet for the specific changes to other CMI versions.

Register Types

The ACT88329 ICs contain the following register types.

Basic Volatile - Customer R/W (Read and Write) and RO (Read only). The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed.

Basic Non-Volatile - Customer R/W and RO. The customer can modify these register values to change IC functionality. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult Sales@Qorvo.com for custom options and minimum order quantities.

Factory Non-Volatile – Factory bits. These bits are used by the factory to set IC functionality. The customer can read these bits but cannot write to them. The default values can be modified at the factory to optimize IC functionality for specific applications.

The ACT88329 contains five major register spaces.

Master Reg	0x00h to 0x1Dh
Buck1 Reg	0x40h to 0x50h
Buck2 Reg	0x60h to 0x70h
Buck3 Reg	0x80h to 0x90h
LDO12 Reg	0xA0h to 0xB1h

Register Map Overview

The following table show an overview of the ACT88329 register map. Note that not all register addresses are sequential.

MASTER REGISTERS								
AADR (HEX)	7	6	5	4	3	2	1	0
00	ROM STAT	WD TIMER ALERT	TWARN	VSYSSTAT	VIN_POK_OV	PBASTAT	VSYSWARN	RFU
01	ROM INT MSK	WD ALERT MSK	TMSK	VSYSMSK	VIN_POK_OV_MASK	PBAMSK	VSYSWARN MASK	RFU
02	RFU	RFU	VSYSWARN Real time	VSYSDAT	RFU	RFU	RFU	PBDAT
03	RFU	GPIO7 STAT	GPIO6 STAT	GPIO5 STAT	GPIO4 STAT	GPIO3 STAT	GPIO2 STAT	GPIO1 STAT
04	RFU	GPIO7 Toggled	GPIO6 Toggled	GPIO5 Toggled	GPIO4 Toggled	GPIO3 Toggled	GPIO2 Toggled	GPIO1 Toggled
05	RFU	GPIO7 MASK	GPIO6 MASK	GPIO5 MASK	GPIO4 MASK	GPIO3 MASK	GPIO2 MASK	GPIO1 MASK
06	INTADR							
07	MR	SLEEP	RFU	DPSLP	RFU	POWER OFF	WDPCEN	WDSREN
08	MR	SLEEP	RFU	DPSLP	RFU	POWER OFF	WDPCEN	WDSREN
09	TRST_DLY[2:0]			RFU		RFU		DIS OV UV SHUTDOWN
0A	EN POWERCYCLE	EN POWEROFF	ROM_EN	VSYSMON[4:0]				
0B	IO1_DLY[1:0]		IO2_DLY[1:0]		IO3_DLY[1:0]		IO4_DLY[1:0]	
0C	IO5_DLY[1:0]		IO6_DLY[1:0]		IO7_DLY[1:0]		WDTIME	RETRY TIME
0D	RFU				RFU			
0E	RFU				RFU			
0F	RFU				RFU			
10	RFU				RFU			
11	RFU				RFU			
12	RFU				RFU			
13	RFU				RFU			
14	POK_OV[2:0]			VSYSWARN[4:0]				
15	VIN_LVL	RFU	RFU	SLEEP MODE	DPSLP MODE	EN_DVS_BY_I2C	RFU	RFU
16	I2C ADDR MSB[1:0]		RFU	RFU	RFU	VIN_OV[2:0]		
	BUCK1							
40	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
41	FORCE_LPM_FONT	RFU	ENPD_LOAD	DIS_PULLDOWN	BUCK1_BYP_EN	EN_SKIP_LPM	DRV_ADJ<1:0>	
42	RFU	VSET0[6:0]						
43	RFU	VSET1[6:0]						
44	ON	PBINEN	QLTCH	SLEEP EN	RFU	DP SLEEP EN	ILIM_SET	RFU
45	MODE	RST	DBQL			DBOK		
46	DBON				SST	DISLPM	DBSTBY	
47	PHASE_DELAY	PHASE	ON DELAY[2:0]			OFF DELAY[2:0]		
	BUCK2							
60	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
61	FREQ_SEL[1:0]		ENPD_LOAD	DIS_PULLDOWN	IPD_LOAD[1:0]		DRV_ADJ<1:0>	
62	SAVE_IQQ	VSET0[6:0]						
63	RFU	VSET1 [6:0]						
64	ON	PBINEN	QLTCH	SLEEP EN	RFU	DP SLEEP EN	ILIM_SET	FCCM
65	MODE	RST	DBQL			DBOK		
66	DBON				SST[1:0]		DBSTBY	
67	IPD_LOAD		ON DELAY[2:0]			OFF DELAY[2:0]		
	BUCK3							
80	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
81	FREQ_SEL[1:0]		ENPD_LOAD	DIS_PULLDOWN	IDP_LOAD[1:0]		DRV_ADJ<1:0>	
82	SAVE_IQQ	RFU	RFU	VSET0[4:0]				
83	RFU	RFU	RFU	VSET1[4:0]				
84	ON	PBINEN	QLTCH	SLEEP EN	RFU	DP SLEEP EN	ILIM_SET	FCCM
85	MODE	RST	DBQL			DBOK		
86	DBON				SST[1:0]		DBSTBY	
87	IPD_LOAD		ON DELAY[2:0]			OFF DELAY[2:0]		
	LDO1/2							
A0	PWR_GOOD_LDO1	OV_LDO1	LDO1_ILIM	RFU	UV_FLTMSK_LDO1	LDO1_OV_FLTMSK	LDO1_ILIM_FLTMSK	RFU
A1	B1_IPD_LOAD		LDO1 VSET[5:0]					
A2	ON LDO1 (DEFAULT 1)	PBIN EN LDO1	RFU	SLEEP EN LDO1	DPSLEEP EN LDO1	DBQL LDO1 [2:0]		
A3	ON DELAY LDO1 [2:0]			OFF DELAY LDO1 [2:0]			MODE LDO1	RST LDO1
A4	DBON LDO1[3:0]				DBOK LDO1[3:0]			
A5	IM SHUTDOWN DIS_LDO	ENOV_PLSW1	RFU	DIS_PULLDOWN_L1	NLSW1_ILIM_SCL	ILIM_SCL_LDO1	SST_LDO1	LDO1_QLTCH
A6	PWR_GOOD_LDO2	OV_LDO2	LDO2_ILIM	RFU	UV_FLTMSK_LDO2	LDO2_OV_FLTMSK	LDO2_ILIM_FLTMSK	RFU
A7	B1_IPD_LOAD[3:2]		LDO2 VSET[5:0]					
A8	ON LDO2 (DEFAULT 1)	EN_BYP_OV	RFU	SLEEP EN LDO2	DPSLEEP EN LDO2	DBQL LDO2 [2:0]		
A9	ON DELAY LDO2 [2:0]			OFF DELAY LDO2 [2:0]			MODE LDO2	RST LDO2
AA	DBON LDO2 [3:0]				DBOK LDO2 [3:0]			
AB	ILIM SHUTDOWN DIS_LDO2	RFU	RFU	DIS_PULLDOWN_LDO2	RFU	ILIM_SCL_LDO2	SST_LDO2	LDO2_QLTCH
AE	RFU	LDO2_MODE_SEL	RFU	RFU	RFU	RFU	RFU	RFU

MASTER REGISTERS

MSTR00 - Master Configuration Register

Address = 0x00h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ROM_STAT	WD_TIMER_ALERT	TWARN	VSYS_STAT	VIN_POK_OV	RFU	VSYSWARN	RFU
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
ROM_STAT	0 – Not in ROM mode. 1 – in ROM mode	If ROM mode is started, this bit goes high and stay high until is read. This register is only valid with ICs that use PWREN mode
WD_TIMER_ALERT	0 – the timer is not expired 1 – the timer is expired	If watchdog is enabled and watchdog timer time out, this bit goes high and stay high until is read.
TWARN	0 – Junction temperature < TWARN Threshold 1 – Junction temperature > TWARN Threshold	If die temperature > 135 deg C, this bit goes high. It stays high until die temperature < 115oC and it is read.
VSYS_STAT	0 – VSYS > VSYS Monitor Threshold 1 – VSYS < VSYS Monitor Threshold	When VIN < SYSMON, this bit goes high and stays high until is read.
VIN_POK_OV	0 – VIN < VIN_POK_OV 1 – VIN> VIN_POK_OV	When VIN > POK_OV, this bit goes high. It is latched high until VIN < POK_OV-200mV and the bit is read via I2C
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSYSWARN	0 – VIN > VSYS_WARN 1 – VIN< VSYS_WARN	When VIN < SYSWARN, this bit goes high and stays high until is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

MSTR01 - Master Configuration Register

Address = 0x01h	Default = 0xFFh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	ROM_INT _MSK	WD_ALERT _MSK	TMSK	VSYS_MSK	VIN_POK_OV _MASK	RFU	VSYSWARN _MASK	RFU
Default	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	RO	R/W	RO

Name	Description	Notes
ROM_INT_MSK	0 – Interrupt is not masked 1 – Interrupt is masked	Masks the ROM interrupt bit
WD ALERT MSK	0 – Interrupt is not masked 1 – Interrupt is masked	Masks the Watch Dog Timer Expiration interrupt bit
TMSK	0 – Interrupt is not masked 1 – Interrupt is masked	Masks the Thermal Warning Status interrupt bit
VSYS_MSK	0 – Interrupt is not masked 1 – Interrupt is masked	Masks the VSYS UV interrupt mask bit
VIN_POK_OV_MASK	0 – Interrupt is not masked 1 – Interrupt is masked	Masks the VIN POK OV interrupt mask bit
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSYSWARN_MASK	0 – Interrupt is not masked 1 – Interrupt is masked	Masks the SYSWARN interrupt mask bit
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

MSTR02 - Master Configuration Register

Address = 0x02h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [1:0]		VSYSWARN_RT	VSYSDAT	RFU [2:0]			PBDAT
Default	00		0	0	000			0
Access	RO		R/W	R/W	RO			RO

Name	Description	Notes
RFU [1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSYSWARN_RT	0 – VIN is lower than VSYSWARN 1 – VIN is higher than VSYSWARN	Real time status of the AVIN voltage being above or below the SYSWARN threshold
VSYSDAT	0 – VIN is lower than VSYSMON 1 – VIN is higher than VSYSMON	Real time status of the AVIN voltage being above or below the SYSMON threshold
RFU [2:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
PBDAT	0 – Push Button is being asserted 1 – Push Button is de-assert	Real time status of the push button pin. Only valid for ICs with pushbutton functionality

MSTR03 - Master Configuration Register

Address = 0x03h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
	RFU	GPIO7_STAT	GPIO6_STAT	GPIO5_STAT	GPIO4_STAT	GPIO3_STAT	GPIO2_STAT	GPIO1_STAT
Default	0	0	0	0	0	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
GPIO7_STAT	0 – GPIO7 input is logic low 1 – GPIO7 input is logic high	Shows the GPIOx input real-time status when the GPIO is configured as an input.
GPIO6_STAT	0 – GPIO6 input is logic low 1 – GPIO6 input is logic high	
GPIO5_STAT	0 – GPIO5 input is logic low 1 – GPIO5 input is logic high	
GPIO4_STAT	0 – GPIO4 input is logic low 1 – GPIO4 input is logic high	
GPIO3_STAT	0 – GPIO3 input is logic low 1 – GPIO3 input is logic high	
GPIO2_STAT	0 – GPIO2 input is logic low 1 – GPIO2 input is logic high	
GPIO1_STAT	0 – GPIO1 input is logic low 1 – GPIO1 input is logic high	

MSTR04 - Master Configuration Register

Address = 0x04h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
	RFU	GPIO7_Toggled	GPIO6_Toggled	GPIO5_Toggled	GPIO4_Toggled	GPIO3_Toggled	GPIO2_Toggled	GPIO1_Toggled
Default	0	0	0	0	0	0	0	0
Access	R0	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
GPIO7_Toggled	0 – GPIO7 input logic level has not changed 1 – GPIO7 input logic level has changed	When this bit is a 1, reading it resets it to 0
GPIO6_Toggled	0 – GPIO6 input logic level has not changed 1 – GPIO6 input logic level has changed	When this bit is a 1, reading it resets it to 0
GPIO5_Toggled	0 – GPIO5 input logic level has not changed 1 – GPIO5 input logic level has changed	When this bit is a 1, reading it resets it to 0
GPIO4_Toggled	0 – GPIO4 input logic level has not changed 1 – GPIO4 input logic level has changed	When this bit is a 1, reading it resets it to 0
GPIO3_Toggled	0 – GPIO3 input logic level has not changed 1 – GPIO3 input logic level has changed	When this bit is a 1, reading it resets it to 0
GPIO2_Toggled	0 – GPIO2 input logic level has not changed 1 – GPIO2 input logic level has changed	When this bit is a 1, reading it resets it to 0
GPIO1_Toggled	0 – GPIO1 input logic level has not changed 1 – GPIO1 input logic level has changed	When this bit is a 1, reading it resets it to 0

MSTR05 - Master Configuration Register

Address = 0x05h	Default = 0x7Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	GPIO7 _MASK	GPIO6 _MASK	GPIO5 _MASK	GPIO4 _MASK	GPIO3 _MASK	GPIO2 _MASK	GPIO1 _MASK
Default	0	1	1	1	1	1	1	1
Access	R0	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
GPIO7_MASK	0 – GPIO7 Toggle Interrupt is not masked 1 – GPIO7 Toggle Interrupt is masked	If not masked, a GPIO input logic level status change triggers an interrupt in register 0x04h.
GPIO6_MASK	0 – GPIO6 Toggle Interrupt is not masked 1 – GPIO6 Toggle Interrupt is masked	
GPIO5_MASK	0 – GPIO5 Toggle Interrupt is not masked 1 – GPIO5 Toggle Interrupt is masked	
GPIO4_MASK	0 – GPIO4 Toggle Interrupt is not masked 1 – GPIO4 Toggle Interrupt is masked	
GPIO3_MASK	0 – GPIO3 Toggle Interrupt is not masked 1 – GPIO3 Toggle Interrupt is masked	
GPIO2_MASK	0 – GPIO2 Toggle Interrupt is not masked 1 – GPIO2 Toggle Interrupt is masked	
GPIO1_MASK	0 – GPIO1 Toggle Interrupt is not masked 1 – GPIO1 Toggle Interrupt is masked	

MSTR06 - Master Configuration Register

Address = 0x06h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	INTADR [7:0]							
Default	00000000							
Access	RO							

Name	Description	Notes
INTADR [7:0]	Value Register Function 0x00h System Level Functions 0x01h GPIO 0x40h Buck1 0x60h Buck2 0x80h Buck3 0xA1h LDO1 0xA2h LDO2	The value contained in this register identifies the I^2C register that generated the interrupt.

MSTR07 - Master Configuration Register

Address = 0x07h	Default = 0x00h	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	MR	SLEEP	RFU	DPSLP	RFU	POWER_OFF	WDPCEN	WDSREN
Default	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
MR	0 – No Manual Reset 1 – Initiate a Manual Reset or Power Cycle by setting this bit by I^2C	Writing a 1 to this bit clears all VM registers, move IC to POWER OFF state, then restarts after 0.5s.
SLEEP	0 – Can make IC exit SLEEP state 1 – Can make IC enter SLEEP state	See datasheet for details on how this bit puts IC into SLEEP state
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
DPSLP	0 – Can make IC exit DPSLP state. 1 – Can make IC enter DPSLP state.	See datasheet for details on how this bit puts IC into DPSLP state
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
POWER_OFF	0 – IC is operating normally 1 – IC Defaults to POWER OFF = 1 and all regulators are off when POWER OFF = 1 upon power up.	Clear Power Off to 0 using I2C to start a power on sequence.
WDPCEN	0 – IC does not power cycle if the watchdog timer times out 1 – IC power cycles if the watchdog timer times out	Note that this is a higher priority than WDSREN
WDSREN	0 – Disables a soft reset if the watchdog timer times out 1 – Enables a soft reset if the watchdog timer times out	

MSTR09 - Master Configuration Register

Address = 0x09h	Default = 0xA0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	TRST_DLY [2:0]			RFU [3:0]				DIS_UV_OV_Shutdown
Default	101			0000				0
Access	R/W			RO				R/W

Name	Description	Notes
TRST_DLY [2:0]	000 – 0.5ms 001 – 1ms 010 – 2.5ms 011 – 5ms 100 – 10ms 101 – 20ms 110 – 50ms 111 – 100ms	Sets the nRESET delay time
RFU [3:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DIS_UV_OV_Shutdown	0 – If an output enters an UV/OV fault condition, the IC enters the OVUV Fault State 1 – If an output enters an UV/OV fault condition, the IC does not enter UVOV Fault State	

MSTR0A - Master Configuration Register

Address = 0x0Ah	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	EN_POWERCYCLE	EN_ POWEROFF	ROM_EN	VSYSMON [4:0]				
Default	0	0	0	00000				
Access	R/W	R/W	R/W	R/W				

Name	Description	Notes
EN_POWERCYCLE	0 – Disable Power Cycle by Push-Button 1 – Enable Power Cycle by Push-Button	
EN_ POWEROFF	0 – Disable Power OFF by Push-Button 1 – Enable Power OFF by Push-Button	
ROM_EN	0 – Disable ROM mode 1 – Enable ROM mode	
VSYSMON [4:0]	00000 = 2.7V to 10110 = 4.8V Step size = 0.1V per bit 10111 to 11111 = 4.8V	SYSMON rising threshold voltage setting. All values above 10111b set to 4.8V

MSTR0B - Master Configuration Register

Address = 0x0Bh	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IO1_DLY [1:0]		IO2_DLY [1:0]		IO3_DLY [1:0]		IO4_DLY [1:0]	
Default	00		00		00		00	
Access	R/W		R/W		R/W		R/W	

Name	Description	Notes
IO1_DLY [1:0]	00 – 0ms 01 – 1ms 10 – 5ms 11 – 10ms	Delay setting for both input mode/ output OD mode of GPIO1
IO2_DLY [1:0]	00 – 0ms 01 – 1ms 10 – 5ms 11 – 10ms	Delay setting for both input mode/ output OD mode of GPIO2
IO3_DLY [1:0]	00 – 0ms 01 – 1ms 10 – 5ms 11 – 10ms	Delay setting for both input mode/ output OD mode of GPIO3
IO4_DLY [1:0]	00 – 0ms 01 – 1ms 10 – 5ms 11 – 10ms	Delay setting for both input mode/ output OD mode of GPIO4

MSTR0C - Master Configuration Register

Address = 0x0Ch	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IO5_DLY [1:0]		IO6_DLY [1:0]		IO7_DLY [1:0]		WD_TIME	RETRY_TIME
Default	00		00		00		0	0
Access	R/W		R/W		R/W		R/W	R/W

Name	Description	Notes
IO5_DLY [1:0]	00 – 0ms 01 – 1ms 10 – 5ms 11 – 10ms	Delay setting for both input mode/ output OD mode of GPIO1
IO6_DLY [1:0]	00 – 0ms 01 – 1ms 10 – 5ms 11 – 10ms	Delay setting for both input mode/ output OD mode of GPIO2
IO7_DLY [1:0]	00 – 0ms 01 – 1ms 10 – 5ms 11 – 10ms	Delay setting for both input mode/ output OD mode of GPIO3
WD_TIME	0 – 7s 1 – 20s	Watchdog out time of ROM mode
RETRY_TIME	0 – 100ms 1 – 250ms	Retry timer setting when IC shuts down and restarts

RFU - RFU

Address = 0x0Dh-0x13h	Default = N/A	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [7:0]							
Default	N/A							
Access	R/W							

Name	Description	Notes
RFU [7:0]	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.

MSTR14 – Master Configuration Register

Address = 0x14h	Default = 0x03h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK_OV [2:0]			VSYSWARN [4:0]				
Default	000			00011				
Access	R/W			R/W				

Name	Description	Notes
POK_OV [2:0]	000 – 3.50V 001 – 3.80V 010 – 4.11V 011 – 4.40V 100 – 4.70V 101 – 5.00V 110 – 5.30V 111 – 5.60V	VIN_POK_OV setting (rising)
VSYSWARN [4:0]	00000 = 2.7V to 11110: 5.7V Step size = 0.1V per bit 11110 to 11111 = 5.7V	VSYSWARN setting (rising)

MSTR15 – Master Configuration Register

Address = 0x15h	Default = 0x18h	Type = Factory Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	VIN_LVL	RFU	DIS_OTS	SLEEP_MODE	DPSLP_MODE	EN_DVS_BY_I2C	RFU	RFU
Default	0	0	0	1	1	0	0	0
Access	RO	RO	RO	RO	RO	RO	RO	RO

Name	Description	Notes
VIN_LVL	0 – 2.6V 1 – 3.5V	VIN UV setting (falling)
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
SLEEP_MODE	0 – AND function of inputs: I2C, GPIOs 1 – OR function	Sleep mode
DPSLP_MODE	0 – AND function of inputs: I2C, GPIOs 1 – OR function	Deep sleep mode
EN_DVS_BY_I2C	0 – Disable DVS using I2C by NVM bit 1 – Enable DVS using I2C by NVM bit to control DB9, DB10 and DB11	
RFU	Reserved for Future Use	Do not change this register value. Changing the register values can affect IC functionality.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

MSTR16 – Master Configuration Register

Address = 0x16h	Default = 0x00h	Type = Factory Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	I2CAddMsb [1:0]		RFU [2:0]			VIN_OV [2:0]		
Default	00		000			000		
Access	RO		RO			RO		

Name	Description	Notes
I2CAddMsb [1:0]	00 – 7-Bit Slave Address = 0x25h 01 – 7-Bit Slave Address = 0x27h 10 – 7-Bit Slave Address = 0x67h 11 – 7-Bit Slave Address = 0x6Bh	Set's the IC's default I2C Address
RFU [2:0]	Reserved for Future Use	Do not change these register values. Changing the register values can affect IC functionality.
VIN_OV [2:0]	000 – 3.70V 001 – 4.00V 010 – 4.31V 011 – 4.61V 100 – 4.91V 101 – 5.20V 110 – 5.50V 111 – 5.81V	Sets the VIN_OV over-voltage rising threshold

BUCK REGULATORS REGISTERS

Buck1 Registers

B1_REG00 – Buck1 Configuration Register

Address = 0x40h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	ILIM_WARN	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	ILIM_WARN_FLTMSK
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	0 – Buck1 voltage is below the power good threshold 1 – Buck1 voltage is above the power good threshold	Provides real-time power good status
OV	0 – Buck1 voltage is below the overvoltage threshold 1 – Buck1 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It stays high until output voltage < OV and the bit is read.
ILIM	0 – Buck1 is below the ILIM threshold 1 – Buck1 is above the ILIM threshold	If the peak switch current reaches 122% of ILIMSET threshold, this bit goes high. It stays high until peak switch current < 122% of ILIMSET and this bit is read.
ILIM_WARN	0 – Buck1 is below the ILIM warning threshold 1 – Buck1 is above the ILIM warning threshold	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It stays high until peak switch current < ILIMSET and this bit is read.
UV_FLTMSK	0 – Unmasks the Buck1 POK signal 1 – Masks the Buck1 POK signal	When 1, the Buck1 POK signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is disabled or drops out of regulation. B1_POK still provides real-time power good status.
OV_FLTMSK	0 – Unmasks the Buck1 OV register 1 – Masks the Buck1 OV register	When 1, the Buck1 OV signal is masked and does not go to the master controller. This prevents Buck1 from asserting the nIRQ pin when it is above regulation limits. B1_OV still provides OV status.
ILIM_FLTMSK	0 – Unmasks the Buck1 ILIM register 1 – Masks the Buck1 ILIM register	When 1, the ILIM fault bit is masked from the master fault register. ILIM still provides current limit status.
ILIM_WARN_FLTMSK	0 – Unmasks the Buck1 ILIM_WARN register 1 – Masks the Buck1 ILIM_WARN register	When 1, the ILIM_WARN fault bit is masked from the master fault register. ILIM_WARN still provides current limit warning status.

B1_REG01 – Buck1 Configuration Register

Address = 0x41h	Default = 0x00h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FORCE_LPM_FONT	RFU	ENPD_LOAD	DIS_PULL-DOWN	BYP_EN	EN_SKIP_LPM	DRV_ADJ [1:0]	
Default	0	0	0	0	0	0	00	
Access	R/W	R/W	RO	R/W	R/W	R/W	R/W	

Name	Description	Notes
FORCE_LPM_FONT	0 – Does not force Buck1 to operate in ULPM mode. 1 – Force Buck1 to operate in ULPM mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
ENPD_LOAD	0 – Disable Buck1 pulldown load function 1 – Enable Buck1 pulldown load function	Enable Buck1 pull-down load when Buck1 is enabled. Registers 0xA1[7:6] and 0xA7[7:6] config the current load.
DIS_PULLDOWN	0 – Enable the discharge resistor. 1 – Disable the discharge resistor	When = 0, the 4.4Ohm discharge resistor is connected to Vout when Buck1 is turned off.
BYP_EN	0 – Configures Buck1 for BUCK Mode 1 – Configured Buck1 for BYPASS Mode	Do not change this bit when Buck1 is enabled.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DRV_ADJ [1:0]	00 – Slowest 11 – Fastest	Adjust Gate Driver (Rising and Falling SW)

B1_VSET00 – Buck1 Voltage Set0 Register

Address = 0x42h	Default = 0x5Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET0 [6:0]						
Default	0	1011100						
Access	R/O	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET0 [6:0]	Buck1 output voltage setting in ACTIVE mode.	Controls the Buck1 output voltage. B1_VSET0 is used in ACTIVE mode. The output voltage is equal to VSET [6:0] * 0.025 + 0.6V.

B1_VSET01 – Buck1 Voltage Set1 Register

Address = 0x43h	Default = 0x4Ch	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET1 [6:0]						
Default	0	1001100						
Access	R/O	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET1 [6:0]	Buck1 output voltage setting for dynamic voltage scaling and SLEEP mode.	Controls Buck1 output voltage. B1_VSET1 is used in DVS or SLEEP modes. The output voltage setting is the same as the B1_VSET0 register.

B1_REG04 – Buck1 Configuration Register

Address = 0x44h	Default = 0x42h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBIN_EN	QLTCH	SLEEP_EN	RFU	DPSLP_EN	ILIM_SET	RFU
Default	0	1	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Buck1 is enabled through normal sequencing 1 – Buck1 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck1 shuts down when its sequenced input shuts down 1 – Buck1 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck1 stays on when the IC enters Sleep mode 1 – Buck1 turns off when the IC enters Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DPSLP_EN	0 – Buck1 stays on when the IC enters Deep Sleep mode 1 – Buck1 turns off when the IC enters Deep Sleep mode	
ILIM_SET	0 – Peak current limit set to 3.8A 1 – Peak current limit set to 5.0A	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B1_REG05 – Buck1 Configuration Register

Address = 0x45h	Default = 0x93h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	0	010			011		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck1 does not affect nRESET output 1 – Buck1 turning off asserts nRESET output low	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG06 – Buck1 Configuration Register

Address = 0x46h	Default = 0x21h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST	DISLPM	DBSTBY [1:0]	
Default	0010				0	0	01	
Access	R/W				R/W	R/W	R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SST	0 – 500us 1 – 250us	Soft-start time option
DISLPM	0 – Enable LPM mode 1 – Disable LPM mode	Disable Low Power Mode. Will works in DCM or CCM depend on the output load
DBSTBY [1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B1_REG07 – Buck1 Configuration Register

Address = 0x47h	Default = 0xC0h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	PHASE_DELAY	PHASE	ON_DELAY [2:0]			OFF_DELAY [2:0]		
Default	1	1	000			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
PHASE_DELAY	0 – Aligns converter switching to the main clock edge 1 – Delays converter switching 100ns from the main clock edge	
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	
ON_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the Buck1 enable input to when it turns on.
OFF_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the Buck1 disable input to when it turns off.

BUCK2 REGULATOR REGISTERS

B2_REG00 – Buck2 Configuration Register

Address = 0x60h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
Default	0	0	0	0	1	1	1	1
Access	RO	RO	RO	RO	R/W	R/W	R/W	R/W

Name	Description	Notes
POK	0 – Buck2 voltage is below the power good threshold 1 – Buck2 voltage is above the power good threshold	Provides real-time power good status
OV	0 – Buck2 voltage is below the overvoltage threshold 1 – Buck2 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It stays high until output voltage < OV and this bit is read.
ILIM	0 – Buck2 is below the ILIM threshold 1 – Buck2 is above the ILIM threshold	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It stays high until peak switch current < ILIMSET and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK	0 – Unmasks the Buck2 POK signal 1 – Masks the Buck2 POK signal	When 1, the Buck2 POK signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is disabled or drops out of regulation. B2_POK still provides real-time power good status.
OV_FLTMSK	0 – Unmasks the Buck2 OV register 1 – Masks the Buck2 OV register	When 1, the Buck2 OV signal is masked and does not go to the master controller. This prevents Buck2 from asserting the nIRQ pin when it is above regulation limits. OV still provides OV status.
ILIM_FLTMSK	0 – Unmasks the Buck2 ILIM register 1 – Masks the Buck2 ILIM register	When 1, the ILIM fault bit is masked from the master fault register. ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B2_REG01 – Buck2 Configuration Register

Address = 0x61h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD	DIS_PULLDOWN	IPD_LOAD[1:0]		DRV_ADJ [1:0]	
Default	01		00	0	00		00	
Access	R/W	R/W	R/O	R/W	R/W		R/W	

Name	Description	Notes
FREQ_SEL[1:0]	00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 – Disable Buck2 pulldown load function 1 – Enable Buck2 pulldown load function	Enable Buck2 pull-down load when Buck2 is enabled. Registers 0x61[3:2] and 0x67[7:6] config the current load.
DIS_PULLDOWN	0 – Discharge VOUT when turn-off BUCK by 9.4Ohm 1 – Don't discharge VOUT when turn-off BUCK	Option disable Pull-Down Resistor when BUCK is turned-off
IPD_LOAD[1:0]	Sets Buck2 pulldown load	Combine with IPD_LOAD[3:2] bits in register 0x67h 0000 – 10mA 0001 – 13mA 0010 – 17mA 0011 – 20mA 0100 – 24mA 0101 – 27mA 0110 – 30mA 0111 – 34mA 1000 – 37mA 1001 – 40mA 1010 – 44mA 1011 – 47mA 1100 – 50mA 1101 – 54mA 1110 – 57mA 1111 – 60mA
DRV_ADJ [1:0]	00 – Slowest 11 – Fastest	Adjust Gate Driver (Rising and Falling SW)

B2_VSET00 – Buck2 Voltage Set0 Register

Address = 0x62h	Default = 0xABh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	SAVE_IQQ	VSET0 [6:0]						
Default	1	0101011						
Access	R/W	R/W						

Name	Description	Notes
SAVE_IQQ	0 – Iqq = 45uA 1 – Iqq = 250uA	
VSET0 [6:0]	Buck2 output voltage setting in ACTIVE mode. 0.5V to 1.77V in 10mV steps	Controls the Buck2 output voltage. B2_VSET0 is used in ACTIVE mode. The output voltage is equal to VSET [6:0] * 0.01 + 0.5V.

B2_VSET01 – Buck2 Voltage Set1 Register

Address = 0x63h	Default = 0x19h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU	VSET0 [6:0]						
Default	0	0011001						
Access	R/O	R/W						

Name	Description	Notes
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET0 [6:0]	Buck2 output voltage setting in ACTIVE mode. 0.5V to 1.77V in 10mV steps	Controls the Buck2 output voltage. B2_VSET1 is used in ACTIVE mode. The output voltage is equal to VSET [6:0] * 0.01 + 0.5V.

B2_REG04 – Buck2 Configuration Register

Address = 0x64h	Default = 0xC2h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBIN_EN	QLTCH	SLEEP_EN	RFU	DPSLP_EN	ILIM_SET	FCCM
Default	1	1	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Buck2 is enabled through normal sequencing 1 – Buck2 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck2 shuts down when its sequenced input shuts down 1 – Buck2 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck2 stays on when the IC enters Sleep mode 1 – Buck2 turns off when the IC enters Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DPSLP_EN	0 – Buck2 stays on when the IC enters Deep Sleep mode 1 – Buck2 turns off when the IC enters Deep Sleep mode	
ILIM_SET	0 – Peak current limit set to 3.8A 1 – Peak current limit set to 5.0A	
FCCM	0 – Allows Buck2 to operate in both continuous conduction mode and LPM mode 1 – Force Buck2 to operate in continuous conduction mode.	

B2_REG05 – Buck2 Configuration Register

Address = 0x65h	Default = 0x88h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	0	001			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck2 does not affect nRESET output 1 – Buck2 turning off asserts nRESET output low	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B2_REG06 – Buck2 Configuration Register

Address = 0x66h	Default = 0x0Eh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST		DBSTBY [1:0]	
Default	0000				11		10	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SST	00 – 50us 01 – 100us 10 – 250us 11 – 500us	Soft-start time option
DBSTBY [1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B2_REG07 – Buck2 Configuration Register

Address = 0x67h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_LOAD[3:2]		ON_DELAY [2:0]			OFF_DELAY [2:0]		
Default	00		001			000		
Access	R/W		R/W			R/W		

Name	Description	Notes
IPD_LOAD[3:2]	Sets Buck2 pulldown load	See register 0x61h for details
ON_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the Buck2 enable input to when it turns on.
OFF_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the Buck2 disable input to when it turns off.

BUCK3 REGULATOR REGISTERS

B3_REG00 – Buck3 Configuration Register

Address = 0x80h	Default = 0x0Fh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	POK	OV	ILIM	RFU	UV_FLTMSK	OV_FLTMSK	ILIM_FLTMSK	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
POK	0 – Buck3 voltage is below the power good threshold 1 – Buck3 voltage is above the power good threshold	Provides real-time power good status
OV	0 – Buck3 voltage is below the overvoltage threshold 1 – Buck3 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It stays high until output voltage < OV and this bit is read.
ILIM	0 – Buck3 is below the ILIM threshold 1 – Buck3 is above the ILIM threshold	If the peak switch current reaches the ILIMSET threshold for 16 consecutive switching cycles, this bit goes high. It stays high until peak switch current < ILIMSET and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
UV_FLTMSK	0 – Unmasks the Buck3 POK signal 1 – Masks the Buck3 POK signal	When 1, the Buck3 POK signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is disabled or drops out of regulation. B3_POK still provides real-time power good status.
OV_FLTMSK	0 – Unmasks the Buck3 OV register 1 – Masks the Buck3 OV register	When 1, the Buck3 OV signal is masked and does not go to the master controller. This prevents Buck3 from asserting the nIRQ pin when it is above regulation limits. OV still provides OV status.
ILIM_FLTMSK	0 – Unmasks the Buck3 B3_ILIM register 1 – Masks the Buck3 B3_ILIM register	When 1, the B3_ILIM fault bit is masked from the master fault register. ILIM still provides current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

B3_REG01 – Buck3 Configuration Register

Address = 0x81h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	FREQ_SEL[1:0]		ENPD_LOAD	DIS_PULLDOWN	IPD_LOAD[1:0]		DRV_ADJ [1:0]	
Default	01		0	0	0		00	
Access	R/W		R/W	R/W	R/W		R/W	

Name	Description	Notes
FREQ_SEL[1:0]	00 – 1.5MHz 01 – 2.0MHz 10 – 2.5MHz 11 – 3.3MHz	
ENPD_LOAD	0 –Disable Buck3 pulldown load function 1 –Enable Buck3 pulldown load function	Enable Buck3 pull-down load when Buck3 is enabled. Registers 0x81[3:2] and 0x87[7:6] config the current load.
DIS_PULLDOWN	0 – Discharge VOUT when turn-off BUCK by 9.4Ohm 1 – Don't discharge VOUT when turn-off BUCK	Option disable Pull-Down Resistor when BUCK is turned-off
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
IPD_LOAD[1:0]	Sets Buck3 pulldown load	Combine with IPD_LOAD[3:2] bits in register 0x87h 0000 – 10mA 0001 – 13mA 0010 – 17mA 0011 – 20mA 0100 – 24mA 0101 – 27mA 0110 – 30mA 0111 – 34mA 1000 – 37mA 1001 – 40mA 1010 – 44mA 1011 – 47mA 1100 – 50mA 1101 – 54mA 1110 – 57mA 1111 – 60mA
DRV_ADJ [1:0]	00 – Slowest 11 – Fastest	Adjust Gate Driver (Rising and Falling SW)

B3_VSET00 – Buck3 Voltage Set0 Register

Address = 0x82h	Default = 0x8Dh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	SAVE_IQQ	RFU		VSET [4:0]				
Default	1	00		01101				
Access	RO	RO		R/W				

Name	Description	Notes
SAVE_IQQ	0 – Iqq=45uA 1 – Iqq=250uA	
RFU[1:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET0[4:0]	Buck3 output voltage setting in ACTIVE mode. 0.5V to 3.6V in 100mV steps.	Controls the Buck3 output voltage. VSET0 is used in ACTIVE mode. The output voltage is equal to VSET [4:0] * 0.1 + 0.5V

B3_VSET01 – Buck3 Voltage Set1 Register

Address = 0x83h	Default = 0x07h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	RFU [2:0]			VSET [4:0]				
Default	000			00111				
Access	R/O			R/W				

Name	Description	Notes
RFU [2:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
VSET0[4:0]	Buck3 output voltage setting in ACTIVE mode. 0.5V to 3.7V in 100mV steps	Controls the Buck3 output voltage. VSET0 is used in ACTIVE mode. The output voltage is equal to VSET [4:0] * 0.1 + 0.5V

B3_REG04 – Buck3 Configuration Register

Address = 0x84h	Default = 0x42h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	ON	PBIN_EN	QLTCH	SLEEP_EN	RFU	DPSLP_EN	ILIM_SET	FCCM
Default	0	1	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
ON	0 – Buck3 is enabled through normal sequencing 1 – Buck3 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
PBIN_EN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
QLTCH	0 – Buck3 shuts down when its sequenced input shuts down 1 – Buck3 stays on when its sequenced input shuts down	
SLEEP_EN	0 – Buck3 stays on when the IC enters Sleep mode 1 – Buck3 turns off when the IC enters Sleep mode	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
DPSLP_EN	0 – Buck3 stays on when the IC enters Deep Sleep mode 1 – Buck3 turns off when the IC enters Deep Sleep mode	
ILIM_SET	0 – Peak current limit set to 2.0A 1 – Peak current limit set to 3.0A	
FCCM	0 – Allows Buck3 to operate in both continuous conduction mode and LPM mode 1 – Force Buck3 to operate in continuous conduction mode.	

B3_REG05 – Buck3 Configuration Register

Address = 0x85h	Default = 0x898h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	MODE	RST	DBQL [2:0]			DBOK [2:0]		
Default	1	0	011			000		
Access	R/W	R/W	R/W			R/W		

Name	Description	Notes
MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RST	0 – Buck3 does not affect nRESET output 1 – Buck3 turning off asserts nRESET output low	
DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
DBOK [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B3_REG06 – Buck3 Configuration Register

Address = 0x86h	Default = 0x2Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	DBON [3:0]				SST[1:0]		DBSTBY [1:0]	
Default	0010				11		11	
Access	R/W				R/W		R/W	

Name	Description	Notes
DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
SST[1:0]	00 – 50us 01 – 100us 10 – 250us 11 – 500us	Soft-start time option
DBSTBY [1:0]	Determines DVS inputs from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

B3_REG07 – Buck3 Configuration Register

Address = 0x87h	Default = 0x08h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	IPD_LOAD[3:2]		ON_DELAY [2:0]			OFF_DELAY [2:0]		
Default	00		001			000		
Access	R/W		R/W			R/W		

Name	Description	Notes
IPD_LOAD_B3[3:2]	Sets Buck3 pulldown load	See register 0x81h for details
PHASE	0 – Aligns converter switching to the main clock rising edge 1 – Aligns converter switching to the main clock falling edge	
ON_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the Buck3 enable input to when it turns on.
OFF_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the Buck3 disable input to when it turns off.

LDO REGISTERS

LDO12_REG00 – LDO1 Configuration Register

Address = 0xA0h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO1_PWR_GOOD	LDO1_OV	LDO1_ILIM	RFU	LDO1_UV_FLTMSK	LDO1_OV_FLTMSK	LDO1_ILIM_FLTMSK	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	R/W	R/W	R/W	RO

Name	Description	Notes
LDO1_PWR_GOOD	0 – LDO1 voltage is below the power good threshold 1 – LDO1 voltage is above the power good threshold	Provides real-time power good status
LDO1_OV	0 – LDO1 voltage is below the overvoltage threshold 1 – LDO1voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It stays high until output voltage < OV and this bit is read.
LDO1_ILIM	0 – Output ILIM is not triggered 1 – Output ILIM is triggered	When output current reached ILIM setting, this bit goes high. It stays high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
LDO1_UV_FLTMSK	0 - Unmasks the LDO1 UV_LDO1 register 1 - Masks the LDO1 UV_LDO1 register	When 1, the UV_LDO1 fault bit is masked from the master UV fault register. UV_LDO1 still provides real-time current limit status.
LDO1_OV_FLTMSK	0 - Unmasks the LDO1 OV_LDO1 register 1 - Masks the LDO1 OV_LDO1 register	When 1, the OV_LDO1 fault bit is masked from the master OV fault register, MSTR05. OV_LDO1 still provides overvoltage status.
LDO1_ILIM_FLTMSK	0 - Unmasks the LDO1 ILIM interrupt 1 - Masks the LDO1 ILIM interrupt	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_VSET – LDO1 Voltage Set0 Register

Address = 0xA1h	Default = 0x3Fh	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B1_IPD_LOAD[1:0]		LDO1_VSET [5:0]					
Default	00		111111					
Access	R/W		R/W					

Name	Description	Notes
B1_IPD_LOAD[1:0]	Sets Buck1 pulldown load	Combine with IPD_LOAD[3:2] bits in register 0xA7h 0000 – 10mA 0001 – 13mA 0010 – 17mA 0011 – 20mA 0100 – 24mA 0101 – 27mA 0110 – 30mA 0111 – 34mA 1000 – 37mA 1001 – 40mA 1010 – 44mA 1011 – 47mA 1100 – 50mA 1101 – 54mA 1110 – 57mA 1111 – 60mA
LDO1_VSET [5:0]	LDO1 output voltage setting. 0.6V to 3.75V in 50mV steps	Controls the LDO1 output voltage. The LDO output voltage is equal to LDO1_VSET [5:0] * 0.05 + 0.6V

LDO12_REG02 – LDO1 Configuration Register

Address = 0xA2h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO1_ON	LDO1_PBIN_EN	RFU	LDO1_SLEEP_EN	LDO1_DPSLP_EN	LDO1_DBQL [2:0]		
Default	0	1	0	0	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
LDO1_ON	0 – LDO1 is enabled through normal sequencing 1 – LDO1 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
LDO1_PBIN_EN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
LDO1_SLEEP_EN	0 – LDO1 stays on when the IC enters Sleep mode 1 – LDO1 turns off when the IC enters Sleep mode	
LDO1_DPSLP_EN	0 – LDO1 stays on when the IC enters Deep Sleep mode 1 – LDO1 turns off when the IC enters Deep Sleep mode	
LDO1_DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG03 – LDO1 Configuration Register

Address = 0xA3h	Default = 0x02h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO1_ON_DELAY [2:0]			LDO1_OFF_DELAY [2:0]			LDO1_MODE	LDO1_RST
Default	000			000			1	0
Access	R/W			R/W				

Name	Description	Notes
LDO1_ON_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the LDO1 enable input to when it turns on.
LDO1_OFF_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the LDO1 disable input to when it turns off.
LDO1_MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
LDO1_RST	0 – LDO1 does not affect nRESET output 1 – LDO1 turning off asserts nRESET output low	

LDO12_REG04 – LDO1 Configuration Register

Address = 0xA4h	Default = 0x40h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO1_DBON [3:0]				LDO1_DBOK [3:0]			
Default	0100				0000			
Access	R/W				R/W			

Name	Description	Notes
LDO1_DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
LDO1_DBOK [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG05 – LDO1 Configuration Register

Address = 0xA5h	Default = 0x8Ch	Type n/a = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO1_ILIM _STDN_DIS	ENOV_ PLSW1	RFU	LDO1_DIS_PLDN	NLSW1_ILIM _SCL	LDO1_ILIM _SCL	LDO1_SST	LDO1_QLTCH
Default	1	0	0	0	1	1	0	0
Access	R/W	R/W	RO	R/W	R/W	R/W	R/W	R/W

Name	Description	Notes
LDO1_ILIM _STDN_DIS	0 – Enable LDO1 shutdown by current limit 1 – Disable LDO1 shutdown by current limit	
ENOV_PLSW1	0 – Disable OV protect in PLSW mode. 1 – Enable OV protect in PLSW mode.	
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
LDO1_DIS_PLDN	0 – Discharge LDO1 output by resistor when turn off 1 – Disable LDO1 output discharge by resistor when turn off	
NLSW1_ILIM_SCL	0 – 650mA 1 – 1110mA	Current limit setting for NLSW mode
LDO1_ILIM_SCL	0 – 400mA 1 – 500mA	Current limit setting for LDO/PLSW mode
LDO1_SST	0 – 200us 1 – 320us	LDO1 soft-start time
LDO1_QLTCH	0 – LDO1 shuts down when its sequenced input shuts down 1 – LDO1 stays on when its sequenced input shuts down	

LDO12_REG06 – LDO1 Configuration Register

Address = 0xA6h	Default = 0x0Eh	Type = Basic Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO2_PWR_GOOD	LDO2_OV	LDO2_ILIM	RFU	LDO2_UV_FLTMSK	LDO2_OV_FLTMSK	LDO2_ILIM_FLTMSK	RFU
Default	0	0	0	0	1	1	1	0
Access	RO	RO	RO	RO	RW	R/W	R/W	RO

Name	Description	Notes
LDO2_PWR_GOOD	0 – LDO2 voltage is below the power good threshold 1 – LDO2 voltage is above the power good threshold	Provides real-time power good status
LDO2_OV	0 – LDO2 voltage is below the overvoltage threshold 1 – LDO2 voltage is above the overvoltage threshold	When output voltage > OV, this bit goes high. It stays high until output voltage < OV and this bit is read.
LDO2_ILIM	0 – LDO2 is below the ILIM threshold 1 – LDO2 is above the ILIM threshold	When output current reached ILIM setting, this bit goes high. It stays high until output current < ILIM and this bit is read.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
LDO2_UV_FLTMSK	0 - Unmasks the LDO2 UV_LDO2 register 1 - Masks the LDO2 UV_LDO2 register	When 1, the UV_LDO2 fault bit is masked from the master UV fault register, MSTR06. UV_LDO2 still provides real-time current limit status.
LDO2_OV_FLTMSK	0 - Unmasks the LDO2 OV_LDO2 register 1 - Masks the LDO2 OV_LDO2 register	When 1, the OV_LDO2 fault bit is masked from the master OV fault register. OV_LDO2 still provides real-time overvoltage status.
LDO2_ILIM_FLTMSK	0 - Unmasks the LDO2 ILIM_LDO2 register 1 - Masks the LDO2 ILIM_LDO2 register	When 1, the ILIM_LDO2 fault bit is masked from the master ILIM fault register, MSTR04. ILIM_LDO2 still provides real-time current limit status.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

LDO12_VSET – LDO2 Voltage Set0 Register

Address = 0xA7h	Default = 0x18h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	B1_IPD_LOAD[3:2]		LDO2_VSET [5:0]					
Default	00		011000					
Access	R/W		R/W					

Name	Description	Notes
B1_IPD_LOAD [1:0]	Sets Buck1 pulldown load	See register 0xA1h for details
LDO2_VSET [5:0]	LDO2 output voltage setting. 0.6V to 3.75V in 50mV steps	Controls the LDO2 output voltage. The LDO output voltage is equal to LDO2_VSET [5:0] * 0.05 + 0.6V

LDO12_REG08 – LDO2 Configuration Register

Address = 0xA8h	Default = 0xC0h	Type = Factory Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO2_ON	EN_BYP_OV	RFU	LDO2_SLEEP_EN	LDO2_DPSLP_EN	LDO2_DBQL [2:0]		
Default	1	1	0	0	0	000		
Access	R/W	R/W	R/W	R/W	R/W	R/W		

Name	Description	Notes
LDO2_ON	0 – LDO2 is enabled through normal sequencing 1 – LDO2 is enabled via I2C that bypasses normal sequencing	This functionality is dependent on the overall IC configuration. Consult the factory for details.
LDO2_PBIN_EN	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
RFU	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
LDO2_SLEEP_EN	0 – LDO2 stays on when the IC enters Sleep mode 1 – LDO2 turns off when the IC enters Sleep mode	
LDO2_DPSLP_EN	0 – LDO2 stays on when the IC enters Deep Sleep mode 1 – LDO2 turns off when the IC enters Deep Sleep mode	
LDO2_DBQL [2:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG09 – LDO2 Configuration Register

Address = 0xA9h	Default = 0x03h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO2_ON_DELAY [2:0]			LDO2_OFF_DELAY [2:0]			LDO2_MODE	LDO2_RST
Default	000			000			1	1
Access	R/W			R/W			R/W	R/W

Name	Description	Notes
LDO2_ON_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the LDO2 enable input to when it turns on.
LDO2_OFF_DELAY [2:0]	000 – 0ms 001 – 0.5ms 010 – 1ms 011 – 2ms 100 – 4ms 101 – 8ms 110 – 16ms 111 – 32ms	Sets the delay time between the LDO2 disable input to when it turns off.
LDO2_MODE	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
LDO2_RST	0 – LDO2 does not affect nRESET output 1 – LDO2 turning off asserts nRESET output low	

LDO12_REG0A – LDO2 Configuration Register

Address = 0xAAh	Default = 0x01h	Type = Basic Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO2_DBON [3:0]				LDO2_DBOK [3:0]			
Default	0000				0001			
Access	R/W				R/W			

Name	Description	Notes
LDO2_DBON [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.
LDO2_DBOK [3:0]	Determines startup sequencing from the CMI code	This is a factory expert bit that should not be changed. Modifying this bit may result in unexpected IC behavior.

LDO12_REG0B – LDO2 Configuration Register

Address = 0xABh	Default = 0x84h	Type = Factory Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO2_ILIM _STDN_DIS	RFU [2:0]		LDO2_DIS_PLDN	RFU	LDO2_ILIM _SCL	LDO2_SST	LDO2_QLTCH
Default	1	00		0	0	1	0	0
Access	R/W	RO		R/W	RO	R/W	R/W	R/W

Name	Description	Notes
LDO2_ILIM _STDN_DIS	0 – Enable LDO2 shutdown by current limit 1 – Disable LDO2 shutdown by current limit	
RFU [2:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.
LDO2_DIS_PLDN	0 – Discharge LDO2 output by resistor when turn off 1 – Disable LDO2 output discharge by resistor when turn off	
RFU	Reserved for Future Use	
LDO2_ILIM_SCL	0 – 400mA 1 – 500mA	Current limit setting for LDO/PLSW mode
LDO2_SST	0 – 200us 1 – 320us	LDO2 soft-start time
LDO2_QLTCH	0 – LDO2 shuts down when its sequenced input shuts down 1 – LDO2 stays on when its sequenced input shuts down	

LDO12_REG0D – LDO1 Configuration Register

Address = 0xADh	Default = 0x80h	Type = Factory Non-Volatile

BIT	7	6	5	4	3	2	1	0
Name	LDO1_MODE_SEL		RFU					
Default	10		000000					
Access	RO		RO					

Name	Description	Notes
LDO1_MODE_SEL	00 – LDO mode 01 – PLSW (Pch Load Switch) Mode 10 – NLSW (Nch Load Switch) Mode 11 – PLSW + NLSW Mode	
RFU[5:0]	Reserved for Future Use	Do not change this register value. Changing the register value can affect IC functionality.

ACT88321 vs ACT88329 Registers

The ACT88321 IC is a subset of the ACT88329 functionality. The differences between the two ICs are that the ACT88321 does not support GPIO1, GPIO3, or GPIO6. The registers for these GPIOs are available in the IC but have no effective functionality.

References

The following data sheets can be used as references for details for electrical parameters and available configuration settings and values.

1. *ACT88329 Datasheet*