N-Channel 100-V (D-S) MOSFET

Key Features:

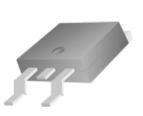
- Low r_{DS(on)} trench technology
- · Low thermal impedance
- · Fast switching speed

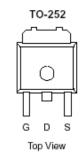
Typica	l Appl	ications:
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- White LED boost converters
- Automotive Systems
- Industrial DC/DC Conversion Circuits

PRODUCT SUMMARY			
V _{DS} (V)	$r_{DS(on)}(m\Omega)$	I _□ (A)	
100	28 @ V _{GS} = 10V	34.6	
	$30 @ V_{GS} = 4.5V$	33.4	







ABSOLUTE MAXIMUM RATINGS ($T_A = 25^{\circ}$ C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	Limit	Units	
Drain-Source Voltage		V_{DS}	100	V	
Gate-Source Voltage			±20	V	
Continuous Drain Current a	T _C =25°C	I_D	34.6	Α	
Pulsed Drain Current ^b		I _{DM}	160	A	
Continuous Source Current (Diode Conduction) a			2.1	Α	
Power Dissipation ^a	T _C =25°C	P_{D}	50	W	
Operating Junction and Storage Temperature Range	_	T_J, T_{stg}	-55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Maximum	Units		
Maximum Junction-to-Ambient ^a	$R_{\theta JA}$	40	°C/W		
Maximum Junction-to-Case	$R_{\theta JC}$	3	C/VV		

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Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
- b. Pulse width limited by maximum junction temperature

Electrical Characteristics

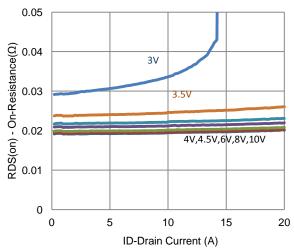
Parameter	Symbol	Test Conditions	Min	Тур	Max	Unit	
Static							
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250 \text{ uA}$	1			V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			±100	nA	
Zero Gate Voltage Drain Current	lana	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	uA	
Zelo Gate Voltage Brain Gurrent	I _{DSS}	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55^{\circ}\text{C}$			10	uA	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} = 5 \text{ V}, V_{GS} = 10 \text{ V}$	51.9			Α	
Drain Cauras On Basistanas a	r	$V_{GS} = 10 \text{ V}, I_{D} = 20 \text{ A}$			28	mΩ	
Drain-Source On-Resistance ^a	r _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 18 \text{ A}$			30	11122	
Forward Transconductance a	g _{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 20 \text{ A}$		57		S	
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.05 \text{ A}, V_{GS} = 0 \text{ V}$		0.75		V	
	Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = 40 \text{ V}, V_{GS} = 4.5 \text{ V},$		10			
Gate-Source Charge	Q_{gs}	$I_D = 2 A$		3.5		nC	
Gate-Drain Charge	Q_gd	10 - 2 A		3.1			
Turn-On Delay Time	t _{d(on)}	$V_{DS} = 40 \text{ V}, R_{L} = 20 \Omega,$		11			
Rise Time	t _r	$V_{DS} = 40 \text{ V}, R_L - 20 \Omega,$ $I_D = 2 \text{ A},$		9		no	
Turn-Off Delay Time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_{GEN} = 6 \Omega$		98		ns	
Fall Time	t _f	V GEN = 10 V, 1 (GEN = 0.22		23			
Input Capacitance	C _{iss}	_		4081			
Output Capacitance	C _{oss}	$V_{DS} = 20 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ Mhz}$		142		pF	
Reverse Transfer Capacitance	C_{rss}			114			

Notes

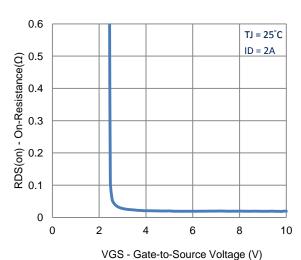
- a. Pulse test: PW <= 300us duty cycle <= 2%.
- b. Guaranteed by design, not subject to production testing.

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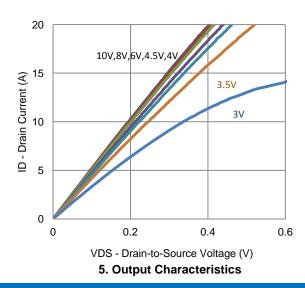
Typical Electrical Characteristics

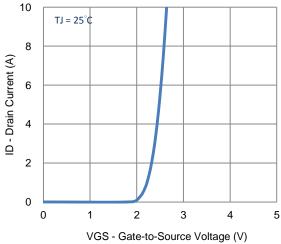


1. On-Resistance vs. Drain Current

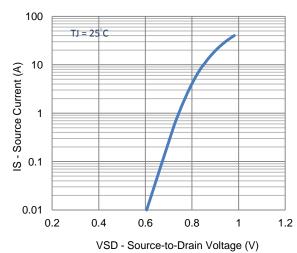


3. On-Resistance vs. Gate-to-Source Voltage

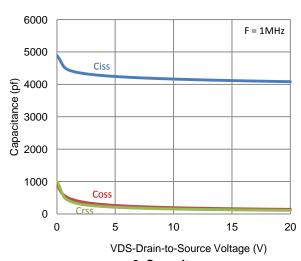




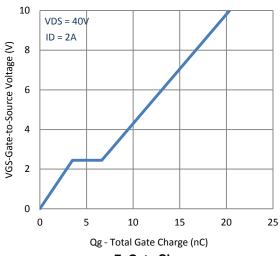
2. Transfer Characteristics



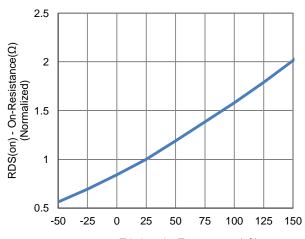
4. Drain-to-Source Forward Voltage



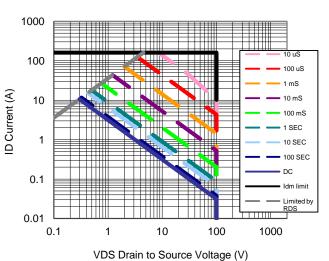
Typical Electrical Characteristics



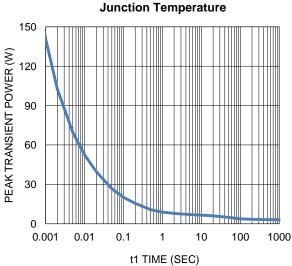
7. Gate Charge



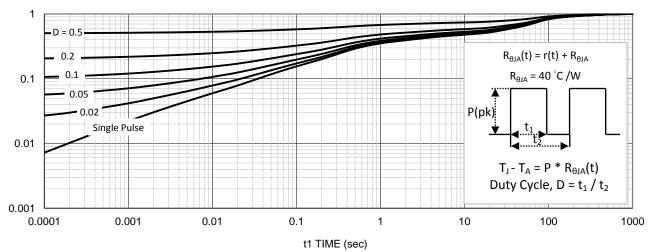
TJ -JunctionTemperature(°C)
8. Normalized On-Resistance Vs



9. Safe Operating Area

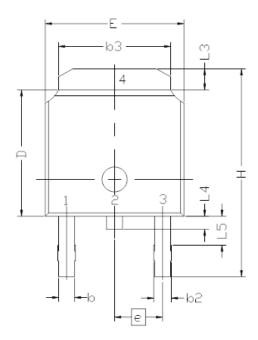


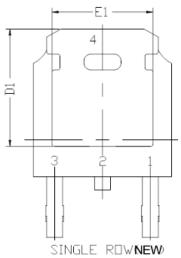
10. Single Pulse Maximum Power Dissipation

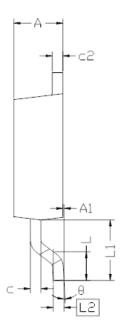


11. Normalized Thermal Transient Junction to Ambient

Package Information







CVADEL	DIMENS:	IONAL F	REQMTS
SYMBOL	MIN	NDM	MAX
E	6.40	6.60	6.731
L	1.40	1.52	1.77
L1		.743 RI	
L2		.508 BS	_
L3	0.89		1.27
L4	0.64		1.01
L5			
D	6.00	6.10	6,223
Н	9.40	10.00	10.40
b	0.64	0.76	0,88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
е	2.	286 BS	C
Α	2,20	2.30	2,38
A1	0		0.127
	0.45	0.50	0.60
c2	0.45	0.50	0.58
D1	5,30		
E1	4.40		
θ	0°		10°

Note:

- 1. All Dimension Are In mm.
- 2. Package Body Sizes Exclude Mold Flash, Protrusion Or Gate Burrs. Mold Flash, Protrusion Or Gate Burrs Shall Not Exceed 0.10 mm Per Side.
- 3. Package Body Sizes Determined At The Outermost Extremes Of The Plastic Body Exclusive Of Mold Flash, Gate Burrs And Interlead Flash, But Including Any Mismatch Between The Top And Bottom Of The Plastic Body.