Adaptive Multi-Rail Power Platform B – AmP

AmP8DB6

Product Description

The AmP™ device is an FPGA based platform for creating a custom Power Management Integrated Circuit (PMIC). The AmP device is customized by adding available Power Components designs based on system requirements. AmP device customization is as easy as using WebAmp™ application software to produce a customized PMIC in a very short period of time. AmP devices can be used to power FPGAs, Processors, Microcontrollers, and ASICs by integrating multiple power rails into single chip designs. The AmP device input voltage range is 4.5V to 20V. The AmP device is targeted for wall-powered applications or 2S-4S Li-Ion battery packs. AmP devices have up to 4 additional integrated LDOs of which two are fixed output voltages (3.3V and 1.2V) and two are user programmable.

Features

- Platform_B incorporates several improvements over previous generation platform including:
  - Extended Vin range to minimum 4.5 V
  - Increased Efficiency up to 4% better than Platform A
  - Dynamic enable/disable of user programmable LDOs
  - Better resource utilization
  - Extended voltage reference range
  - Improved accuracy, ripple, and noise rejection
  - Reduced BoM
- Integrate application targeted Power Components
- Power Blocks for a variety of topologies
  - Scalable Integrated N-channel MOSFETs (SIM)
  - Current sense for protection, telemetry, regulation
  - Build Switching topologies - Buck, Boost, Buck-Boost
  - Build Linear topologies - LDO, Load Switch
  - Build Mixed topologies - Battery Charger
  - Build BLDC (Motor Control) topologies – H-Bridge
- Sensor Blocks, sensing voltages and currents
  - Regulation, protection and telemetry
  - Adaptive Digitizer (ADi)
  - Threshold Comparators (ThC)
  - Summation Amplifier (SuM)
  - Voltage Reference (Nref) Array
- Analog fabric connectivity for sensor signals
- Digital µLogic fabric connectivity: Analog/Digital Blocks
- Industry first: Analog Proficiency – Digital Flexibility

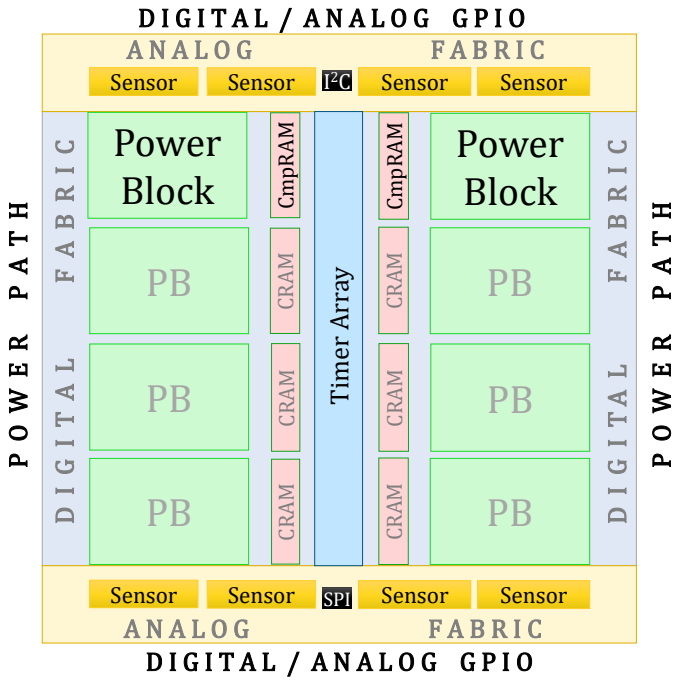
AmP Family

- 12 V platform family
  - Eight Power & Sensor Blocks
  - Up to eight switcher or linear rails
  - 6A per DMOS MOSFETs; RDSon 30mΩ
  - Analog or Digital I/Os: 23
  - Package: QFN 5x5 sq. mm
- Standard BCD process: 110nm, V_{DS}max 20V

AmP DMOS Platform

Power Blocks	GPIOs	Device
Eight	23	AmP8DB6

Adaptive Multi-Rail Power Platform – AmP



Applications

Power Component Integrator

- Build Buck, Boost, Buck-Boost POL topologies
- PWM – CV/CC, voltage mode or current mode
- COT – Constant-On-Time
- Load Switch, LDO - Source/Drain, DDR LDO
- External Switching Controllers/Gate Drivers
- Peak efficiency > 92%, Soft start/stop

Digital power management IC

- Monitor and throttle/margin power rails
- Power ON/OFF/Sequence power rails
- I^2C, PMBus, DVS for Telemetry and control
- Protection: On-demand OCP, OVP, OTP, UVLO

AmP8DB6 Platform Features

Device			8DBx6
Drain Current			6A
Power Blocks			8
Sensor Blocks			8
Nrefs			24
Timers			16
Integrated LDOs			4
µLogic Fabric LUTs			512
Package			GPIOs
QF65	5x5mm	8D MOSFETs	23

*T_A: -40C to 85C, T_J: -40C to 125C;

Order Information

Platform	MOSFETs	Technology	Current – A	Package	Ordering Part Number	Availability
AmP	8	D	6	QF65	AmP8DB6QF65	Now

Package Marking Example – QF65

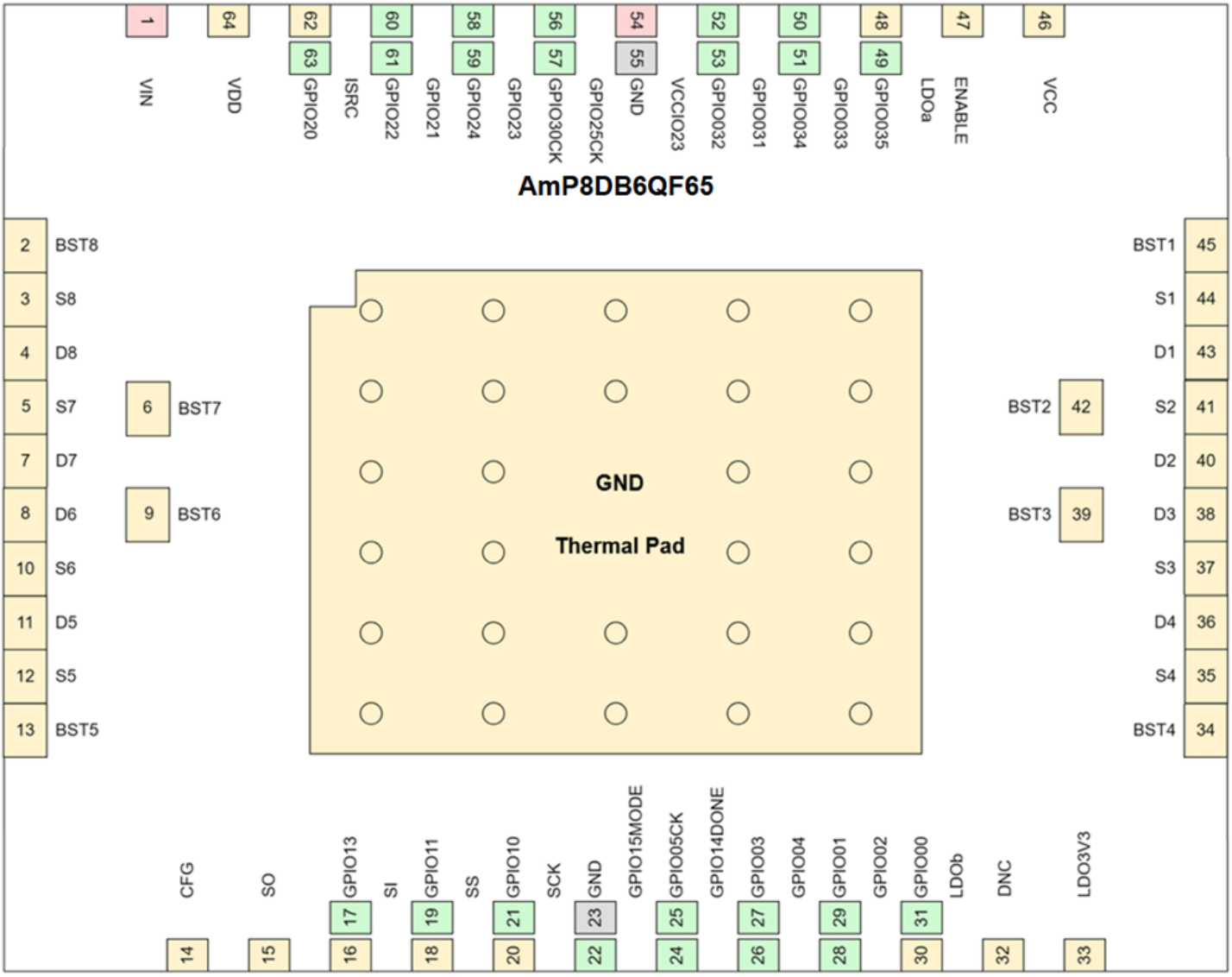
Package Configuration

Top View (Pin and Thermal Pads are on bottom side)

AmP8DB6

QF65

5X5 mm



Pin Configurations

Name	QF65	Function
BST1	45	Boost
S1	44	Source
D1	43	Drain
BST2	42	Boost
S2	41	Source
D2	40	Drain
BST3	39	Boost
D3	38	Drain
S3	37	Source
BST4	34	Boost
D4	36	Drain
S4	35	Source
LDO3V3	33	LDO 3.3 V
DNC	32	DNC
LDOb	30	LDO Prog.
GPIO00	31	GPIO
GPIO01	29	GPIO
GPIO02	28	GPIO
GPIO03	27	GPIO
GPIO04	26	GPIO
GPIO05CK	25	GPIOCK
GND	23	GND
GPIO10	21	GPIO
GPIO11	19	GPIO
GPIO13	17	GPIO
GPIO14DONE	24	GPIODONE
GPIO15MODE	22	GPIOMODE
SCK	20	SPI clock
SS	18	SPI select
SI	16	SPI serial in
SO	15	SPI serial out
CFG	14	Configuration

Name	QF65	Function
S5	12	Source
D5	11	Drain
BST5	13	Boost
S6	10	Source
D6	8	Drain
BST6	9	Boost
D7	7	Drain
S7	5	Source
BST7	6	Boost
D8	4	Drain
S8	3	Source
BST8	2	Boost
ISRC	62	Prog. Cur. Src.
VIN	1	Supply
VDD	64	LDO 4.5V
VCCIO23	54	IO bank supply
GPIO20	63	GPIO
GPIO21	60	GPIO
GPIO22	61	GPIO
GPIO23	58	GPIO
GPIO24	59	GPIO
GPIO25CK	56	GPIOCK
GND	55	GND
GPIO30CK	57	GPIOCK
GPIO31	52	GPIO
GPIO32	53	GPIO
GPIO33	50	GPIO
GPIO34	51	GPIO
GPIO35	49	GPIO
LDOa	48	LDO, prog.
VCC	46	LDO, 1.2 V
ENABLE	47	Enable AmP
GND	65	GND Thermal Pad

Pin Function and Description

Function	Description
Boost	Bootstrap pin for MOSFET gate drive
Drain	MOSFET drain
Source	MOSFET source
GND	Digital ground Analog ground, thermal pad
LDO 3.3V	LDO output 3.3V
DNC	Do not connect, floating
LDO Prog.	LDO output voltage programmable
IO bank supply	Supply input to GPIO bank
GPIO	General purpose input-output
GPIOCK	GPIO shared with input low skew global clock driver to digital fabric
GPIODONE	GPIO shared with DONE output
GPIOMODE	Dual function: Before config, pin in Mode function; after config, pin in Sequencer function. Mode function: Host ROM or Flash mode: connect high through 47kΩ resistor. Client AmPLink or external controller: connect low through 47kΩ resistor. Sequencer function: Output from Sequence 3. Connect to relevant Buck EN pin to be the third in sequence. Do not leave floating.
SPI clock	SLK output clock when AmP is Host, input clock when AmP is Client
SPI select	SS output Client select when AmP is Host, input when AmP is Client
SPI serial in	SI input receives SPI data
SPI serial out	SO output transmits SPI commands
Configuration	CFG input active high configuration restart. AmP is held in reset while signal is high. Reconfiguration is triggered on negative edge.
Prog. Cur. Src.	Programmable current source
Supply	Vin bias supply for, VDD, VCC, LDO3V3, LDOa, LDOb
LDO 4.5V	VDD LDO 4.5V output
LDO 1.2V	VCC, LDO 1.2V output
Enable AmP	AmP Platform powered on when floating, powered down when pulled low.

Global Input Under Voltage (ViUVLO)

To protect system operation when any input voltage goes below the AmP device operating voltage (4.5V), the Global Input Under Voltage (ViUVLO) will be set based on all the individual power component ViUVLOs. When any power component ViUVLO goes high, all the power components will power down, until Global ViUVLO goes low, then power components will power up. When there are multiple power components in the design, the Global ViUVLO set closest to 4.1 V AND higher than 4.1V is used to power down.

If no Power Component ViUVLO is set or is not higher than 4.1V the Global ViUVLO will be disabled. To ensure graceful startup and shutdown, in Single Supply Configuration, it is recommended that at least one power component has its ViUVLO feature set and higher than 4.1V.

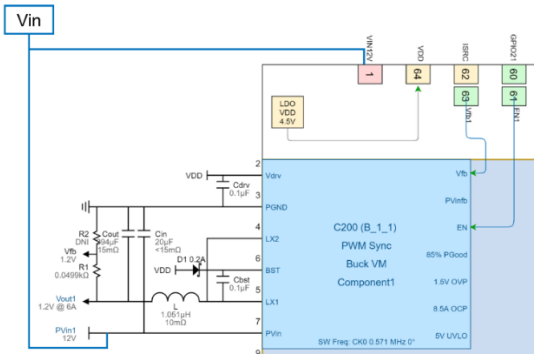
Vin and PVin Requirements

Minimum Vin and PVin requirements are as follows:

AmP pin	Single Supply	Separate Supplies
Bias Supply	Vin ≥ 4.5V	Vin ≥ 4.5V
Power Stage	PVin ≥ 4.5V	PVin ≥ 3.0V

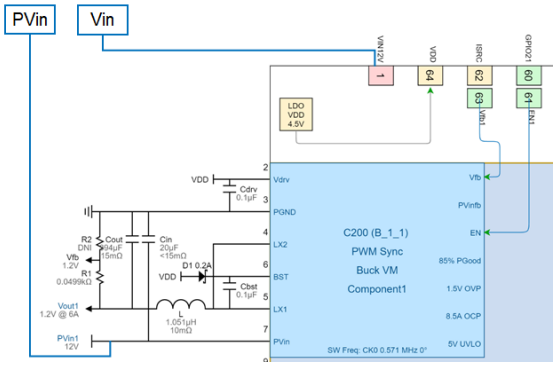
Single Supply Example

Vin and Pvin tied together requires ViUVLO ≥ 4.1V.



Separate Supply Example

Vin separate from Pvin requires ViUVLO ≥ 2.6V.



Over Temperature Protection (OTP)

The AmP Platform has an integrated temperature sensor for over temperature monitoring and protection. For system safety, the AmP platform will shut down if the device junction temperature goes over the OTP set limit. The OTP limit is set at 150°C. This will shut down all the power rails.

The enable (EN) pins of each power component are routed through the OTP fuse module. If the design includes a sequencer and enable pins are connected to the sequencer, the sequencer "On" input is routed through OTP fuse module. When the temperature reaches the OTP set limit, the OTP flag goes high and all EN pins that are routed through OTP fuse module will be pulled low. After cooling down, the OTP flag will go low and each Power Component EN or sequencer "On" pin needs to be triggered by a rising edge on that input pin. The system can be brought back up without reprogramming of the AmP device. There will be no chattering of operation mode when the temperature hovers around the OTP limit. If your system requires a lower temperature setting please contact factory. Also, if your system requires a temperature warning prior to reaching over temperature shut down, please contact your application and sales team.

Internal Clock

The Amp Platform has two integrated clocks which operate independently and have a programmable frequency of up to 64MHz. These clocks can be divided down to a lower frequency range of 62.5KHz to 32MHz. WebAmp tools provide clock frequency selection. The power component frequency can be selected separately by using WebAmp Tools. Clock frequencies of 4MHz or lower are recommended for the current power components. In addition, an external clock can be used with the AmP platform. The external oscillator can be connected to any of the GPIO pins. GPIOCK pins are recommended for oscillator connections to have higher performance.

Integrated LDO

The Amp Platform has 4 integrated LDOs of which two are fixed output voltages (3.3V and 1.2V) and two are user programmable. The user programmable LDOs can be customized by using WebAmP Tools. The user programmable LDOs can be dynamically enabled/disabled from the digital fabric, allowing sequencing and external control. The input voltage to the four LDO's is from the internal 4.5V bias voltage. The pin locations of these integrated LDOs, are fixed and cannot be modified by WebAmP Tools. The 3.3V output is pin 33 of the QF65 package. The 1.2V LDO is connected to pin 46 of the QF65 package. The other two programable LDO outputs are pins 30 and 48 respectively in the QF65 package. Please see table below for electrical characteristics of these LDOs.

Integrated LDO

Symbol	Parameter	Condition	Min	Typ	Max	Unit
LDO1V2	LDO 1.2V output voltage	I_{CC}=0mA, V_{IN}=4.5V	1.164	1.2	1.236	V
	LDO 1.2V load regulation	I_{CC}=200mA, V_{IN}=4.5V		1.1		V
I_{CC}	LDO 1.2V output current**				200	mA
LDO3V3	LDO 3.3V output voltage	I3V3=0mA,V_{IN}=4.5V	3.201	3.3	3.399	V
	LDO 3.3V load regulation	I3V3=200mA,V_{IN}=4.5V		3.2		V
I3V3	LDO 3.3V output current**				200	mA
LDOa	LDOa Programmable range		0		V_{DD}	V
	LDOa load regulation	Ia=200mA, V_{IN}=4.5V		Vnom-0.1		V
	LDOa tolerance	Ia=0mA, V_{IN}=4.5V	-3		+3	%Vnom
Ia	LDOa output current**				200	mA
LDOb	LDOb Programmable range		0		V_{DD}	V
	LDOb load regulation	Ib=200mA, V_{IN}=4.5V		Vnom-0.1		V
	LDOb tolerance	Ib=0mA, V_{IN}=4.5V	-3		+3	%Vnom
Ib	LDOb output current**				200	mA

**Total LDO power dissipation must not exceed Package Dissipation Ratings. VIN supplies VDD LDO which supplies sub LDOs VCC, LDO3V3, LDOa and LDOb. VDD pin requires >10µF external decoupling and is for internal use only.

Absolute Maximum Ratings*

		Min	Max	Unit
Drain to Source Voltage		-1	22	V
V_{IN} Bias Supply		-1	22	V
Boost Voltage, referenced to Source		-1	6.6	V
Continuous Drain Current	Package power dissipation may limit current		8	A
Temperature range	Junction temperature, $T_{J(max)}$		150	°C
	Storage temperature range, T_{stg}	–65	150	

* Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ESD Ratings

		Value	Unit
Electrostatic Discharge	Human body model	±2000	V
	Charged device model	±500	V

Thermal Information

Symbol	Thermal Metric	QF65	Unit
$\theta_{JA(effective)}$	Effective Junction-to-ambient thermal resistance (System Level)*	20	°C/W
	Package Manufacturer ratings (JEDEC reference)		
θ_{JC}	Junction-to-case (top) thermal resistance	11	°C/W
θ_{JB}	Junction-to-board thermal resistance	9	°C/W

*$\theta_{JA\{effective\}}$ measured on AnDAPT AnD8400EB Evaluation Board and AmP8DB1 REV5.0 Demonstration Board

Package Dissipation Ratings

Package	$\Theta_{JA(effective)}$	T_A = 55°C Power Rating (W) Still air flow	T_A = 55°C Power Rating (W) 200 LFM air flow	T_A = 55°C Power Rating (W) 400 LFM air flow
QF65	20	3.5	3.8	4.1

Recommended Operating Conditions

		Min	Typ	Max	Unit
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

Electrical Characteristics

V_{IN}=V_{DS}=12V, T_A=25°C, Cvdd=10µF, Cvcc=1µF, Cldo3v3=1µF, Cldoa=1µF and Cldob=1µF unless otherwise specified

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DS}	Drain to Source Voltage N-channel		-0.3		20	V
R_{DS}(on)	Drain to Source On Resistance			30		mΩ
I_{Lmax}	Load Current Maximum		6			A
V_{IN}	Bias Supply		4.5		20*	V
V_{IN} **ramp** rate	Slew rate limit of bias supply				10**	V/ms
I_Q	Input Shutdown Current (V_{IN})	V_{IN} = 12V, No configuration		1.1		mA
$V_{CCIO\ 0,\ 1,\ 2,\ 3}$	I/O Bank Supply		1.71		5.5	V
I_{SRC}	Current Source Programmable range		0		100	mA
	ISRC Programmable tolerance		-8		+8	%Inom

Note: *For Vin>14V an external 5V power rail needs to be connected to LDO 4.5V. The external power rail minimum current capability needs to be 100mA plus the current consumption of the Integrated LDOs. Contact factory for alternative solutions.
Note: **Ensure monotonic startup of bias supply. Example case: for bias supply, Vin = 12V, ramp rate should be limited to 10V/ms or maximum Vin rise time should be 1.2 ms.

Analog GPIO Electrical Characteristics

V_{IN} =12V and T_A=25°C

Symbol	Parameter	Min	Typ	Max	Unit
Ipup80	Programmable Pullup Current Source*		78		µA
Ipup100	Programmable Pullup Current Source*		104		µA
Ipup150	Programmable Pullup Current Source*		156		µA
R_{PDOWN}	Programmable Weak Pull Down Resistance		5.1		kΩ
C_{PIN}	Pin Capacitance		8		pF
I_{IN}	GPIO Input leakage current		±5		µA

Note: All TBD pending characterization. *USB Type-C CC configuration channel logic enables Ipup80 for Default (80 µA), Ipup80 + Ipup100 for Medium(180 µA) and Ipup80 + Ipup100 + Ipup150 for High(330 µA).

Digital GPIO Electrical Characteristics

V_{IN}=12V and T_A=25°C

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3 V	3.14	3.3	3.46	-0.3	0.8	2.0	V_{CCIO} + 0.2	0.4	V_{CCIO} – 0.5	2	-2
2.5 V	2.37	2.5	2.62	-0.3	0.7	1.7	V_{CCIO} + 0.2	0.4	V_{CCIO} – 0.5	1.5	-1.5
1.8 V	1.71	1.8	1.89	-0.3	0.35*V_{CCIO}	0.65*V_{CCIO}	V_{CCIO} + 0.2	0.4	V_{CCIO} – 0.4	1	-1

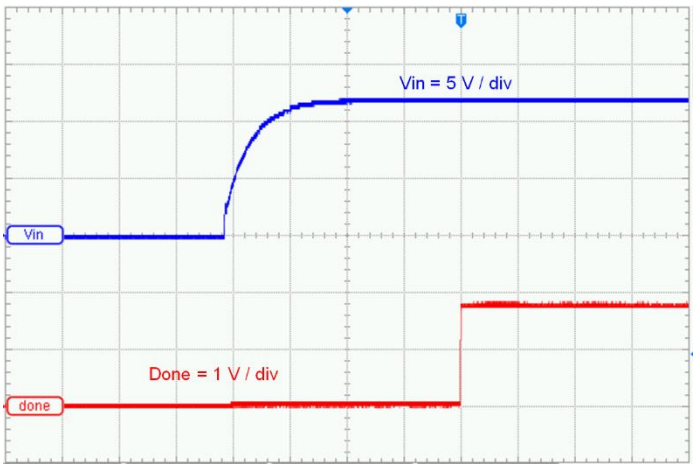
AmP Configuration

The AmP devices store a user design configuration within internal volatile memory. Once the power is removed, the user design configuration is lost and must be reloaded on the next power-up. This behavior provides the most flexible means of configuring an AmP device throughout a product development lifecycle. Re-configuration of the design can happen throughout product development experimentation cycles and can extend to configuration changes that can be provided to products that are already deployed in the field. This flexibility benefit requires storage of the configuration information in a non-volatile device which is loaded onto the AmP device upon power up. An external SPI Flash can serve this purpose when the AmP device is in Host Mode. In Client Mode, the AmP device can be configured by a digital processor through an SPI interface. Additionally, static configurations can be programmed into the device at the factory for customized customer orders. Factory customized device configuration can be modified by using external flash if required.

The AmP platform supports two modes of configuration through the SPI compliant serial interface. In Host mode, the AmP device loads its configuration bitfile (.HEX) from an external non-volatile memory or internal customized ROM. In Client mode, the AmP device is loaded with its configuration bitfile (.HAX) by an external controller or AmPLink™ USB Adapter. The (.HAX) file format is AnDAPT internal format.

AmP SPI Host Configuration Interface

The AmP device simply receives valid input power and takes control of the external FLASH memory to load its configuration. The AmP device acts as the SPI Host and controls the external FLASH memory as a Client. Host mode is ideally suited for applications where the AmP device is independently providing FLASH power (shown below). For a factory customized device, if the AmP device cannot access external flash, it will load from internal customized ROM. External flash then, can be used to modify the factory customized device.



Time = 5 ms / div

AmP SPI Client Configuration Interface

An external controller/AmPLink acts as the SPI bus Host and drives the AmP device as a Client. Configuration data for the device is provided over a sequence of SPI commands. Client mode is ideally suited for applications where the AmP device is configured by a processor.

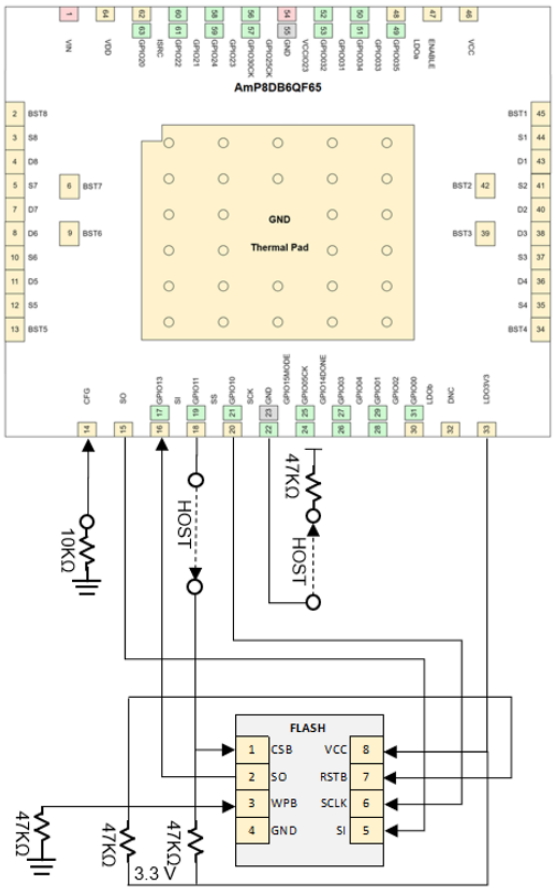
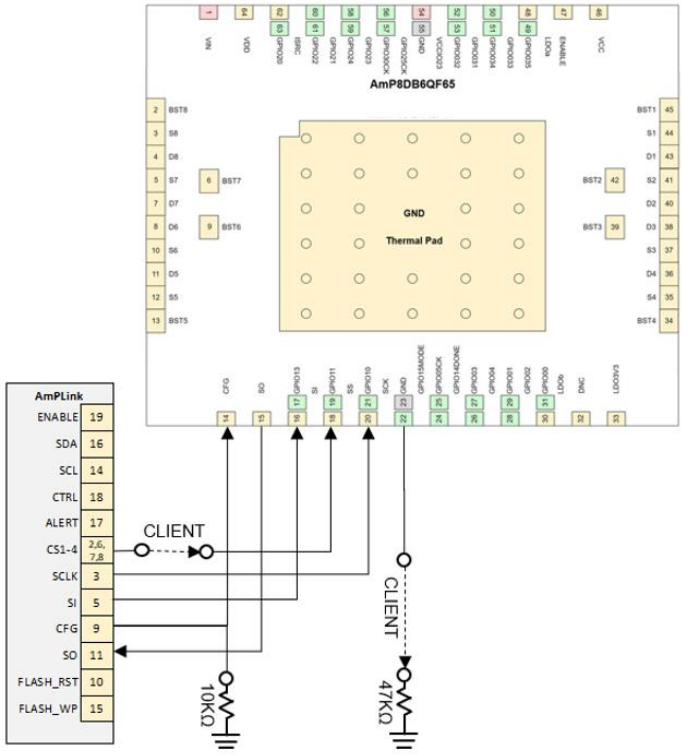
AmPLink and WebAmP

The AmPLink USB Adapter provides the interface between the AmP8DB2 Demonstration Board and the WebAmP design tool to program and control AmP and FLASH memory devices using SPI, I^2C and GPIO interfaces. The I^2C bus provides control and monitoring of the power supply functions of the AmP device, independent of configuration method.

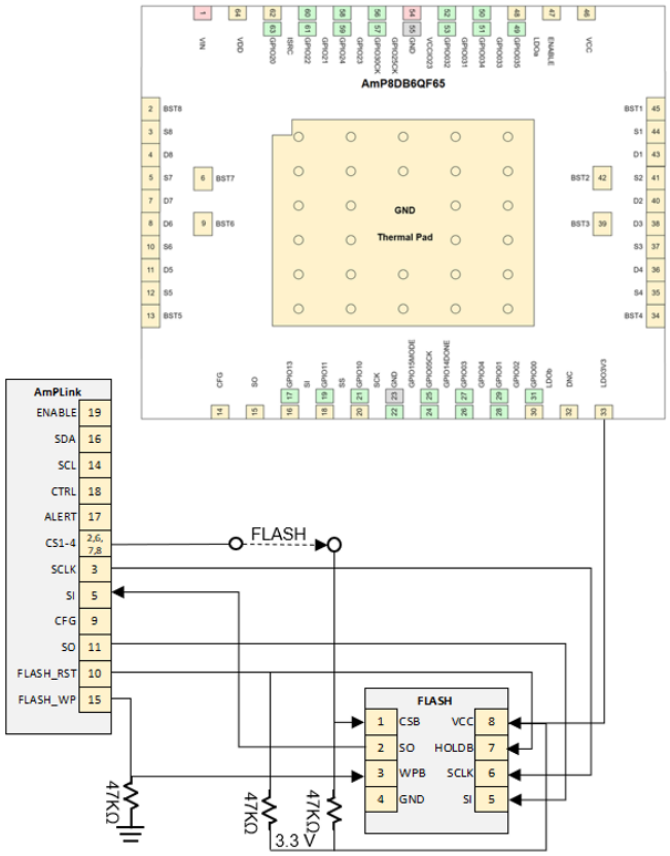
AmP Configuration Times

$V_{IN}=V_{DS}=12V$, $T_A=25°C$

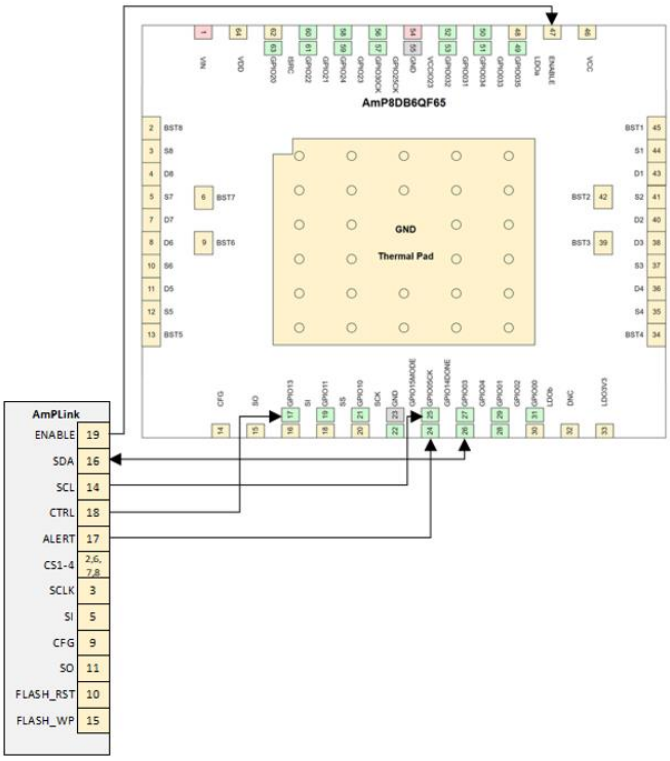
AmP SPI Configuration	Typ	Max	Unit
Host Interface, Flash memory	20	25	ms
Host Interface, internal factory customized ROM	3	4	ms
Client Interface @ SCK = 10MHz	25		ms

SPI Host	SPI Client
	

Programing FLASH by AmpLink

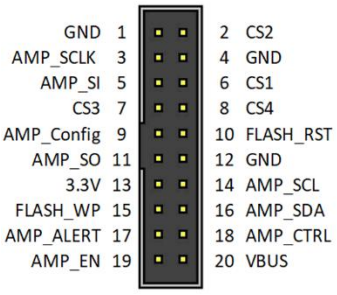


AmpLink Communication using I²C



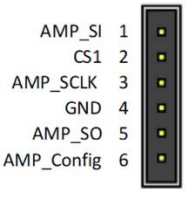
AmPLink Pin Out

20-Pin



Pin 13 should not be connected to LDO3V3

6-Pin



AmPLink Pin Functional Description

FLASH Program / AmP Configuration	AmP	ENABLE	High(float): AmP power on, Low: AmP power off
		CFG	High: config reset, High-to-Low: start config
	SPI	SCLK	Clock output, Hi-Z when not in use
		SI	MOSI output when connecting to AmP devices MISO input when programming flash devices Hi-Z when not in use
		SO	MISO input when connecting to AmP devices MOSI output when programming flash devices Hi-Z when not in use
		SS	Active low chip select enables AmP
	CS	CS1, CS2, CS3, CS4	Active low chip selects connect to AmP SS or FLASH CS Hi-Z when not in use
	FLASH	FLASH_WP	Flash write protect output
		FLASH_RST	Flash reset output
I²C	AmP GPIOs	SCL	Clock output. Open drain with internal 2.2kΩ pull up resistor
		SDA	Bidirectional data line. Open drain with internal 2.2kΩ pull up resistor
		ALERT	alert signal input
		CTRL	control signal output
	Power	GND	Connected to USB GND and shield
		VBUS	5V output 0.5A to 0.7A current limiting
		3.3V	3.3V output with 0.5A current limiting

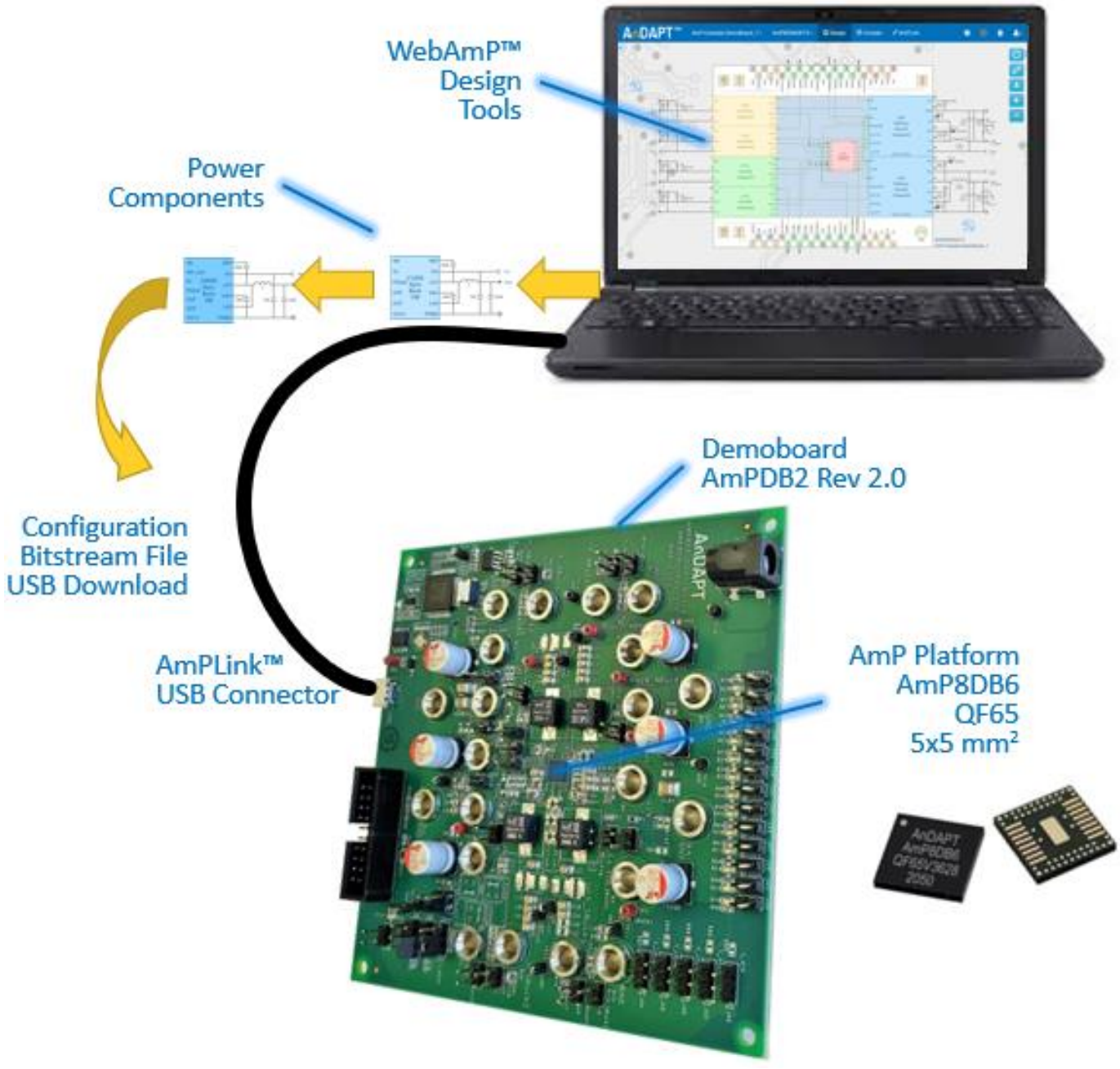
WebAmP Tools

WebAmP™ cloud-based tools enable users to select, integrate, optimize, and manage power components for AmP platforms. Users can select, integrate, optimize, and download on-demand power management devices utilizing an ever-growing library of AmP™ Power Components. The graphical tool is easy-to-use, and provides the capability to integrate, optimize and tune the power components for LC, stability, PID, transient response, efficiency, startup/shutdown, and protection characteristics. Once the design is complete, users simply download the compiled designs to an AmP platform using an AmPLink USB adapter to build a custom PMIC in minutes. WebAmP tools come complete with a suite of Power Analysis modules that enable users to optimize AmP designs. The analysis tools include the following functions.

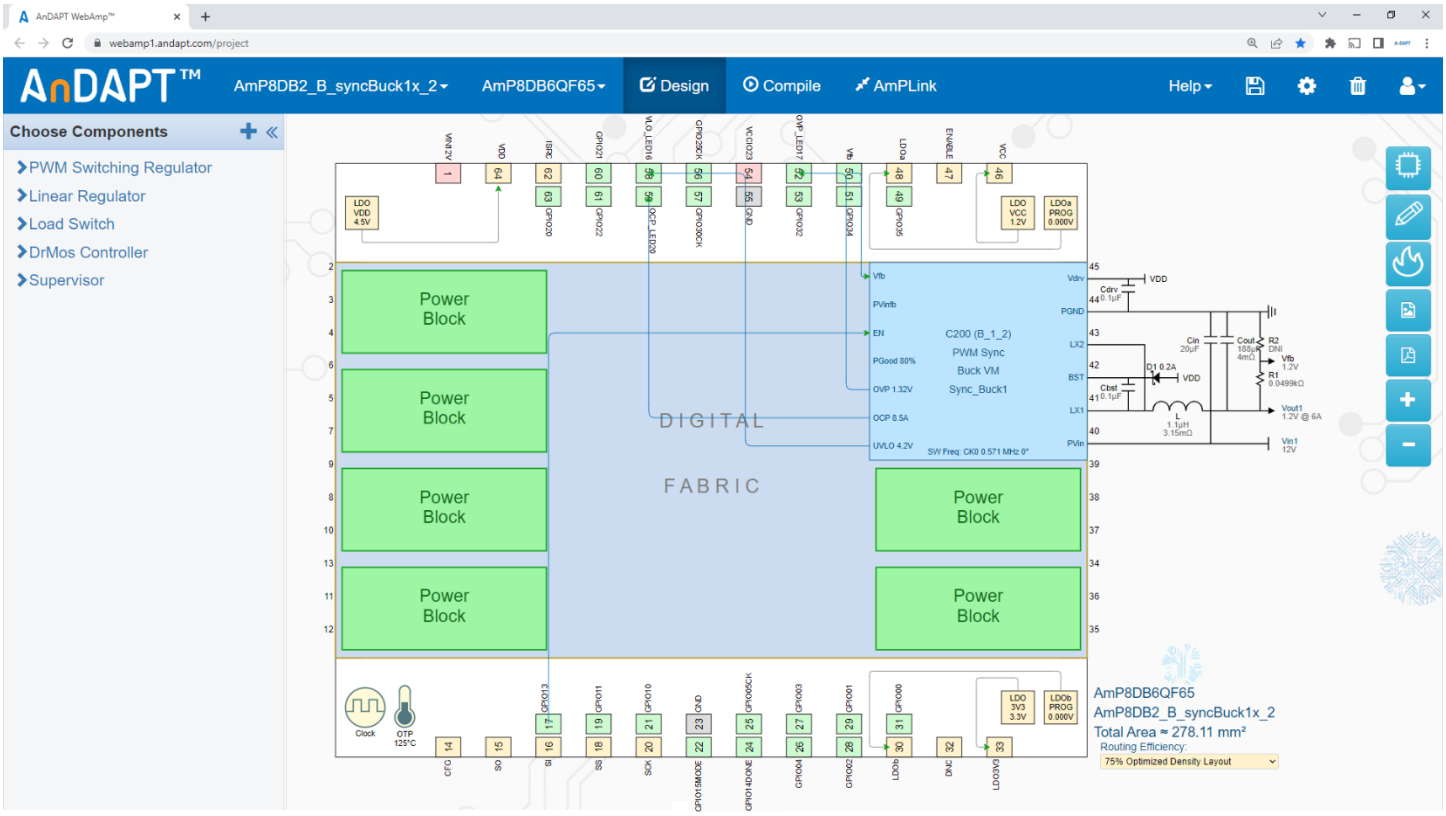
- LC Calculator
- Stability analyzer
- PID tuning
- Thermal Analyzer
- Efficiency calculator
- AmPScope™ to monitor and debug rails in circuit, in real time

On-demand WebAmp design tools enable design teams to deliver a complete integrated, single-chip solution quickly to their design specifications within days.

Application of Demonstration Board



WebAmP Example Project: AmP Example Buck x1



ESD CONSIDERATIONS

Establish and use (Electrostatic Damage) ESD-safe handling precautions when unpacking and handling ESD-sensitive devices. Store ESD sensitive devices in ESD safe containers until ready for use. The Tape-and-Reel moisture-sealed bag is an ESD approved barrier. The best practice is to keep the units in the original moisture sealed bags until ready for assembly. AnDAPT products are qualified to meet at least 500V ESD-MM (Machine Model) 2000V ESD-HM (Human Body Model). Restrict all device handling to ESD protected work areas that measure less than 400V static charge. Ensure that all workstations and personnel are properly grounded to prevent ESD.

Assembly Recommendation

For part placement, please use standard pick and place machine with ± 0.05 mm accuracy. Mount the device with slower speed and higher force. Place the package 1 ~ 2 mils into the paste. The device package has excellent self-alignment during solder reflow if a minimum of 75% of the lead diameter intersect with the pad.

Solder Paste

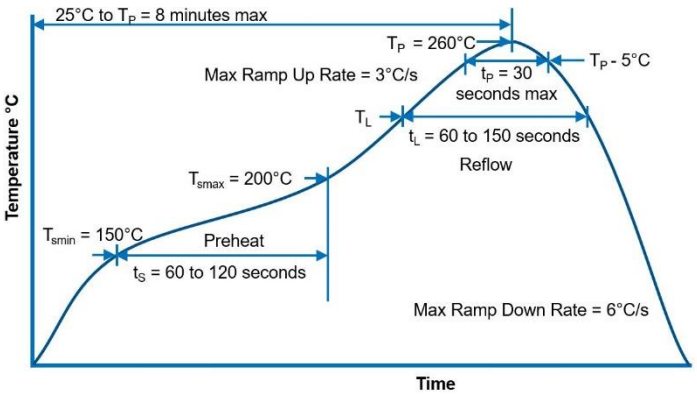
The screen printing quantity of solder paste is a key factor in producing high yield assemblies. Recommended solder paste alloy is Sn/Ag/Cu family for lead-free application. Low residue and no clean flux is recommended. Particle size type IV (25 ~ 38 μm) is preferred to improve printing performance. Particle size type III (25 ~ 45 μm) also is acceptable.

Solder Stencils

The contrast between large thermal pad and small terminal pads of the QFN package can present a challenge in production an even solder line thickness. The precise volume of solder paste deposited onto the device land pattern is controlled by the stencil thickness and the opening geometry. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow- solder processing. The solder joint thickness for QFN package terminal pads should be 50 – 75 μm. Stencil recommended type is laser cutting stainless steel with thickness of 100 ~ 150 μm (125 μm as a guide). The actual thickness of a stencil is depending on other SMD components on the PCB. Metal blade or polymer with 90-degree hardness squeegee is recommended. Aperture size for terminal pad should have aspect ratio (width / thickness) of greater than 1.5 and area ratio (Area of aperture opening / aperture wall area) of greater than 0.66. The stencil aperture is typically designed to match the pad size on the PCB 1 to 1. For fine pitch components of 0.5mm and below it may be necessary to reduce the stencil aperture length by 20%. Oval-shaped opening should be used to get the optimum paste release and rounded corners to minimize clogging. Positive taper walls (5-degree tapering) with bottom opening larger than the top is recommended. The small multiple openings should be used instead of one big opening. 60% ~ 85% solder paste coverage is recommended to reduce the chance of having short connection.

REFLOW SPECIFICATION

AnDAPT products are qualified in accordance with IPC/JEDEC J-STD-020D.1. This standard classifies proper packaging, storage and handling in order to avoid subsequent thermal and mechanical damage during the solder-reflow attachment phase of PCB assembly. Check solder paste data sheet for any additional or different instruction. Using forced convection reflow oven with nitrogen is recommended. Also, the reflow oven should have equal or less than ± 5°C temperature uniformity. The reflow profile for lead-free solder paste is shown below for reference only. Solder paste datasheet should be used accordingly.



Pb Free Classification Process Reflow Profile
JEDEC-J-STD-020D.1

COMPLIANCE

ENVIRONMENTAL COMPLIANCE

AnDAPT products are RoHS and Green compliant.

AnDAPT products are in full environmental compliance as evidenced by our Materials Declaration Data Sheets (MDS). The MDS report, along with support documentation consisting of Material Safety Data Sheets (MSDS) and analytical reports for each homogeneous element of the product are available upon request.

DRC COMPLIANCE

AnDAPT products use materials that comply with DRC (Democratic Republic of the Congo) Conflict-Free Smelter and Mines requirements to meet the SEC implementation of Dodd–Frank Section 1502.

COMPLIANCE DECLARATION DISCLAIMER

AnDAPT believes this compliance information to be correct but cannot guarantee accuracy or completeness. Conformity documents for the above component constitutes are on file. AnDAPT subcontracts manufacturing and the information contained herein is based on data received from vendors and suppliers, which has not been validated by AnDAPT.

GENERAL

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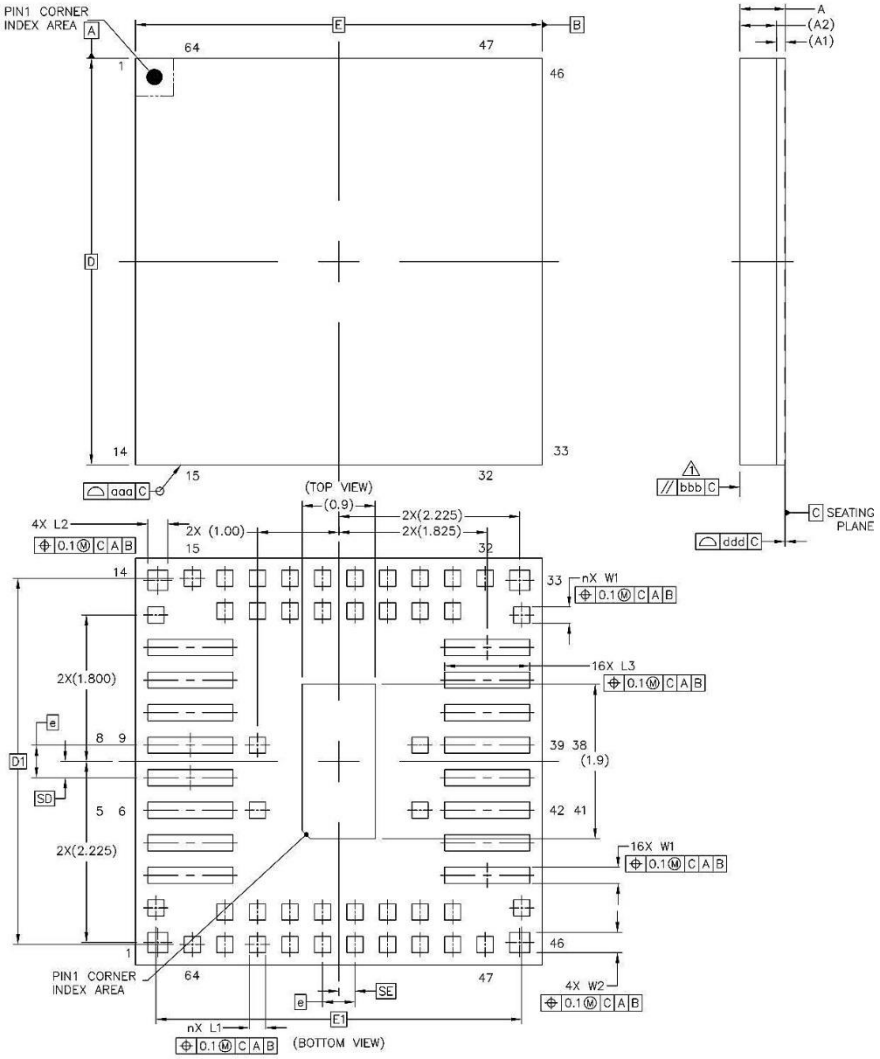
Package Description – QF65 5x5 mm

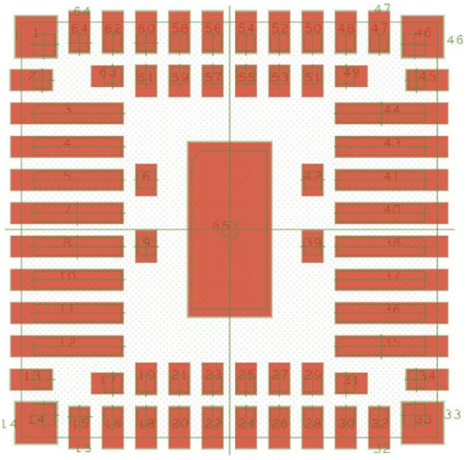


	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	0.65
SUBSTRATE THICKNESS	A1		0.11	REF
MOLD THICKNESS	A2		0.45	
BODY SIZE	D		5	BSC
	E		5	BSC
LEAD WIDTH	W1	0.15	0.2	0.25
LEAD WIDTH	W2	0.2	0.25	0.3
LEAD LENGTH	L1	0.15	0.2	0.25
LEAD LENGTH	L2	0.2	0.25	0.3
LEAD LENGTH	L3	1	1.05	1.1
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		65	
EDGE BALL CENTER TO CENTER	D1		4.5	BSC
	E1		4.5	BSC
BODY CENTER TO CONTACT BALL	SD		0.2	BSC
	SE		0.2	BSC
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		0.1	
COPLANARITY	ddd		0.08	
BALL OFFSET (PACKAGE)	eee		---	
BALL OFFSET (BALL)	fff		---	

QF65 with small Exposed Pad (EP)

The platform B QF65 package has a smaller EP (0.9mm x 1.9mm) compared to Platform A. With the same thermal performance, this new design improves reliability, routability and solderability. The Platform B QF65 is footprint compatible with the Platform A QF65.

Solder Stencil



Download files: AmP8DB6QF65footprint.zip

Additional Resources

- AmPDB2 Demoboard Datasheet
- AmPLink USB Adapter Datasheet
- AmPLink Configuration and Control
- Video - WebAmP Development Software
- Video - Using AmPLink
- Power Components Datasheets

Revision History

Date	Revision
04/19/2023	Added Vin ramp rate limit to EC table
09/01/2022	Updated Absolute Maximum Ratings Operating junction temperature Removed AmP4DB and AmP12DB MOSFET device options Removed AmP8DB1 and AmP8DB3 output current options Added clarification to Global Input Under Voltage (ViUVLO)
08/18/2022	Replaced Electrical Characteristics *QF65 5mm x 5mm Package with *For Vin>14V an external . . . Moved Electrical Characteristics **Total LDO power dissipation . . . to Integrated LDO Changed Order Information from “Part Number” to “Ordering Part Number”
07/21/2022	Changed package QF74 to QF65 in SPI Host, SPI Client, Programing FLASH, AmpLink Communication, WebAmP Tools, and WebAmP Example Project
06/09/2022	Updated Input Shutdown Current (Vin) to 1.1 mA
02/04/2022	Changed Single Supply Example and Separate Supply Example package to QF65 5x5 mm2 with Vin on pin 1
01/20/2022	Removed unused signal names from Pin Configurations table
08/03/2021	Updated Pb Free Classification Process Reflow Profile JEDEC-J-STD-020D.1, T_P = 260 °C
06/08/2021	Removed QF74 8x8 package
03/17/2021	Updated Pb Free Classification Process Reflow Profile JEDEC-J-STD-020D.1
02/09/2021	Update Package Marking Examples
08/10/2020	Added QF65 with small Exposed Pad (EP) Package Description
02/20/2020	Initial release

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