



ALPHA & OMEGA
SEMICONDUCTOR

AOCA33104E
12V Common-Drain Dual N-Channel MOSFET

General Description

- Trench Power MOSFET technology
- Ultra low $R_{SS(ON)}$
- Common drain configuration for design simplicity
- RoHS and Halogen-Free Compliant

Applications

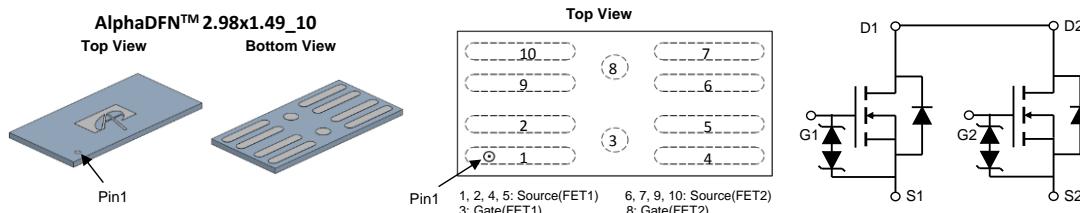
- Battery protection switch
- Mobile device battery charging and discharging

Product Summary

V_{SS}	12V
$R_{SS(ON)}$ (at $V_{GS}=4.5V$)	< 2.8mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.8V$)	< 3mΩ
$R_{SS(ON)}$ (at $V_{GS}=3.1V$)	< 3.5mΩ
$R_{SS(ON)}$ (at $V_{GS}=2.5V$)	< 4.2mΩ

Typical ESD protection

HBM Class 2



Orderable Part Number	Package Type	Form	Minimum Order Quantity
AOCA33104E	AlphaDFN™ 2.98x1.49_10	Tape & Reel	8000

Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Rating	Units
Source-Source Voltage	V_{SS}	12	V
Gate-Source Voltage	V_{GS}	± 8	V
Source Current(DC) ^{Note1}	I_S	30	A
Source Current(Pulse) ^{Note2}	I_{SM}	130	
Power Dissipation ^{Note1}	P_D	3.1	W
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typical	Units
Maximum Junction-to-Ambient $t \leq 10s$	R_{JJA}	30	°C/W
Maximum Junction-to-Ambient Steady-State		40	°C/W

Note 1. I_S rated value is based on bare silicon. Mounted on 70mmx70mm FR-4 board.

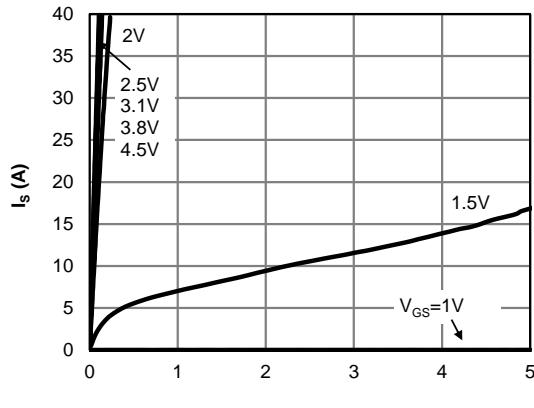
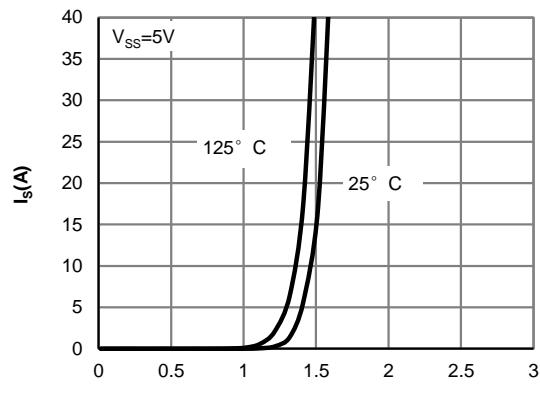
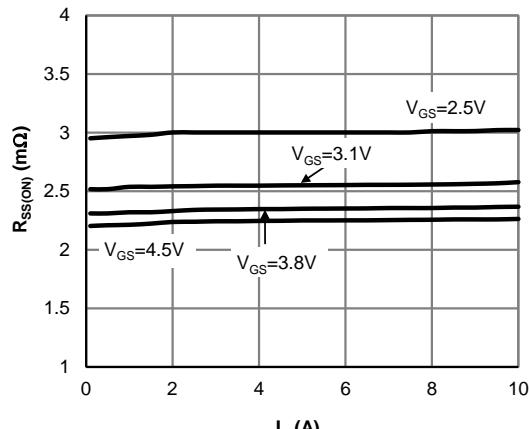
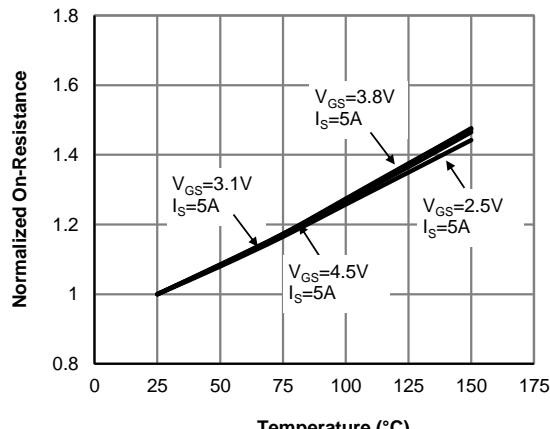
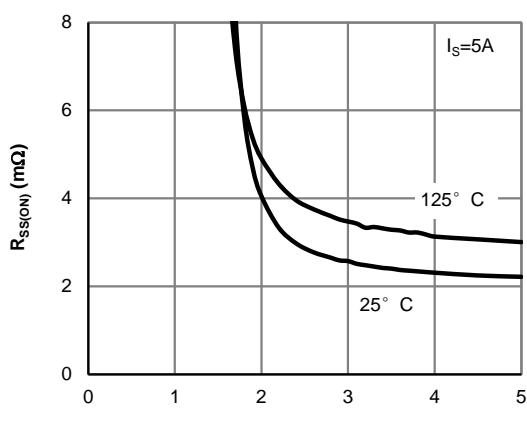
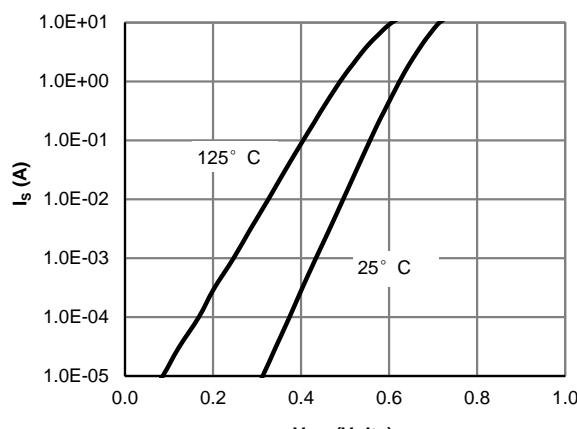
Note 2. PW <10 μs pulses, duty cycle 1% max.

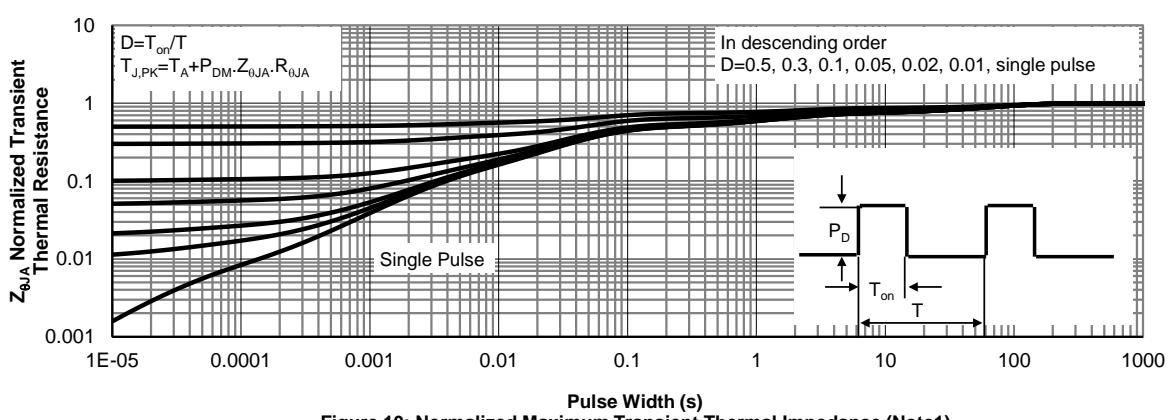
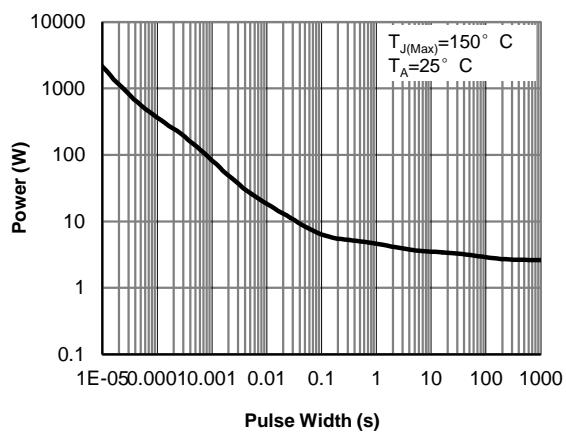
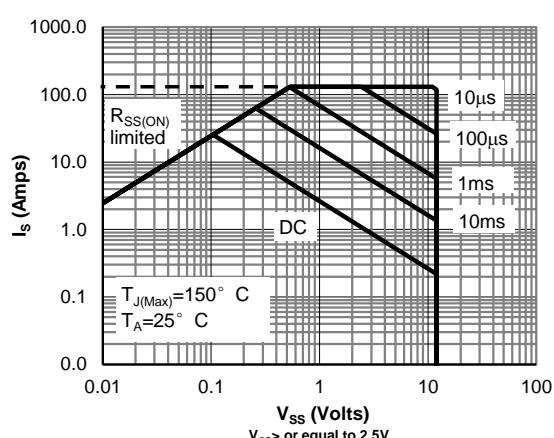
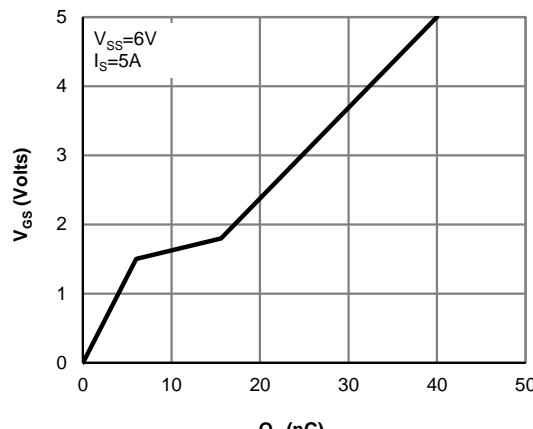
Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

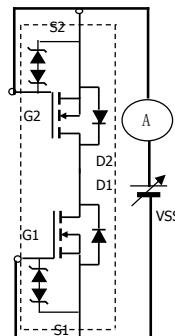
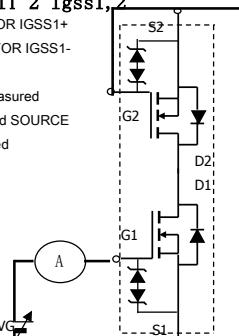
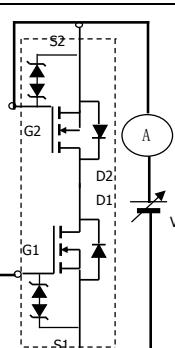
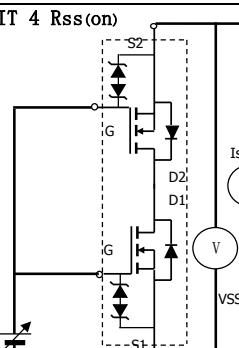
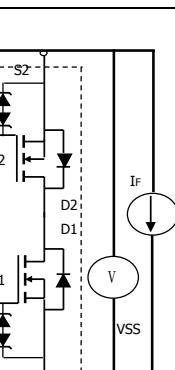
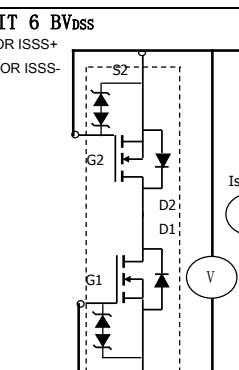
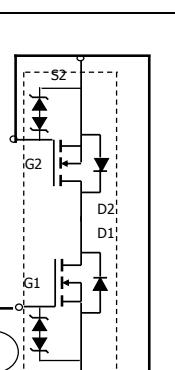
Symbol	Parameter	Conditions	Min	Typ	Max	Units	
STATIC PARAMETERS							
BV_{SSS}	Source-Source Breakdown Voltage	$I_S=250\mu\text{A}, V_{GS}=0\text{V}$	Test Circuit 6	12		V	
I_{SSS}	Zero Gate Voltage Source Current	$V_{SS}=12\text{V}, V_{GS}=0\text{V}$	Test Circuit 1 $T_J=55^\circ\text{C}$		1 5	μA	
I_{GSS}	Gate leakage current	$V_{SS}=0\text{V}, V_{GS}=\pm 8\text{V}$	Test Circuit 2		± 10	μA	
$V_{GS(\text{th})}$	Gate Threshold Voltage	$V_{SS}=V_{GS}, I_S=250\mu\text{A}$	Test Circuit 3	0.4	0.75	1.2	V
$R_{\text{SS(ON)}}$	Static Source to Source On-Resistance	$V_{GS}=4.5\text{V}, I_S=5\text{A}$	Test Circuit 4	1.6	2.25	2.8	$\text{m}\Omega$
		$T_J=125^\circ\text{C}$		2.1	3.1	3.9	
		$V_{GS}=3.8\text{V}, I_S=5\text{A}$	Test Circuit 4	1.7	2.35	3	$\text{m}\Omega$
		$V_{GS}=3.1\text{V}, I_S=5\text{A}$	Test Circuit 4	1.8	2.55	3.5	$\text{m}\Omega$
g_{FS}	Forward Transconductance	$V_{SS}=2.5\text{V}, I_S=5\text{A}$	Test Circuit 4	2	3	4.2	$\text{m}\Omega$
		$V_{SS}=5\text{V}, I_S=5\text{A}$	Test Circuit 3		40		S
V_{FSS}	Forward Source to Source Voltage	$I_S=1\text{A}, V_{GS}=0\text{V}$	Test Circuit 5		0.6	1	V
DYNAMIC PARAMETERS							
R_g	Gate resistance	$f=1\text{MHz}$			1.5	$\text{k}\Omega$	
SWITCHING PARAMETERS							
Q_g	Total Gate Charge	$V_{G1S1}=4.5\text{V}, V_{SS}=6\text{V}, I_S=5\text{A}$			36	nC	
$t_{D(on)}$	Turn-On DelayTime				2.2	μs	
t_r	Turn-On Rise Time	$V_{G1S1}=4.5\text{V}, V_{SS}=6\text{V}, R_L=1.2\Omega,$ $R_{\text{GEN}}=3\Omega$	Test Circuit 8		5	μs	
$t_{D(off)}$	Turn-Off DelayTime				2.6	μs	
t_f	Turn-Off Fall Time				10.4	μs	

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Figure 1: On-Region Characteristics

Figure 2: Transfer Characteristics

Figure 3: On-Resistance vs. Source Current and Gate Voltage

Figure 4: On-Resistance vs. Junction Temperature

Figure 5: On-Resistance vs. Gate-Source Voltage

Figure 6: Forward Source to Source Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS


TEST CIRCUIT 1 Isss POSITIVE VSS FOR ISSS+ NEGATIVE VSS FOR ISSS- 	TEST CIRCUIT 2 Igss1,2 POSITIVE VGS FOR IGSS1+ NEGATIVE VGS FOR IGSS1- <p>When FET1 is measured between GATE and SOURCE of FET2 are shorted</p> 
TEST CIRCUIT 3 Vgs(off) <p>When FET1 is measured between GATE and SOURCE of FET2 are shorted</p> 	TEST CIRCUIT 4 Rss(on) 
TEST CIRCUIT 5 VF(ss)1,2 <p>When FET1 measured FET2 VGS=4.5V</p> 	TEST CIRCUIT 6 BVdss POSITIVE VSS FOR ISSS+ NEGATIVE VSS FOR ISSS- 
TEST CIRCUIT 7 BVgs01,2 POSITIVE VSS FOR ISSS+ NEGATIVE VSS FOR ISSS- <p>When FET1 is measured between GATE and SOURCE of FET2 are shorted</p> 	TEST CIRCUIT 8 Switching time 