AOZ8844

Ultra-Low Capacitance TVS Diode

General Description

The AOZ8844 is a transient voltage suppressor array designed to protect high speed data lines such as HDMI, USB 3.0, MDDI, SATA, and Gigabit Ethernet from damaging ESD events.

This device incorporates eight surge rated, low capacitance steering diodes and a TVS in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground.

The AOZ8844 provides a typical line-to-line capacitance of 0.26 pF and low insertion loss up to 6 GHz providing greater signal integrity making it ideally suited for HDMI 1.3 or USB 3.0 applications, such as Digital TVs, DVD players, computing, set-top boxes and MDDI applications in mobile computing devices.

The AOZ8844 comes in a RoHS compliant and Halogen Free 1.3 mm x 0.8 mm x 0.4 mm DFN-5 package and is rated for -40°C to +125°C junction temperature range.

Features

- ESD protection for high-speed data lines:
  - IEC 61000-4-2, level 4 (ESD) immunity test
  - Air discharge: ±20 kV; contact discharge: ±15 kV
  - IEC61000-4-4 (EFT) 40 A (5/50 ns)
  - IEC61000-4-5 (Lightning) +5 A (8/20 µs)
  - Human Body Model (HBM) ±24 kV
- Array of surge rated diodes with internal TVS diode
- Small package saves board space
- Protects four I/O lines
- Low capacitance between I/O lines: 0.26 pF
- Low clamping voltage

Applications

- HDMI, USB 3.0, MDDI, SATA ports
- Monitors and flat panel displays
- Set-top box
- Video graphics cards
- Digital Video Interface (DVI)
- Notebook computers

Green Product

Typical Applications

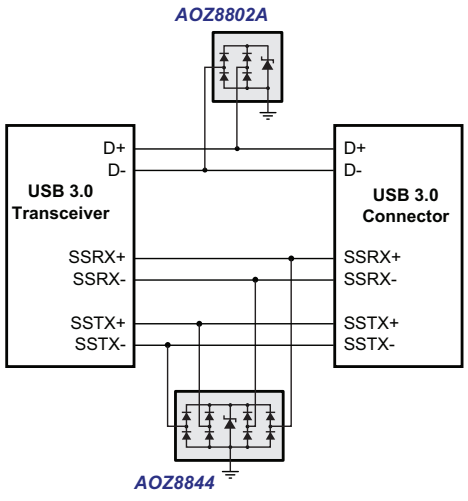


Figure 1. USB 3.0 Ports

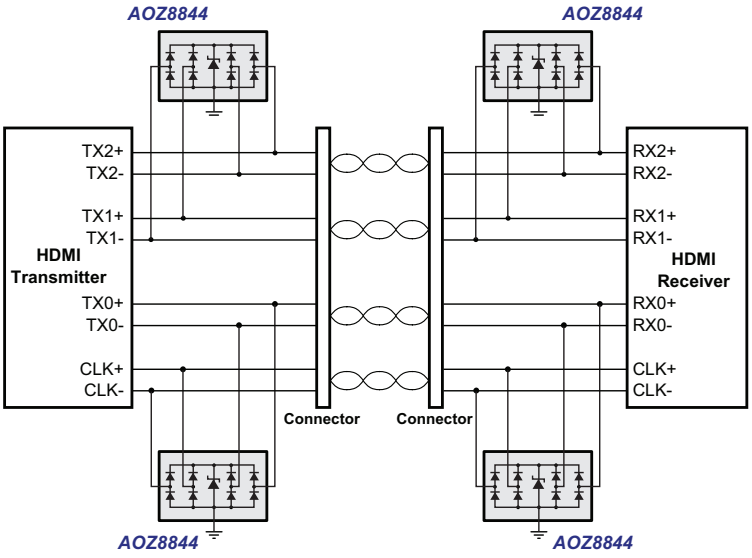


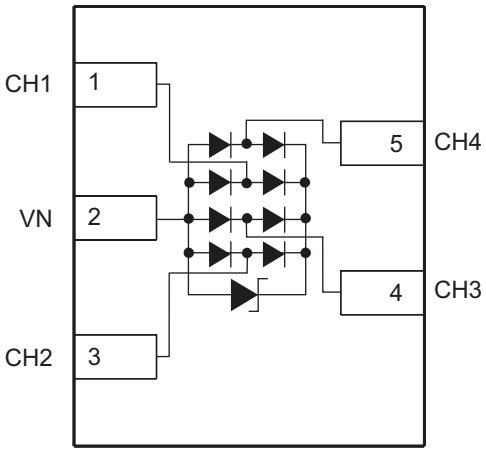
Figure 2. HDMI Ports

Ordering Information

Part Number	Ambient Temperature Range	Package	Environmental
AOZ8844DT	-40°C to +85°C	1.3 mm x 0.8 mm x 0.4 mm DFN-5	Green Product

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

Pin Configuration



DFN-5
(Top View)

Absolute Maximum Ratings

Exceeding the Absolute Maximum ratings may damage the device.

Parameter	Rating
Storage Temperature (T_S)	-65°C to +150°C
ESD Rating per IEC61000-4-2, contact[(1)(3)]	±15 kV
ESD Rating per IEC61000-4-2, air[(1)(3)]	±20 kV
ESD Rating per Human Body Model[(2)(3)]	±24 kV

Notes:

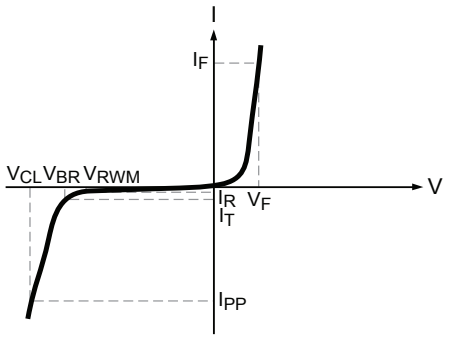
1. IEC 61000-4-2 discharge with $C_{Discharge}$ = 150pF, $R_{Discharge}$ = 330 Ω.
2. Human Body Discharge per MIL-STD-883, Method 3015 $C_{Discharge}$ = 100 pF, $R_{Discharge}$ = 1.5 kΩ.

Maximum Operating Ratings

Parameter	Rating
Junction Temperature (T_J)	-40°C to +125°C

Electrical Characteristics

T_A = 25°C unless otherwise specified.

Symbol	Parameter	Diagram
I_{PP}	Maximum Reverse Peak Pulse Current	
V_{CL}	Clamping Voltage @ I_{PP} (IEC61000-4-5 8/20 µs pulse)	
V_{RWM}	Working Peak Reverse Voltage	
I_R	Maximum Reverse Leakage Current	
V_{BR}	Breakdown Voltage	
I_T	Test Current	
V_F	Forward Voltage @ I_F (I_F = 15 mA)	
P_{pk}	Peak Power Dissipation (IEC61000-4-5 8/20 µs pulse)	
C_J	Capacitance @ V_R = 0 and f = 1 MHz	

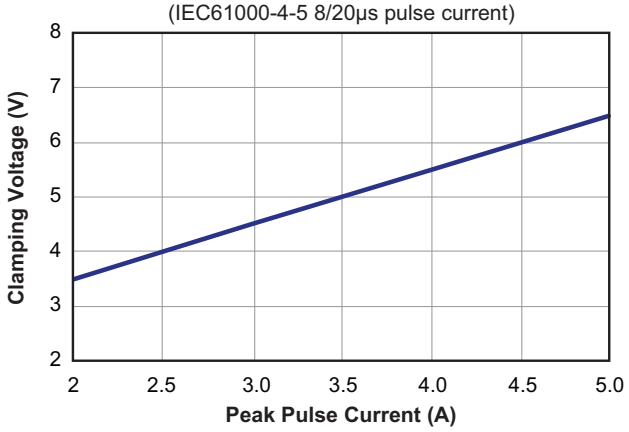
Device	Device Marking	V_{RWM} (V) Max.	V_{BR} (V) Min. I_T = 100 µA	I_R (µA) Max.	V_F (V) Typ.	V_{CL} Max.(3)		P_{PK} (W)	C_J (pF)	
						I_{PP} = 2 A	I_{PP} = 5 A		Typ.	Max.
AOZ8844DT	A	5.0	6.0	1.0	0.85	3.5	6.5	32	0.5	0.6

Notes:

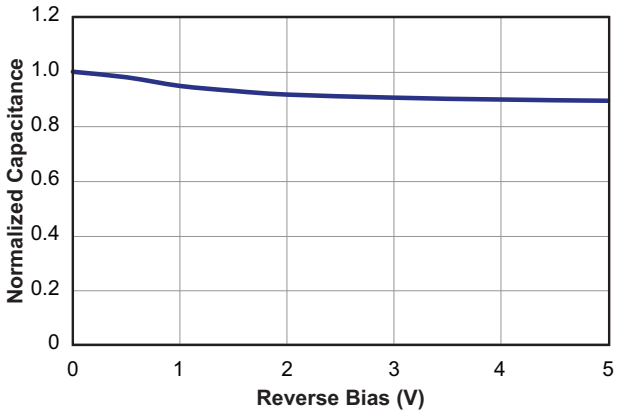
3. These specifications are guaranteed by design and characterization.

Typical Performance Characteristics

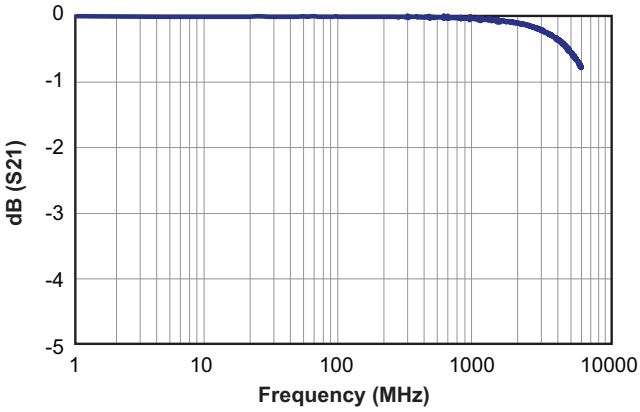
Clamping Voltage vs. Peak Pulse Current
(IEC61000-4-5 8/20µs pulse current)



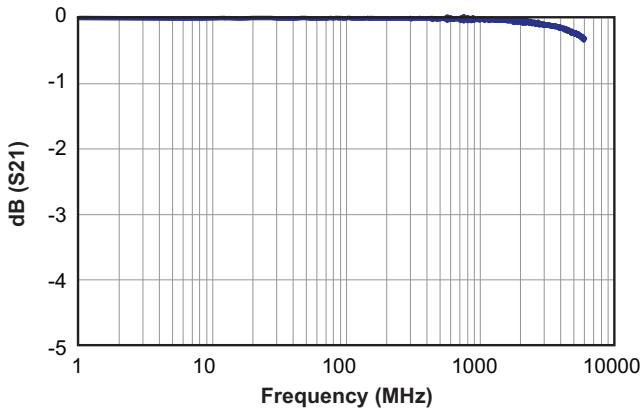
Capacitance vs. Reverse Bias



IO-GND Insertion Loss (S21) vs. Frequency



IO-IO Insertion Loss (S21) vs. Frequency



High Speed PCB Layout Guidelines

Printed circuit board layout is the key to achieving the highest level of surge immunity on power and data lines. The location of the protection devices on the PCB is the simplest and most important design rule to follow. The AOZ8844DT devices should be located as close as possible to the noise source. The AOZ8844DT device should be placed on all data and power lines that enter or exit the PCB at the I/O connector. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Placing the AOZ8844DT devices as close as possible to the noise source ensures that a surge voltage will be clamped before the pulse can be coupled into adjacent PCB traces. In addition, the PCB should use the shortest possible traces. A short trace length equates to low impedance, which ensures that the surge energy will be dissipated by the AOZ8844DT device. Long signal traces will act as antennas to receive energy from fields that are produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD related fields is reduced. Minimize interconnecting line lengths by placing devices with the most interconnect as close together as possible. The protection circuits should shunt the surge voltage to either the reference or chassis ground. Shunting the surge voltage directly to the IC's signal ground can cause ground bounce. The clamping performance of TVS diodes on a single ground PCB can be improved by minimizing the impedance with relatively short and wide ground traces. The PCB layout and IC package parasitic inductances can cause significant overshoot to the TVS's clamping voltage. The inductance of the PCB can be reduced by using short trace lengths and multiple layers with separate ground and power planes. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design.

The AOZ8844DT ultra-low capacitance TVS is designed to protect four high speed data transmission lines from transient over-voltages by clamping them to a fixed reference. The low inductance and construction minimizes voltage overshoot during high current surges. When the voltage on the protected line exceeds the reference voltage the internal steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. The AOZ8844DT is designed for ease of PCB layout by allowing the traces to run underneath the device. The pinout of the AOZ8844DT is designed to simply drop onto the IO lines of a High Definition Multimedia Interface (HDMI) or USB 3.0 design without having to divert the signal lines that may add more parasitic inductance. Pins 1, 2, 4 and 5 are connected to the internal TVS devices and pins 6, 7, 9 and 10 are no connects. The no connects was done so the package can be securely soldered onto the PCB surface.

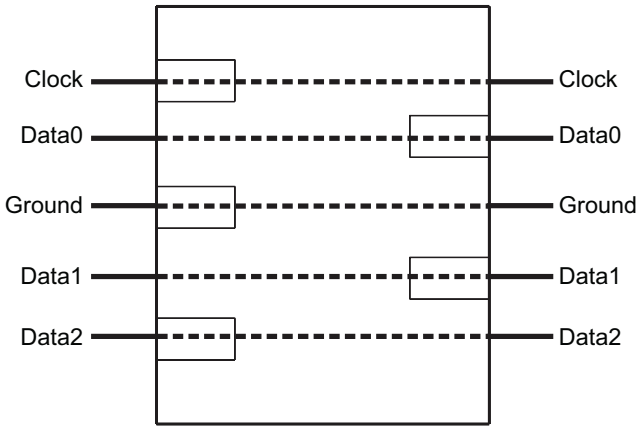


Figure 3. Flow Through Layout for HDMI

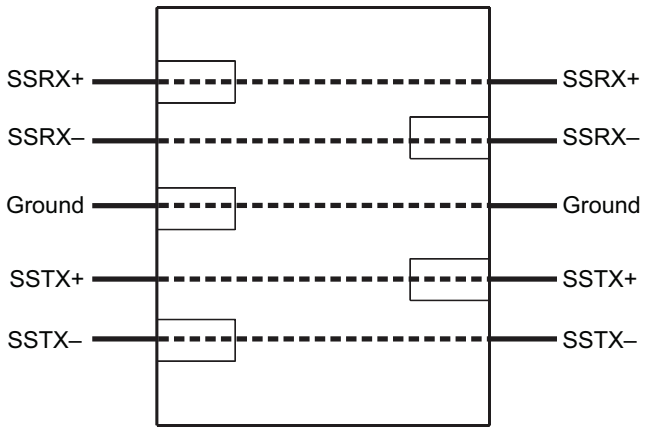


Figure 4. Flow Through Layout for USB 3.0

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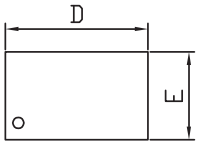
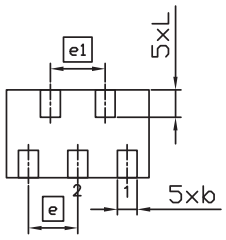
Package Dimensions, DFN1.3x0.8-5L, NEP_S

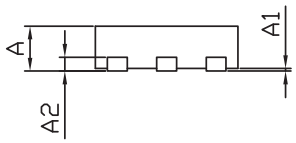
DFN1.3x0.8_5L_NEP_S PACKAGE OUTLINE



TOP VIEW

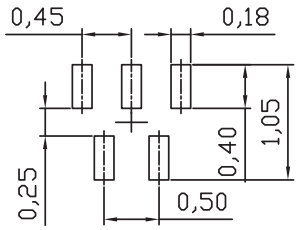


BOTTOM VIEW



SIDE VIEW

RECOMMENDED LAND PATTERN



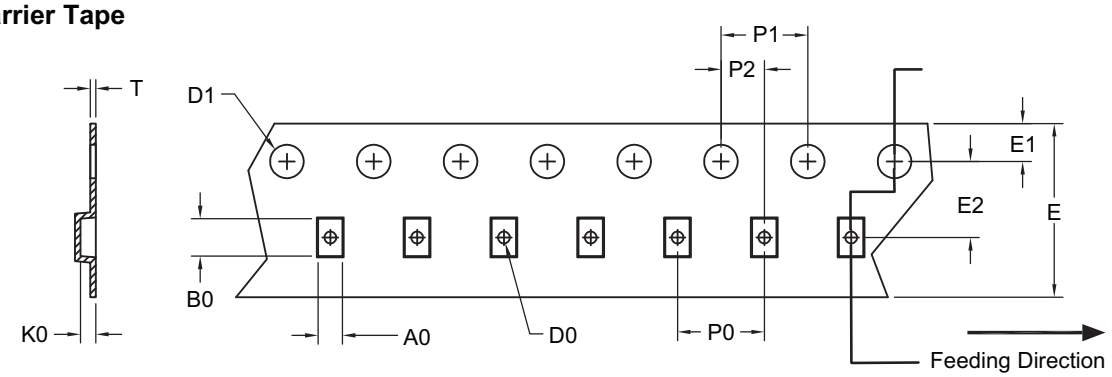
UNIT: mm

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.37	0.40	0.43	0.015	0.016	0.017
A1	0.00	0.01	0.05	0.000	0.000	0.002
A2	0.08	0.13	0.18	0.003	0.005	0.007
b	0.13	0.18	0.23	0.005	0.007	0.009
D	1.20	1.30	1.40	0.047	0.051	0.055
E	0.70	0.80	0.90	0.028	0.031	0.035
e	0.45 BSC			0.018 BSC		
e1	0.50 BSC			0.020 BSC		
L	0.20	0.25	0.30	0.008	0.010	0.012

NOTE
1. CONTROLLING DIMENSION IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
2. LAND PATTERN DIMENSIONS ARE ONLY FOR REFERENCE.

Tape and Reel Dimensions, DFN1.3x0.8-5L, NEP_S

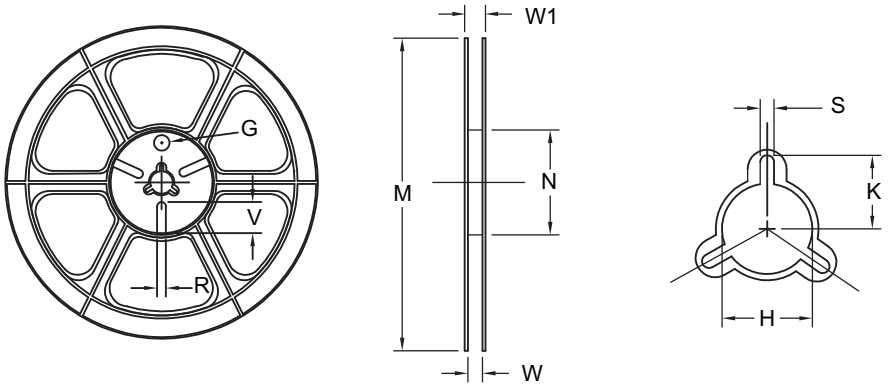
Carrier Tape



UNIT: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
DFN 1.3x0.8 (8mm)	1.02 ±0.05	1.52 ±0.05	0.50 ±0.05	0.50 ±0.05	1.50 ±0.10	8.00 +0.3/-0.10	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.20 ±0.02

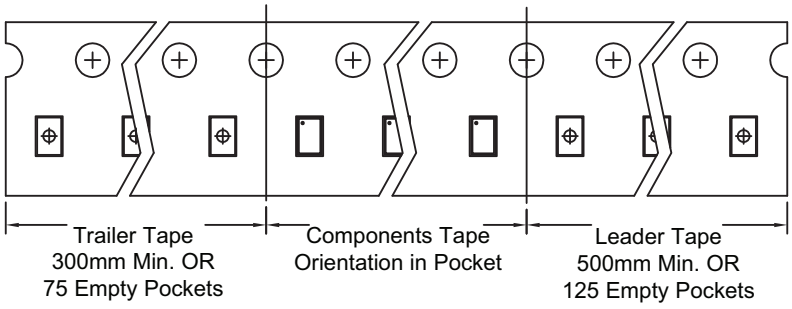
Reel



UNIT: mm

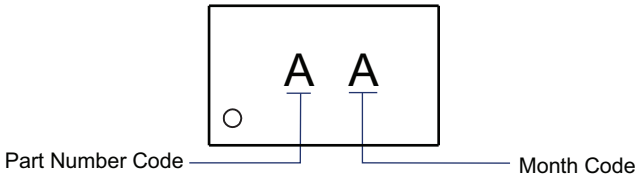
Tape Size	Reel Size	M	N	W	W1	H	K	S	E	R	R
8mm	ø178	ø178.0 ±1.0	ø60.0 ±1.0	9.0 ±0.5	—	ø13.0 +0.5 / –0.2	10.25 ±0.2	2.4 ±0.1	ø9.8	—	—

Leader / Trailer & Orientation



Part Marking

AOZ8844DT
(1.3 x 0.8 DFN)



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