

# BLA9G1011L(S)-300; BLA9G1011L(S)-300G

Power LDMOS transistor

Rev. 1 — 25 July 2017

AMMPLION

Product data sheet

## 1. Product profile

### 1.1 General description

300 W LDMOS power transistor for avionics applications at frequencies from 1030 MHz to 1090 MHz.

**Table 1. Typical information**

Typical RF performance at  $T_{case} = 25\text{ °C}$ ;  $t_p = 50\text{ }\mu\text{s}$ ;  $\delta = 2\%$ ;  $I_{Dq} = 100\text{ mA}$ ; in a class-AB demo test circuit.

Test signal	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	$\eta_D$ (%)	t <sub>r</sub> (ns)	t <sub>f</sub> (ns)
pulsed RF	1030	32	317	20.6	63.5	14	5
	1060	32	317	21.5	64.8	14	5
	1090	32	317	21.8	64.8	14	5

### 1.2 Features and benefits

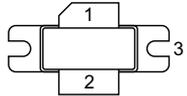
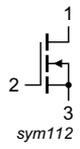
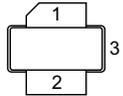
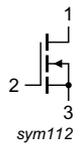
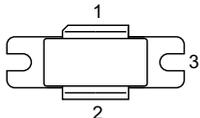
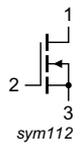
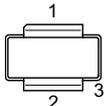
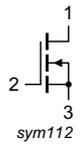
- Easy power control
- Integrated dual sided ESD protection enables excellent off-state isolation
- Enhanced ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (1030 MHz to 1090 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- Avionics transmitter applications in the 1030 MHz to 1090 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLA9G1011L-300 (SOT502A)</b>			
1	drain		
2	gate		
3	source <a href="#">[1]</a>		
<b>BLA9G1011LS-300 (SOT502B)</b>			
1	drain		
2	gate		
3	source <a href="#">[1]</a>		
<b>BLA9G1011L-300G (SOT502F)</b>			
1	drain		
2	gate		
3	source <a href="#">[1]</a>		
<b>BLA9G1011LS-300G (SOT502E)</b>			
1	drain		
2	gate		
3	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BLA9G1011L-300	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT502A
BLA9G1011LS-300	-	earless flanged ceramic package; 2 leads	SOT502B
BLA9G1011L-300G	-	eared flanged ceramic package; 2 leads; 2 mounting holes	SOT502F
BLA9G1011LS-300G	-	earless flanged ceramic package; 2 leads	SOT502E

## 4. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-6	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 25\text{ °C}$ ; $t_p = 100\ \mu\text{s}$ ; $\delta = 10\%$	0.140	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 3.3\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$ ; $I_D = 330\text{ mA}$	1.5	2.0	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 32\text{ V}$	-	-	4.2	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $V_{DS} = 10\text{ V}$	-	60	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	420	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 330\text{ mA}$	-	3	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $I_D = 11.55\text{ A}$	-	0.043	-	$\Omega$

**Table 7. RF characteristics**

Test signal: pulsed RF;  $t_p = 50\ \mu\text{s}$ ;  $\delta = 2\%$ ;  $V_{DS} = 32\text{ V}$ ;  $f = 1060\text{ MHz}$ ;  $I_{Dq} = 100\text{ mA}$ ;  $T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production test circuit for straight leads.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 300\text{ W}$	18	19.5	-	dB
$RL_{in}$	input return loss	$P_L = 300\text{ W}$	-	-10	-	dB
$\eta_D$	drain efficiency	$P_L = 300\text{ W}$	56	60.5	-	%
$t_r$	rise time	$P_L = 300\text{ W}$	-	14	-	ns
$t_f$	fall time	$P_L = 300\text{ W}$	-	5	-	ns

## 7. Test information

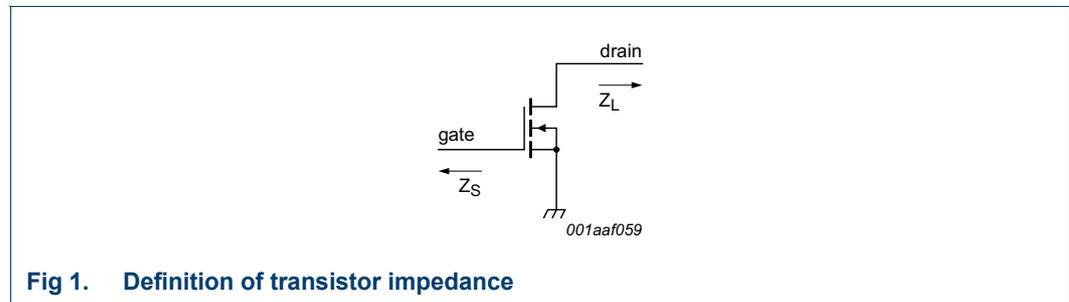
### 7.1 Ruggedness in class-AB operation

The BLA9G1011L-300, BLA9G1011LS-300, BLA9G1011L-300G and BLA9G1011LS-300G are enhanced rugged devices and are capable of withstanding a load mismatch corresponding to  $V_{SWR} = 10 : 1$  through all phases under the following conditions:  $t_p = 50 \mu s$ ;  $\delta = 2 \%$ ;  $V_{DS} = 32 V$ ;  $I_{Dq} = 100 mA$ ;  $P_L = 300 W$ ;  $f = 1030 MHz$  to  $1090 MHz$ .

### 7.2 Impedance information

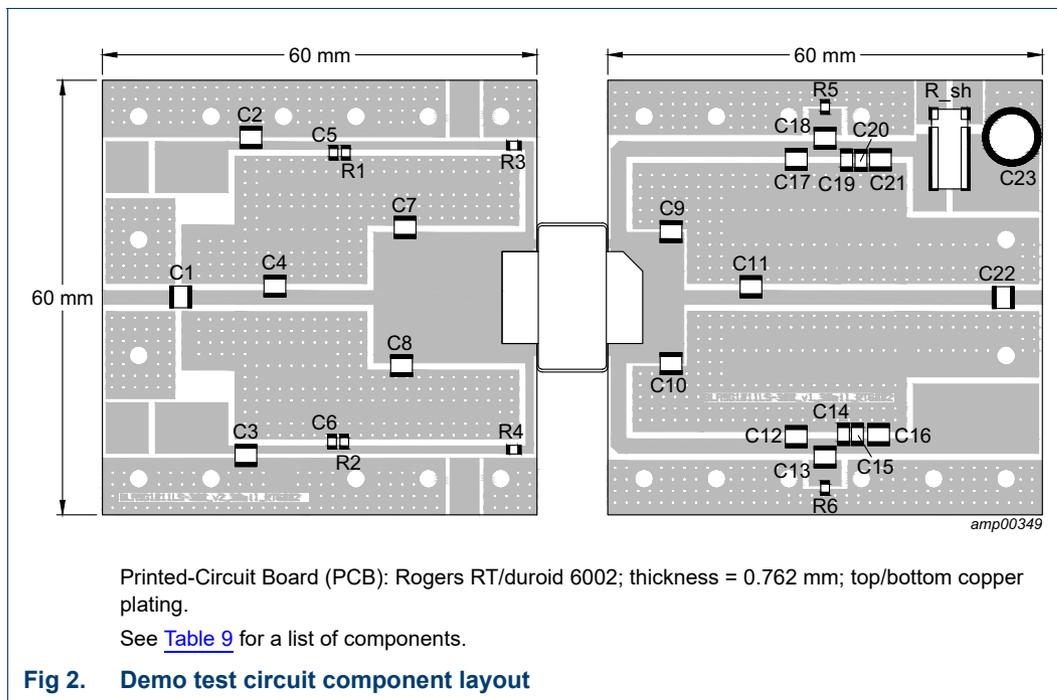
**Table 8. Typical impedance**  
*Typical values unless otherwise specified.*

f (MHz)	Z <sub>S</sub> (Ω)	Z <sub>L</sub> (Ω)
1000	0.87 – j2.02	1.38 – j1.78
1050	1.34 – j2.26	1.4 – j1.54
1100	1.82 – j2.77	1.4 – j1.54



**Fig 1. Definition of transistor impedance**

7.3 Test circuit

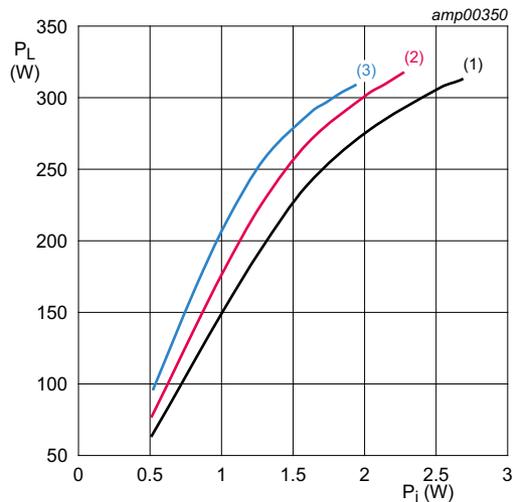


**Table 9. Demo test circuit list of components**

See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	56 pF	ATC: ATC100A560FT150XTV
C2, C3	multilayer ceramic chip capacitor	750 pF	ATC: ATC100B750FT500XTV
C4	multilayer ceramic chip capacitor	2.4 pF	ATC: ATC100B2R4BT500XTV
C5, C6	multilayer ceramic chip capacitor	62 pF	ATC: ATC100A620FT150XTV
C7, C8	multilayer ceramic chip capacitor	3.3 pF	ATC: ATC100B3R3BT500XTV
C9, C10	multilayer ceramic chip capacitor	7.5 pF	ATC: ATC100B7R5BT500XTV
C11	multilayer ceramic chip capacitor	4.7 pF	ATC: ATC100B4R7BT500XTV
C12, C17	multilayer ceramic chip capacitor	62 pF	ATC: ATC100B620FT500XTV
C13, C18	multilayer ceramic chip capacitor	750 pF	ATC: ATC100B751FT500XTV
C14, C19	multilayer ceramic chip capacitor	10 nF	Murata: GRM188R71H103KA01D
C15, C20	multilayer ceramic chip capacitor	100 nF	Murata: GRM31C5C1E104JA01L
C16, C21	multilayer ceramic chip capacitor	10 μF	Murata: GRM319R71H104KA01D
C22	multilayer ceramic chip capacitor	56 pF	ATC: ATC100B560FT500XTV
C23	electrolytic capacitor	470 μF, 63 V	Nichicon: UVZ1J471MHD1TO
R1, R2	SMD resistor	1 kΩ	0603
R3, R4	SMD resistor	5.1 Ω	0603
R5, R6	SMD resistor	3.9 Ω	0603
R_sh	SMD resistor	10 mΩ	Ohmite: FC4L110R010FER

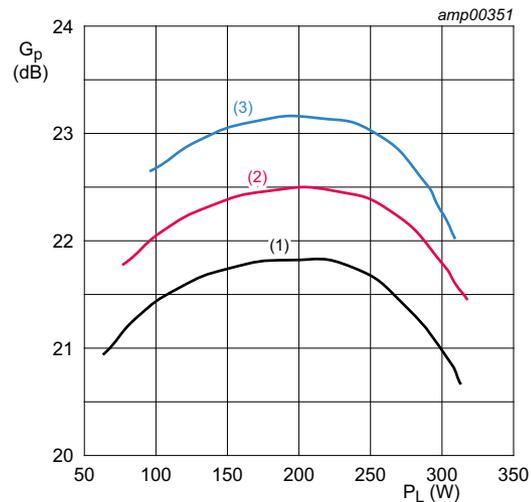
7.4 Graphical data



$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 50\text{ }\mu\text{s}; \delta = 2\text{ }\%$ .

- (1)  $f = 1030\text{ MHz}$
- (2)  $f = 1060\text{ MHz}$
- (3)  $f = 1090\text{ MHz}$

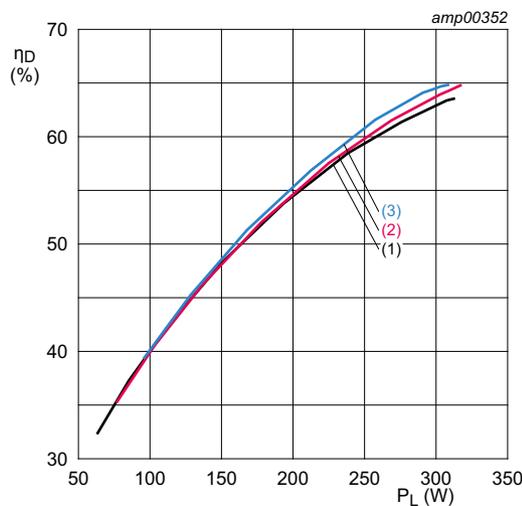
**Fig 3. Output power as a function of input power; typical values**



$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 50\text{ }\mu\text{s}; \delta = 2\text{ }\%$ .

- (1)  $f = 1030\text{ MHz}$
- (2)  $f = 1060\text{ MHz}$
- (3)  $f = 1090\text{ MHz}$

**Fig 4. Power gain as a function of output power; typical values**



$V_{DS} = 32\text{ V}; I_{Dq} = 100\text{ mA}; t_p = 50\text{ }\mu\text{s}; \delta = 2\text{ }\%$ .

- (1)  $f = 1030\text{ MHz}$
- (2)  $f = 1060\text{ MHz}$
- (3)  $f = 1090\text{ MHz}$

**Fig 5. Drain efficiency as a function of output power; typical values**

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads

SOT502A

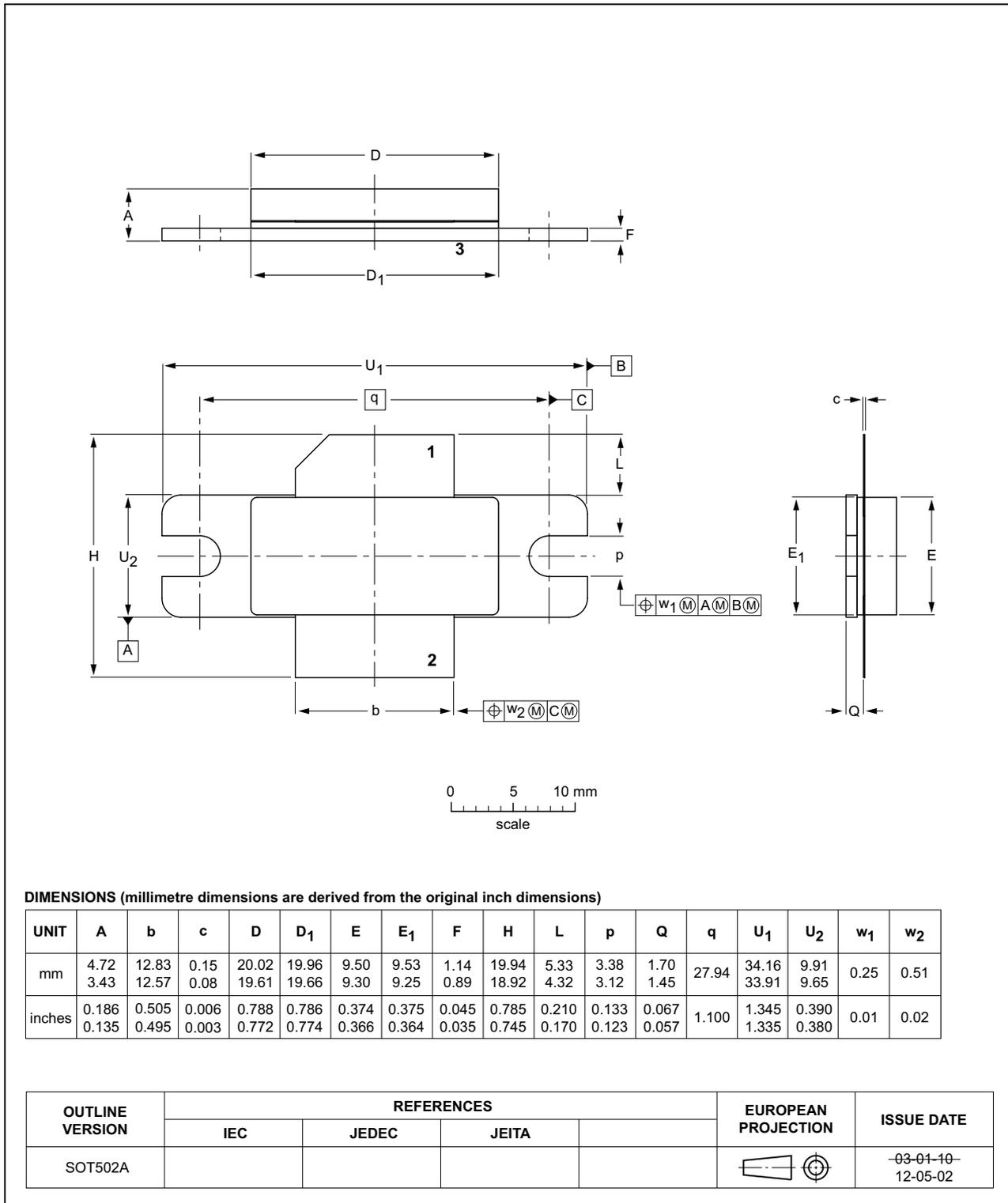


Fig 6. Package outline SOT502A

Earless flanged ceramic package; 2 leads

SOT502B

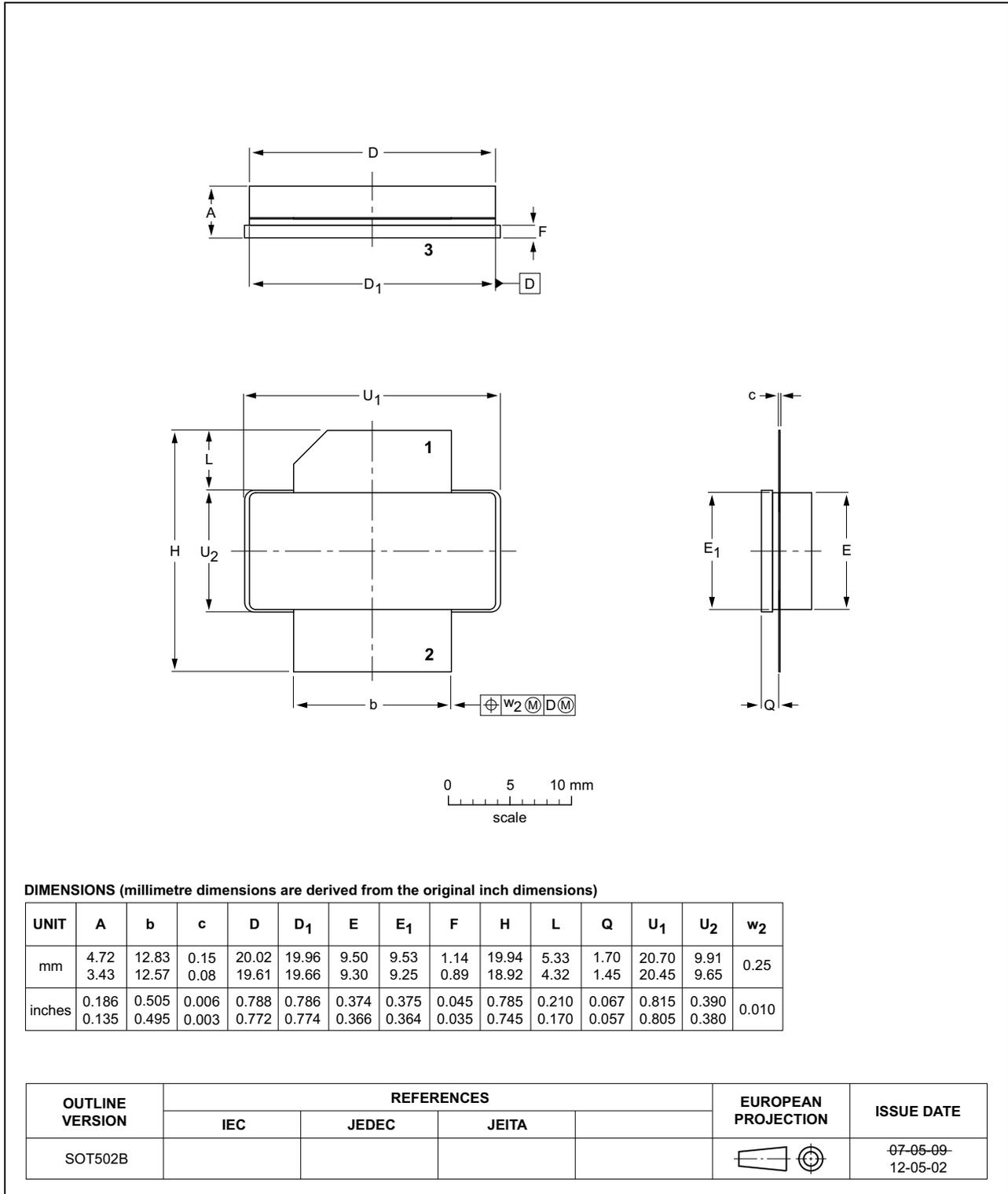


Fig 7. Package outline SOT502B

Earless flanged ceramic package; 2 leads

SOT502E

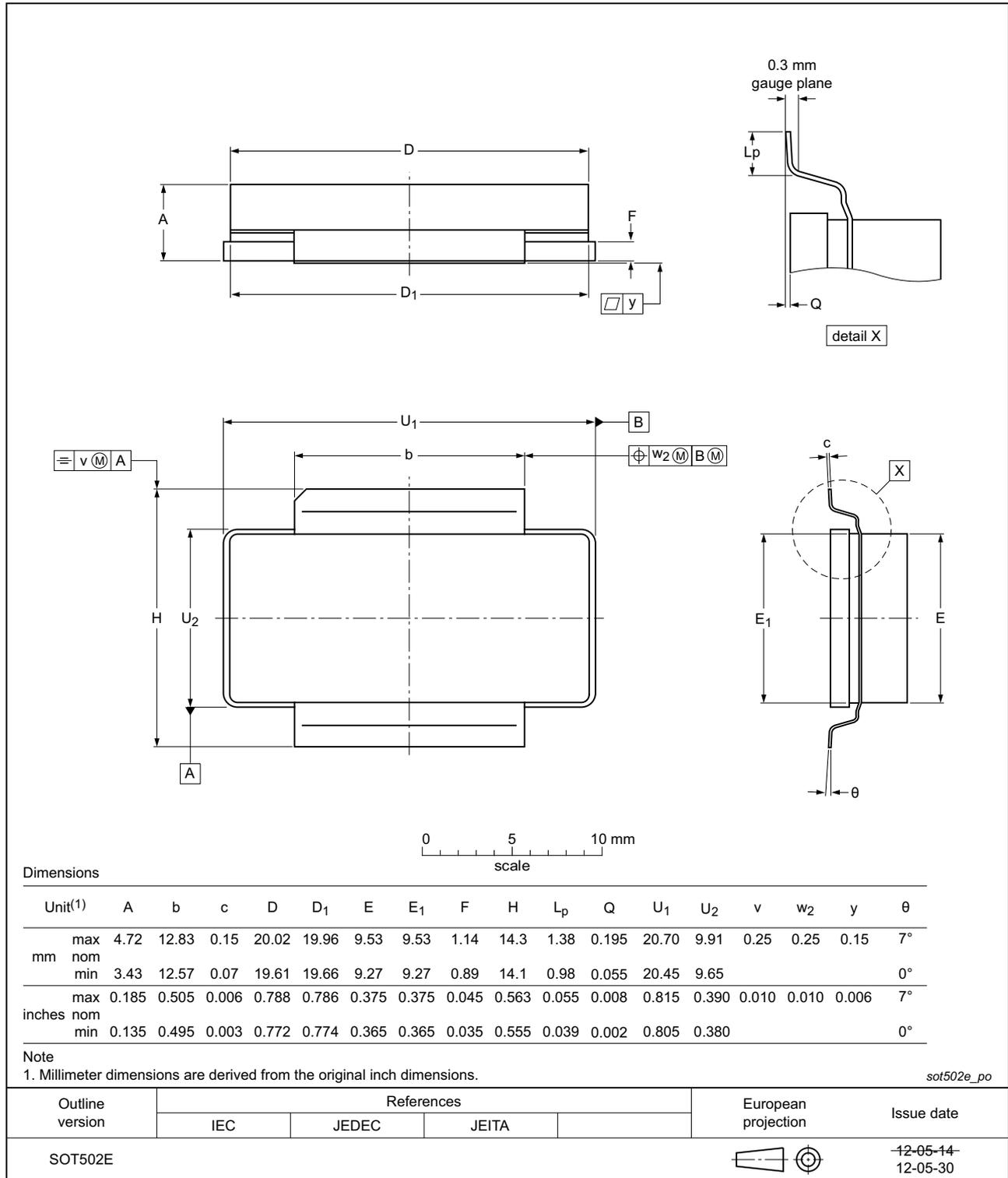


Fig 8. Package outline SOT502E

Eared flanged ceramic package; 2 leads; 2 mounting holes

SOT502F

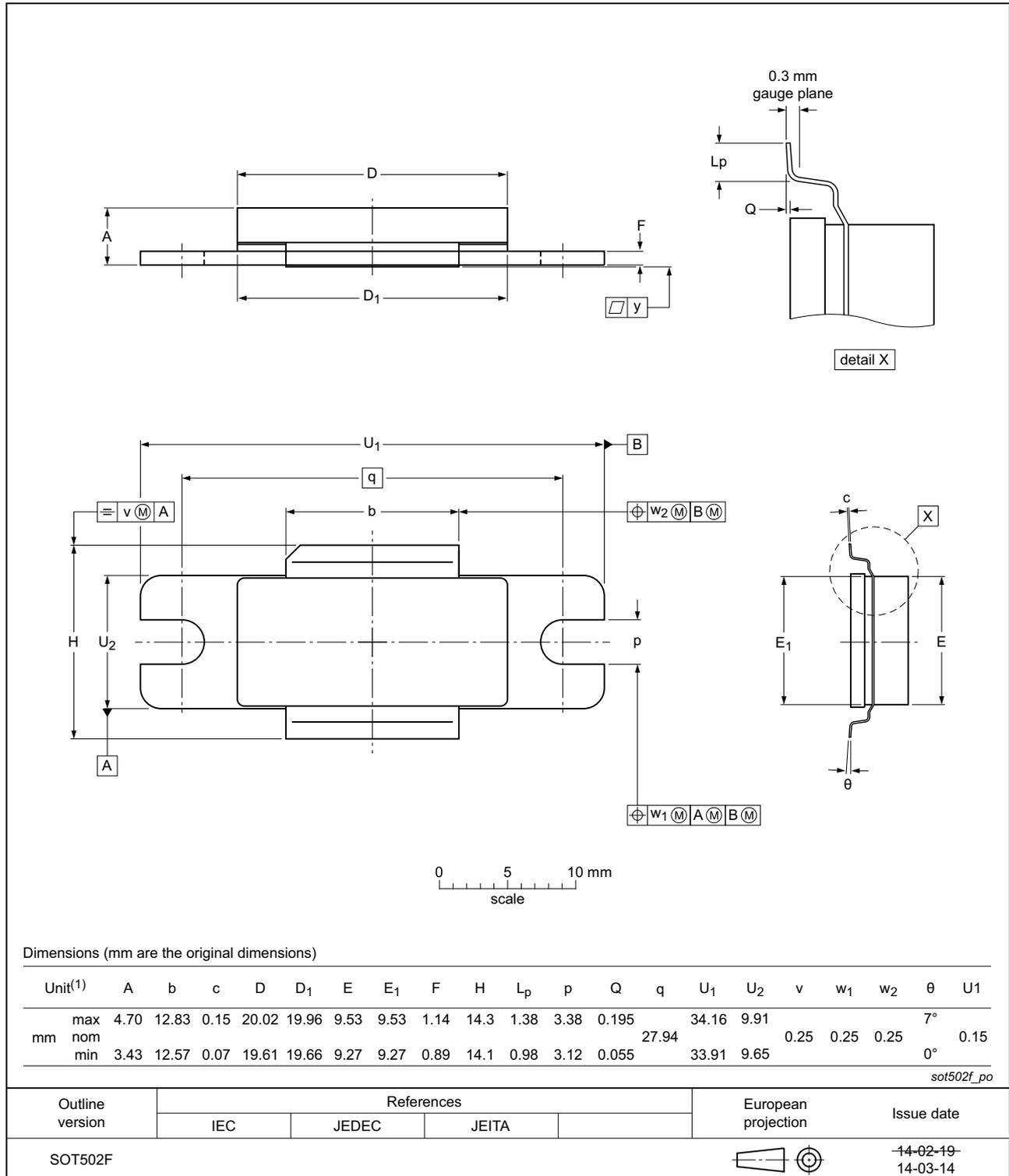


Fig 9. Package outline SOT502F

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 10. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 10. Abbreviations

**Table 11. Abbreviations**

Acronym	Description
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

**Table 12. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA9G1011L-300_LS-300_L-300G_LS-300G v.1	20170725	Product data sheet		-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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