BOS0614 Four-Channel Piezo Haptic Driver with Integrated Sensing

1 Features

- Four-Channel 60 V Low Power Piezo Driver
  - Drives up to four actuators simultaneously
  - Energy Recovery
  - Small Solution Footprint
- Advanced Piezo Sensing Interface
  - 10 kSps Sample Rate
  - 100 µs Detection Latency
  - Zero Power Sensing for Wake-up
  - Automatic Handling of Customized Press and Release Haptic Feedback
  - 220 µV Force Sensing Resolution
- Integrated Digital Front End with I3C/I²C
  - 1024 Samples FIFO
  - 2 kB RAM Waveform Memory
  - Waveform Synthesizer (WFS)
  - 1.2 V to 1.8 V Digital I/O Supply
  - State Retention in SLEEP Mode
- Four GPIOs
  - Open-Drain / Push-Pull
  - Mechanical Button Replacement
  - External Trigger Inputs
- Fast Start-Up Time
- Wide Input Voltage Range of 3 V to 5.5 V

2 Applications

- Smartphones
- Seamless User Interface
- Human-Machine Interface

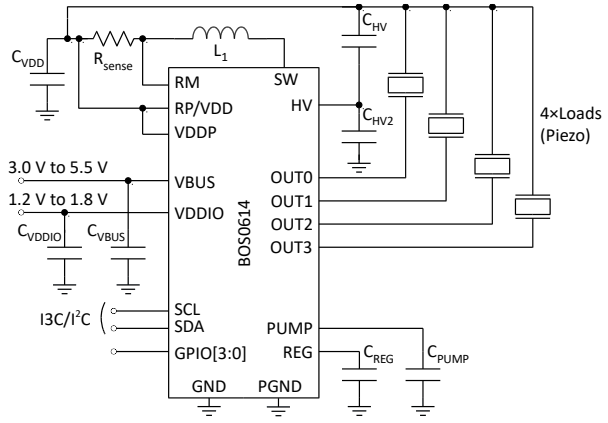

Figure 1: Simplified schematic

3 Description

The BOS0614 is a multi-channel piezo haptic driver based on Boréas' patented CapDrive™ technology. It can drive up to four piezo actuators simultaneously at 60 V. Its Zero Power Sensing (ZPS) capabilities enables the replacement of mechanical buttons in many applications.

The internal 10 kSps sensing interface allows programming of custom press and release haptic feedback on each channel. When detection conditions are met, the BOS0614 can automatically play the programmed haptic feedback and send a notification via four GPIOs within 100 µs. The active-low open-drain configuration of the outputs enable generating signals identical to mechanical buttons for easy integration in a legacy system.

The four GPIOs can be used as an external trigger and connected directly to the outputs of a touch controller to achieve low latency haptic feedback.

Data and configuration can be communicated easily to the BOS0614 through its two-wire MIPI I3C interface. MIPI I3C is backward compatible with I²C for easy integration in most systems. A flexible deep FIFO interface enables the continuous streaming of the digital waveform data for playback or to transmit burst data for more bandwidth efficiency. The interface also integrates a waveform synthesizer and 2 kB RAM waveform memory to generate HD haptic waveforms with minimum communication bandwidth enabling two waveform generation modes: RAM Playback and RAM Synthesis.

Various safety systems protect the BOS0614 from damage in case of a fault.

Table 1: Product information

PART NUMBER	DESCRIPTION
BOS0614CW	WLCSP 30B 2.1mm × 2.5mm

See section 11 for ordering information.

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4 Bumps Configuration and Functions

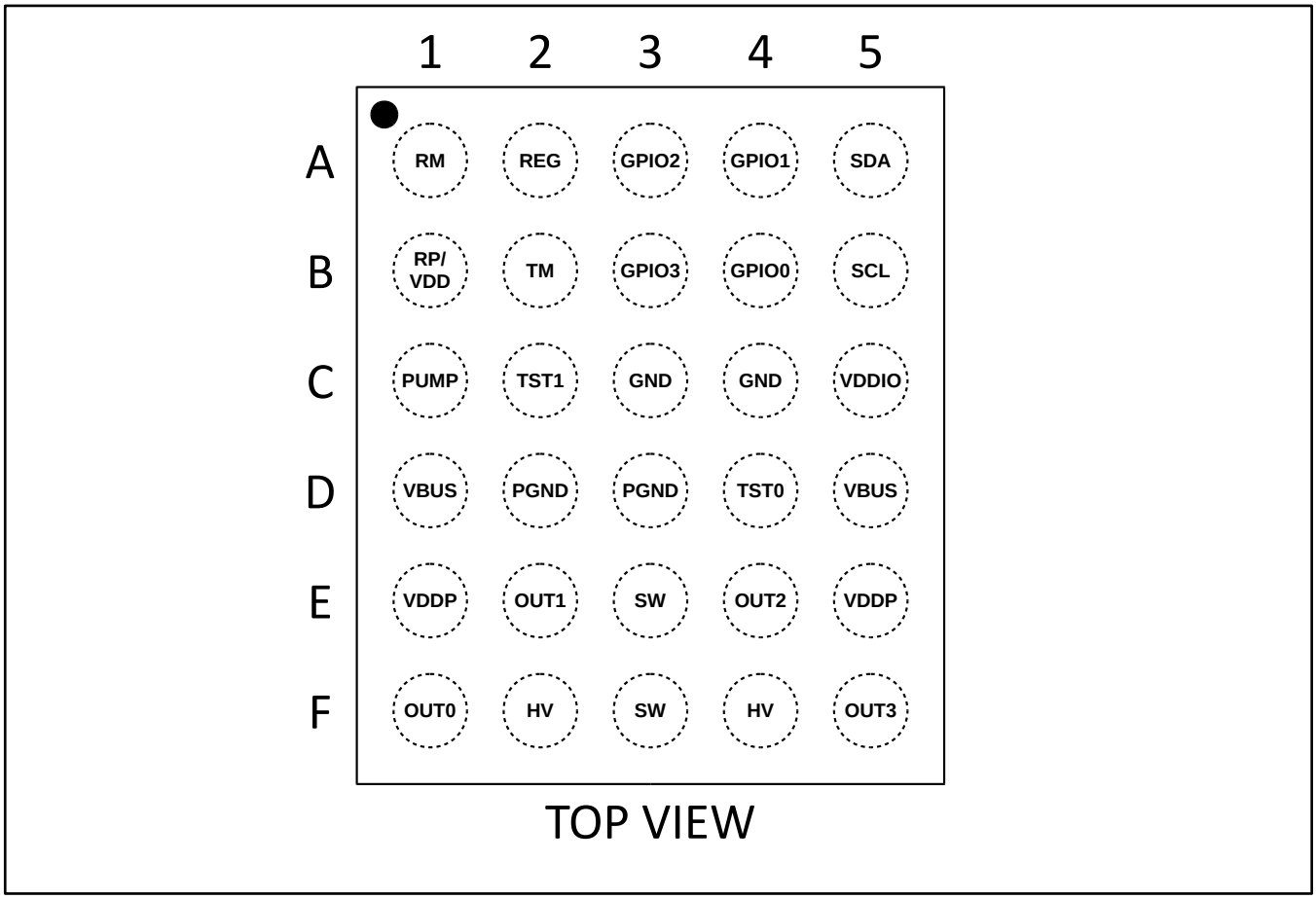


Figure 2: Wafer-Level Chip Scale Package WLCSP 30B 2.1mm × 2.5mm (TOP VIEW; NOT TO SCALE)

Table 2: Pin description

PIN NO.	PIN NAME	TYPE	DESCRIPTION
A1	RM	Input	Current sense negative input
A2	REG	Power	Internal 1.8 V regulator
A3	GPIO2	Input/Output	General-purpose input output
A4	GPIO1	Input/Output	General-purpose input output
A5	SDA	Input/Output	I3C data
B1	RP/VDD	Input/Power	Current sense positive input / Supply
B2	TM	-	Tie to GND
B3	GPIO3	Input/Output	General-purpose input output
B4	GPIO0	Input/Output	General-purpose input output
B5	SCL	Input	I3C clock
C1	PUMP	Power	5V internal charge pump
C2	TST1	-	No connect
C3	GND	Power	Supply ground
C4	GND	Power	Supply ground
C5	VDDIO	Power	Digital I/O supply
D1	VBUS	Power	Main supply voltage
D2	PGND	Power	Supply ground power stage
D3	PGND	Power	Supply ground power stage
D4	TST0	-	No connect
D5	VBUS	Power	Main supply voltage
E1	VDDP	Power	Intermediate supply voltage
E2	OUT1	Output	Piezo output 1
E3	SW	Power	Internal power converter switch pin
E4	OUT2	Output	Piezo output 2
E5	VDDP	Power	Intermediate supply voltage
F1	OUT0	Output	Piezo output 0
F2	HV	Output	HV output
F3	SW	Power	Internal power converter switch pin
F4	HV	Output	HV output
F5	OUT3	Output	Piezo output 3

5 Specifications

5.1 Absolute Maximum Ratings

Table 3: Absolute maximum ratings(1)(2)

	SYMBOL	PARAMETER	MIN	NOM	MAX	UNIT
1		Voltage at pins OUT0, OUT1, OUT2, OUT3, HV, SW	-0.3		70	V
2		Voltage at pins SCL, SDA	-0.3		2.3	V
3		Voltage at all other pins	-0.3		7	V
4	T_{stg}	Storage temperature	-65		150	°C
5	T_J	Operating junction temperature	-40		150	°C

(1) Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
(2) Voltages specified in the table are with respect to GND and PGND unless otherwise stated.

5.2 Recommended Operating Conditions

Table 4: Recommended operating conditions(1)

	SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
1	T_A	Operating Temperature	Operating free-air temp.	-40		85	°C
2	V_{BUS}, V_{DD}, V_{DDP}	Supply voltage		3		5.5	V
3	V_{DDIO} (2)	I/O Supply voltage		1.08		1.98	V
4	$I_{pk\text{-}OUT}$ (3)	Peak transient current per channel	Z_L = 935 Ω, V_{OUT} = 60 V, V_{DD} = 3 V			1	A
5	L_1	Inductance			10		µH
6	R_{sense} (4)	Sense resistor		130			mΩ
7	C_{HV2}	Capacitor on HV pin			1.5		nF
8	f_{OUT}	Output frequency	RAM [1:0] = 0x3	3.9		1000	Hz

(1) Voltages specified in the table are with respect to GND and PGND unless otherwise stated.
(2) Digital I/O voltage (V_{DDIO}) must match the communication interface voltage.
(3) See Figure 13 for SOA and see section 7.4.1 for the maximum current calculation.
(4) R_{sense} value of 130 mΩ limits the current in L_1 inductor and SW pin (I_{pk}) to 2 A. See section 7.4.4 for R_{sense} selection.

5.3 Electrical Characteristics

Table 5: Electrical characteristics. Conditions: T_A = 25°C, V_{BUS} = V_{DD} = V_{DDP} = 3.6 V, V_{DDIO} = 1.8 V (unless otherwise noted)[1]

	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
1	V_{REG}	Voltage at REG pin		1.75	1.80	1.85	V
2	V_{IL}	Digital low-level input voltage	SDA, SCL	-0.3		0.3×V_{DDIO}	V
3	V_{IH}	Digital high-level input voltage	SDA, SCL	0.7×V_{DDIO}		0.3+V_{DDIO}	V
4	V_{OL}	Digital low-level output voltage	SDA, V_{DDIO} < 1.4V SDA, V_{DDIO} ≥ 1.4 V			0.18 0.27	V
5	V_{OH}	Digital high-level output voltage	SDA	0.8×V_{DDIO}			V
6	V_{IL}	Digital low-level input voltage	GPIO0, GPIO1, GPIO2, GPIO3	-0.3		0.54	V
7	V_{IH}	Digital high-level input voltage	GPIO0, GPIO1, GPIO2, GPIO3	1.26		V_{DD}+0.3	V
8	V_{OL}	Digital low-level output voltage	GPIO0, GPIO1, GPIO2, GPIO3			0.18	V
9	V_{OH} [2]	Digital high-level output voltage	GPIO0, GPIO1, GPIO2, GPIO3	0.85×V_{DD}			V
10	t_t	Input transition time of SCL, SDA	VDDIO = 1.8 V, VDDIO = 1.2 V			19.2 72	ns
11	$V_{OUT(FS)}$	Full-scale output voltage		58.8	60	61.2	V
12	I_{Q_VBUS}	V_{BUS} supply quiescent current	SLEEP SLEEP (ZPS 4 Ch.) IDLE[3] IDLE (Sensing 4 Ch.)[4]		4 8 900 1170		µA
13	$I_{VBUS,AVG}$	Average V_{bus} supply current during operation	f_{OUT} = DC V_{OUT} = 60 V C_L = 440 nF		5		mA
			F_{OUT} = 300 Hz V_{OUT} = 60 V C_L = 440 nF		46		mA
14	THD+N	Total Harmonic Distortion + Noise	f_{OUT} = 300 Hz V_{OUT} = 60 V C_{L-Tot} = 875 nF			1	%
15	f_{s-FIFO}	FIFO playback sample rate	PLAY [2:0] = 0x0 PLAY [2:0] = 0x7	1008 7.875	1024 8	1040 8.125	ksps
16	ZTH	Zero Power Sensing (ZPS) Threshold	ZPS_SENS = 0x0 (high sensitivity)		350		mV
			ZPS_SENS=0x1 (low sensitivity)		550		mV

	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
17	PSR	Piezo Sensing Resolution	SENSEDATAx Register (0x18 to 0x1B)		220		µV
18	DHL	Detection to haptic feedback maximum latency	SHORT [1:0] = 0x0			500	µs
19	DGL	Detection to GPIOx notification maximum latency	REP [2:0] = 0x0			100	µs
20	$f_{s\text{-}sens}$	Sensing sample rate per channel	CHx = 0x1		10		kSps

(1) Voltages specified in the table are with respect to GND and PGND unless otherwise stated.
(2) The minimum digital high-level output voltage (V_{OH}) is for push-pull configuration only.
(3) The I_{Q_VBUS} condition IDLE is the quiescent current in IDLE mode with sensing disabled on all channels.
(4) The I_{Q_VBUS} condition IDLE (Sensing 4 Ch.) is the quiescent current in IDLE mode with sensing enabled on all channels.

5.4 Timing Characteristics

5.4.1 I²C

Table 6: Timing characteristics. Condition: I²C communication mode, T_A = 25°C, V_{DDIO} = 1.8 V, SDA/SCL load = 50 pF

	SYMBOL	PARAMETER	FAST MODE		FAST MODE +		UNIT
			MIN	MAX	MIN	MAX	
1	f_{SCL}	SCL clock frequency	0	0.4	0	1.0	MHz
2	t_{LOW}	SCL low period	1300		500		ns
3	t_{HIGH}	SCL high period	600		260		ns
4	t_R	SDA/SCL rise time	20	300	-	120	ns
5	t_F	SDA/SCL fall time	-	300	-	120	ns
6	t_{SU_DAT}	Data setup time	100		50		ns
7	t_{HD_DAT}	Data hold time	0	-	0	-	ns
8	t_{SU_STA}	Setup time for a repeated START condition	600		260		ns
9	t_{HD_STA}	Hold time for a (repeated) START condition	600		260		ns
10	t_{SU_STO}	Setup time for STOP condition	600		260		ns
11	t_{BUF}	Bus free time (time between the STOP and START conditions)	1300		500		ns
12	t_{SPIKE}	Spike suppression pulse width	0	50	0	50	ns

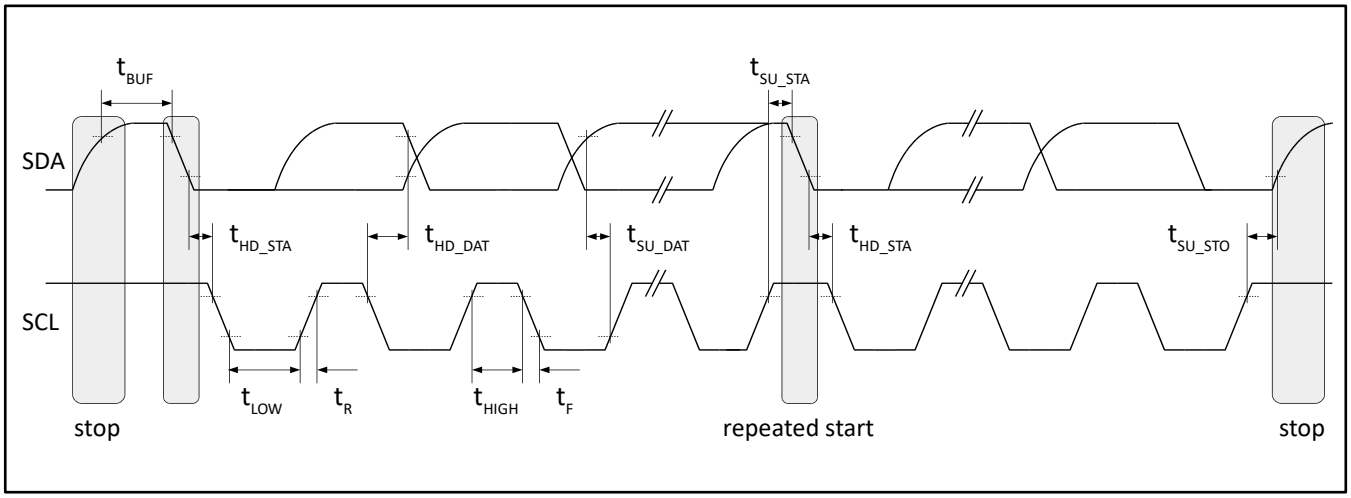


Figure 3: I²C timing diagram

5.4.2 I3C

Table 7: Timing characteristics. Condition: I3C push-pull, T_A = 25°C, V_{DDIO} = 1.8 V, SDA/SCL load = 50 pF

	SYMBOL	PARAMETER	MIN	MAX	UNIT
1	f_{SCL}	SCL clock frequency	0.01	12.5	MHz
2	t_{LOW}	SCL low period	24		ns
3	t_{HIGH}	SCL high period	24	41 (1)	ns
4	t_{CR}	SCL rise time		The minimum between, whether $150\times10^6/f_{SCL}$ or 60	ns
7	t_{CF}	SCL fall time		150e6/ f_{SCL} (60 max.)	ns
8	t_{SU}	Data setup time	3		ns
9	$t_{HD\ (master)}$	Data hold time	t_{CR} +3, t_{CF} +3		ns
10	$t_{HD\ (slave)}$	Data hold time	0		ns
11	t_{CBSr}	Clock before repeated START condition	19.2		ns
12	t_{CAS}	Clock after START condition	38.4		ns
13	t_{CASr}	Clock after repeated START condition	38.4		ns
14	t_{CBP}	Clock before STOP condition	19.2		ns
15	t_{AVAL}	Bus available	1		µs

(1) This maximum high period may be exceeded when the signals can be safely seen by legacy I²C devices.

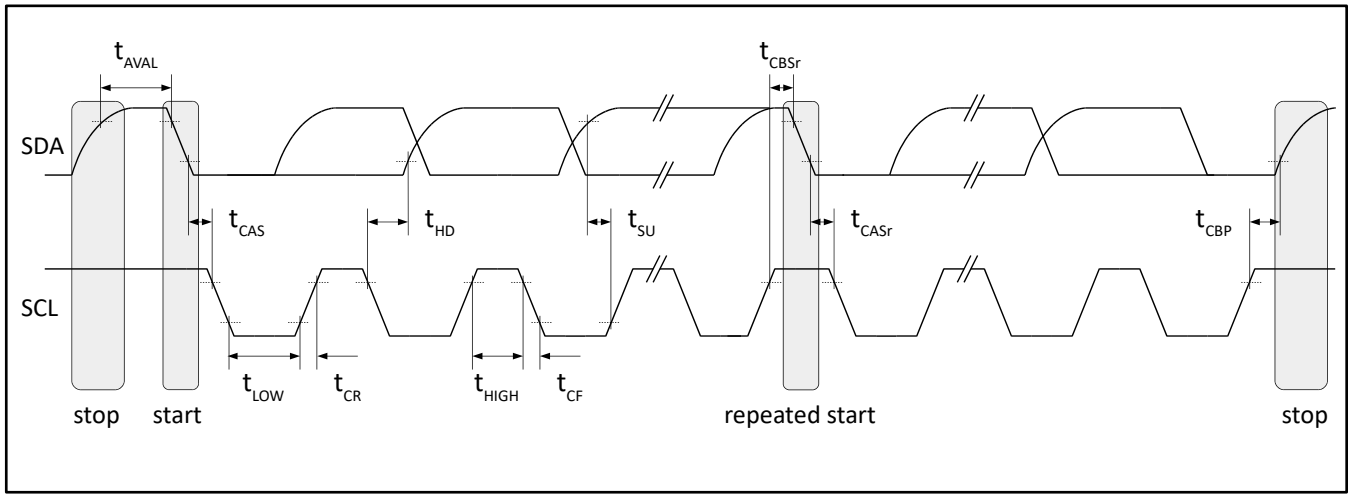


Figure 4: I3C push-pull timing diagram

5.5 Typical Performance Characteristics

Conditions: TA = 25°C, V_{BUS} = 3.6 V, L_1= 10 µH, C_L = 440 nF, f_{OUT} = 300 Hz, V_{OUT} = 60 V sine waveform (unless otherwise noted)

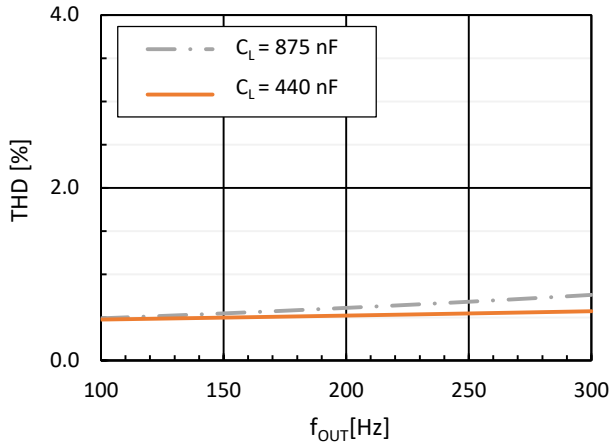


Figure 5: THD vs Output Frequency

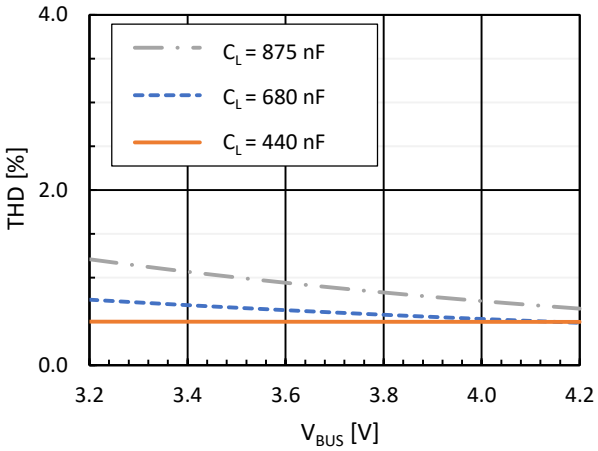


Figure 6: THD vs V_{BUS}

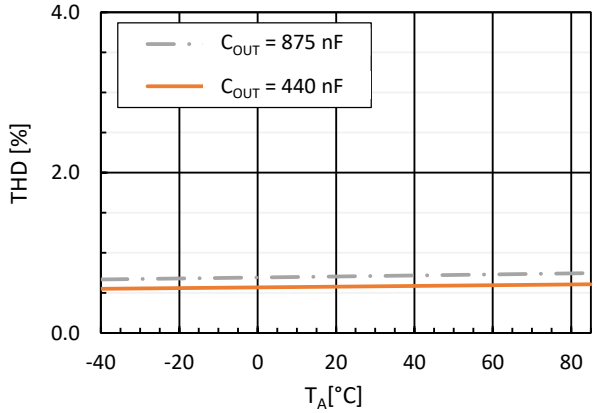


Figure 7: THD vs T_A

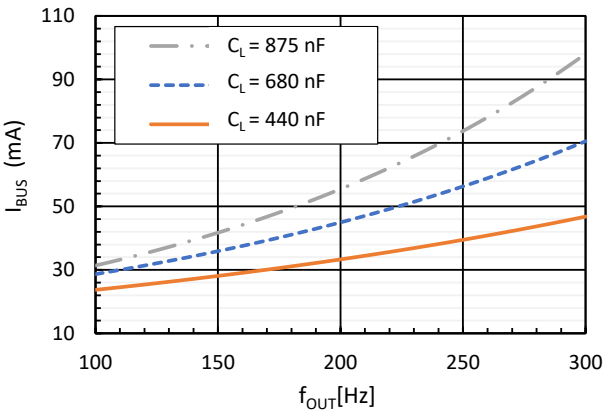


Figure 8: I_{BUS} vs Output Frequency

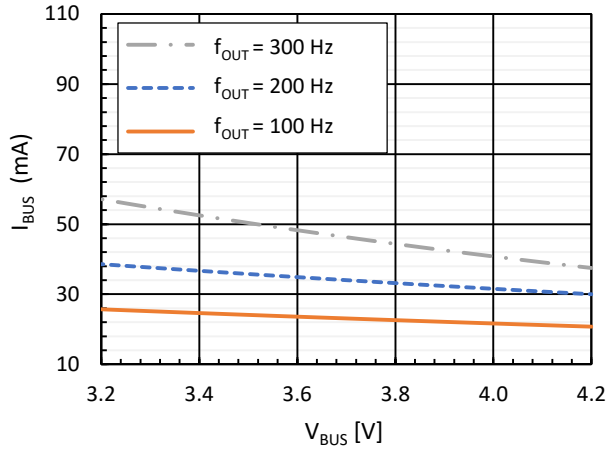


Figure 9: I_{BUS} vs V_{BUS}

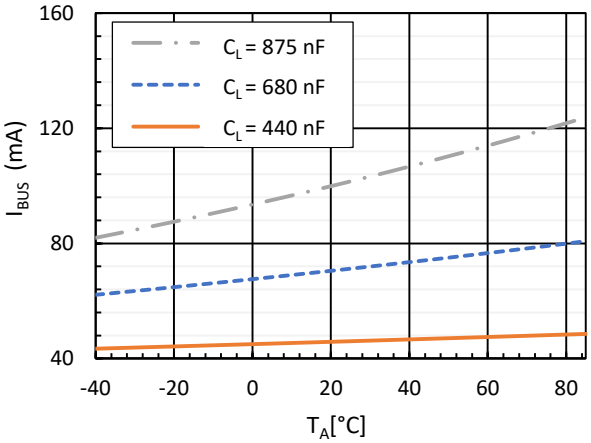


Figure 10: I_{BUS} vs T_A

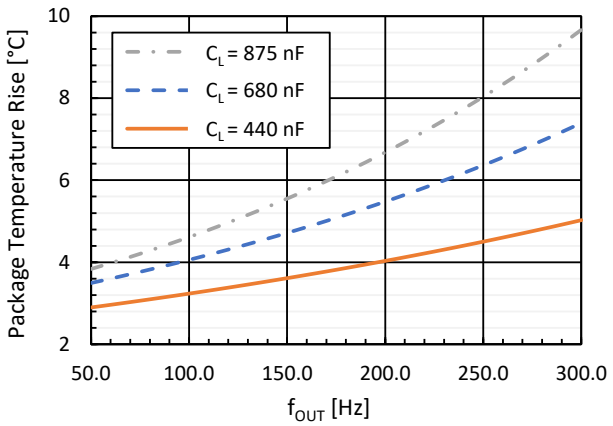


Figure 11: Package Temperature Rise vs Output Frequency

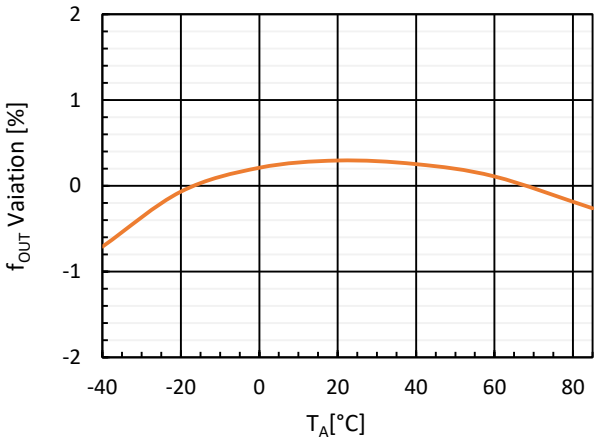


Figure 12: Output Frequency Variation vs T_A

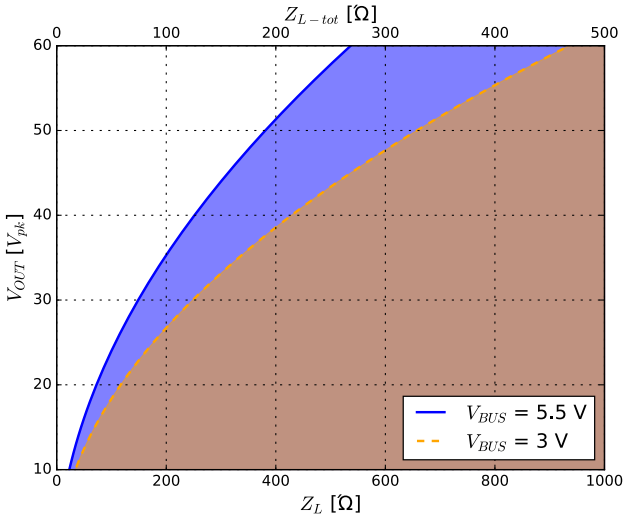


Figure 13: SOA, V_{OUT} vs Per-Channel Load Impedance (Z_L) and Total Load Impedance ($Z_{L\text{-}tot}$)

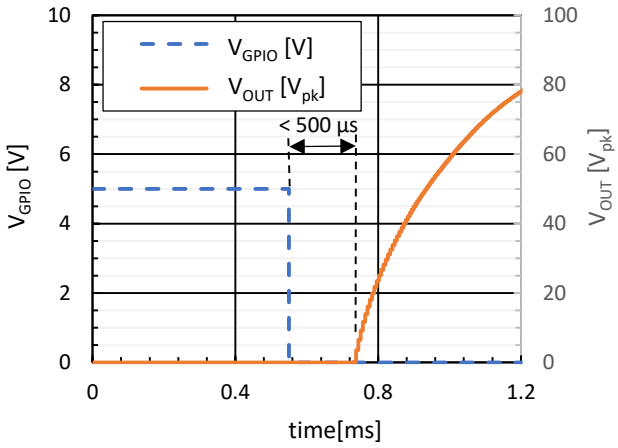


Figure 14: Typical Latency from detection event[1]

[1] The latency is measured from the GPIO falling edge with the according GPIOx [3:0] bits set to 0x1 and SHORT bits set to 0x0.

6 Functional Description

6.1 Overview

The BOS0614 is a highly integrated low-power multi-channel piezo actuator driver with integrated digital front end and advanced sensing interface based on Boréas Technologies patented CapDrive™ technology. The BOS0614 requires a single low-voltage supply and a few passive components to generate waveforms up to 60 V_{pk} on four channels.

The digital interface enables the user to stream the waveform data from any MCU with an I3C or I^2C port to the BOS0614. A flexible FIFO interface enables the generation of haptic playback by streaming the digital waveform data or transmitting burst digital waveform data for more bandwidth efficiency. Waveforms can be generated by reading data from the FIFO at various sample rates. The digital front-end also integrates a Waveform Synthesizer (WFS) and 2 kB on-chip RAM with two waveform generation modes: RAM playback and RAM synthesis. These two modes allow the generation of haptic waveforms with minimal intervention from the host MCU.

The BOS0614 integrates a 10 kSps advanced sensing interface that allows the creation of systems with up to four piezo actuators that can replace mechanical buttons and provide an enhanced user interface. Piezo actuator press/release trigger conditions can be programmed for each channel to detect that a user pressing a piezo actuator with 100 µs latency and automatically trigger a haptic waveform feedback. All four GPIOs can be configured as active low open-drain outputs, facilitating the replacement of mechanical buttons with piezo actuators. Finally, a Zero Power Sensing (ZPS) feature allows a piezo actuator press detection event to wake up the BOS0614 from SLEEP mode.

The BOS0614 is designed to operate with a 10 µH inductor. The L_1 inductor value can be adjusted to achieve an optimal power / size / performance trade-off for a given application. See section 7.4.3 for more details.

With a start-up time of less than 500 µs from SLEEP mode, the BOS0614 can be used in applications where low latency is critical such as touch-enabled devices.

6.2 Features

6.2.1 Digital Front-End Interface

The BOS0614 uses an I3C slave interface supporting SDR communication up to 12.5 Mbps. This high-speed communication interface enables multiple ICs to share a common communication bus. The BOS0614 digital front-end enables waveform data to be stored in memory. The digital interface also provides access to internal registers which control the BOS0614 operation and performance, see section 6.3 for more details.

6.2.2 GPIO

Four general-purpose input / output (GPIOs) are available supporting push-pull (between VDD and GND) or open-drain configuration (a 1.5 kΩ pull-up resistor or greater is required between VDD and GPIO pins). These GPIOs can be used to replace mechanical button switches in legacy systems, as interruption to notify the host MCU of various events such as haptic detection events, or as input to trigger haptic waveform output.

6.2.3 Flexible Waveform Generation

6.2.3.1 Direct Mode

With bits RAM [1:0] set to 0x0, the haptic waveform samples are played as they are sent from the host MCU to the RAM using REFERENCE register. The rate at which the RAM data is read to generate the haptic waveform is set by bits PLAY [2:0]. See section 6.4 for details.

6.2.3.2 FIFO Mode

The digital front-end gives access to a 1024-sample FIFO for waveform playback with bits RAM [1:0] set to 0x1. FIFO entries are appended every time waveform samples are written in the REFERENCE register. Digital samples are represented as 12-bit unsigned values. If bit OE is set to 0x1, the FIFO entries are read automatically out of the FIFO at a rate set by bits PLAY [2:0]. See section 6.5 for details.

6.2.3.3 RAM Playback Mode

The RAM Playback mode is selected with bits RAM [1:0] set to 0x2. In the RAM Playback Mode, the on-chip RAM of 2 kB is used to store haptic waveforms as waveform amplitude samples in 12-bit unsigned format. The waveform is sampled at a rate set by bits PLAY [2:0]. See section 6.6 for more details.

6.2.3.4 RAM Synthesis Mode

The RAM Synthesis mode is selected with bits RAM [1:0] set to 0x3. With this mode, the BOS0614 uses the Waveform Synthesizer (WFS) to generate waveforms using parameters stored in the 2 kB RAM. The RAM Synthesis mode allows the generation of sinusoidal waveforms of various amplitudes and frequencies without having to send every sample of the waveform to RAM as is the case with RAM Playback mode. This allows to produce complex waveforms with minimal data communication. See section 6.7 for details.

6.2.4 Adjustable Internal Clock

The BOS0614 internal clock oscillator frequency is trimmed during fabrication (using hardware fuses, see Figure 36) and the TRIM register allows it to be adjusted. This feature can be used to match the external system clock frequency with the BOS0614 internal clock frequency, which is used to determine the FIFO read-out rate. This might be needed to minimize waveform distortion due to data loss when the host MCU writes waveform samples at a constant rate to the FIFO. To successfully adjust oscillator frequency, bit OE must be set to 0x0.

Note that changing the internal oscillator frequency may induce circuit malfunction and is not recommended for normal operation.

The internal oscillator can be adjusted with the following sequence:

1. Set OE bit to 0x0.
2. Set TRIM.TRIMRW [1:0] bits to 0x2.
3. Wait for 1 ms.
4. Read TRIM.TRIM_OSC [6:0] bits to read the internal oscillator trim value specific to the current chip.
5. Set TRIM.TRIM_OSC [6:0] bits to the desired value and set TRIM.TRIMRW [1:0] bits to 0x3.

The same procedure can be used to adjust the internal 1.8V regulator voltage using bit TRIM_REG [2:0] instead of TRIM_OSC [6:0].

6.2.5 SLEEP Mode

When no output waveform is being requested (bit OE set to 0x0), the BOS0614 can enter in one of the two low power modes: IDLE or SLEEP mode. Bit DS sets the BOS0614 power mode when no output waveform is requested. By default, the power mode is IDLE (bit DS set to 0x0). SLEEP mode is selected when bit DS is set to 0x1. In SLEEP mode, the BOS0614 is in its lowest power state and all registers, and the RAM hold their values. In I3C, the dynamic address assignment can be performed without waking up the BOS0614.

The device can wake up from SLEEP mode by either a ZPS event (as detailed in section 6.2.9) or a communication on I^2C/I3C bus (the data will not have any effect on the configuration of the registers).

Refer to section 7.3.3 for the detailed start-up sequence from SLEEP mode.

6.2.6 Device Reset

The BOS0614 has software-based reset functionality. When bit RST is set to 0x1, all registers are set to their default value and the BOS0614 goes into IDLE mode. Note that if a waveform was playing when resetting, output goes back to 0 V.

6.2.7 Low Latency Startup

The BOS0614 features a fast start-up time. From IDLE or SLEEP mode, the device takes approximately 500 µs to start playing the waveform when auto-calibration piezo zeroing is set to 500 µs with SHORT [1:0] bits set to 0x0 (see Figure 14). This makes the BOS0614 a very small contributor to system latency.

6.2.8 High Resolution Piezo Actuator Sensing

The digital front-end gives access to internal registers (addresses 0x06 to 0x1F) to configure the output channels to sense signals that can trigger detection events and haptic waveform playback.

As an example, the input signal of a piezo actuator connected to OUT0 (F1) which has been pressed could trigger an automatic waveform feedback on the channel using one of the waveform generation mode (section 6.2.3) to mimic the feel of a mechanical button. See section 6.8 for more detail on the sensing configuration.

The sensing resolution of the BOS0614 is 220 µV which enables the design of very sensitive touch interface.

6.2.9 Zero Power Sensing

Channels with the Piezo Sensing feature enabled (see section 6.8) can wake the BOS0614 from SLEEP (if bit DS is set to 0x1). This feature allows the BOS0614 to be in SLEEP mode while still benefiting from

sensing capability. The Zero Power Sensing (ZPS can be configured with low or high sensitivity using the bit ZPS_SENS. The following conditions apply:

- The sensing must be enabled on desired channels using SENSECONFIG [3:0] bits (see section 6.8).
- If bit ZPS is set to 0x0, the BOS0614 wakes-up from SLEEP when the actuator is pressed and the configured sensing conditions on the channel is also successful. If the sensing condition on the channel is not met within 100 ms, the BOS0614 will go back into SLEEP mode.
- If bit ZPS is set to 0x1, the BOS0614 wakes-up from SLEEP when the actuator is pressed without trigger conditions. This configuration is not recommended as it may cause the device to behave unpredictably when it wakes-up from SLEEP using a valid communication on its I^2C/I3C interface.
- When BOS0614 wakes-up from SLEEP with a ZPS event and the actuator is pressed and then released (met the configured release conditions), the MCU must initiate a valid communication on the I^2C/I3C interface within 100 ms, or the BOS0614 will return into SLEEP mode.

See section 7.3.3 for more detail on start-up sequence.

6.2.10 Input Trigger

Each GPIO pin can be used as a trigger input to initiate a predefined haptic waveform, by setting the EXT_TRIG bit to 0x1. This is useful for enabling low-latency communication between a sensor and the BOS0614 by bypassing the MCU. The waveform trigger is based on the GPIO pin state rather than a edge trigger. Note that any input trigger will be ignored while the device is in SLEEP mode.

The followings registers need to be set to configure the haptic waveform triggering using the GPIO:

- TC.POL sets the GPIO input signal polarity required to initiate a predefine haptic waveform.
- SENSEx.WVP [2:0] and SENSEx.WVR [2:0] (registers 0x07, 0x0B, 0x0F and 0x13) define the waveform to play (see Table 16) depending on the GPIOx pin input state and bit TC.POL (as detailed in Table 8 and Table 9).
- AUTOP and AUTOR of any of the sensing channel (registers 0x07, 0x0B, 0x0F and 0x13), enables the automatic haptic waveform start.
- GPIO.GPIOx must be set to 0x7.
- SENSECONFIG.EXT_TRIG must be set to 0x1.

Table 8: WVP [2:0] and WVR [2:0] GPIO Trigger Conditions by GPIO for TC.POL = 0x1

SEQUENCE #	GPIOx PIN INPUT STATE	STATE OF ASSOCIATED PRESS_RELEASE [3:0] BIT		PLAY WVP [2:0] WAVEFORM?	PLAY WVR [2:0] WAVEFORM?
1	0	0x0	Released	No	No
2	1	Switch to 0x1	Pressed	Yes	No
3	0	0x1	Pressed	No	No
4	1	Switch to 0x0	Released	No	Yes
5	0	0x0	Released	No	No

Table 9: WVP [2:0] and WVR [2:0] GPIO Trigger Conditions by GPIO for TC.POL = 0x0

SEQUENCE #	GPIOx PIN INPUT STATE	STATE OF ASSOCIATED PRESS_RELEASE [3:0] BIT		PLAY WVP [2:0] WAVEFORM?	PLAY WVR [2:0] WAVEFORM?
1	1	0x0	Released	No	No
2	0	Switch to 0x1	Pressed	Yes	No
3	1	0x1	Pressed	No	No
4	0	Switch to 0x0	Released	No	Yes
5	1	0x0	Released	No	No

6.2.11 Low-Latency Piezo Button Interface

With the GPIOs configured as open-drain (i.e., bit OD set to 0x1), piezo actuators connected to the BOS0614 channels can replace mechanical buttons. The GPIOx output will be set to high state when the piezo actuator is not pressed (associated PRESS_RELEASE [3:0] bit is set to 0x0) and low state when the piezo actuator is pressed (associated PRESS_RELEASE [3:0] bit is set to 0x1).

Thanks to the combination of the native 10 kSps sample rate per channel and its advanced built-in detection algorithm, the BOS0614 can notify the MCU of a press or release event within 100 µs.

6.2.12 Adjustable Current Limit

The maximum current of the power converter must be limited to avoid damage to the inductor by selecting the proper R_{sense} value for the selected inductor (see section 7.4.4). Current flowing in the inductor is sensed by measuring the voltage drop across the series resistor R_{sense} placed between pins RP and RM.

6.2.13 Energy Recovery

The BOS0614 architecture enables the recovery of the energy accumulated on the capacitive load (piezo) and transfers it back to its input (VDD), which makes the BOS0614 power efficient. The internal controller determines the direction of the power flow during waveform playback. This imposes requirements on the selection of C_{VDD} input capacitor (see section 7.4.5). It may also require the use of the Unidirectional Power Input (i.e., bit UPI set to 0x1, see section 6.2.14) features depending on the characteristic of the power delivery network connected to the BOS0614.

6.2.14 Unidirectional Power Input

The BOS0614 can sink and source current from the power delivery network (PDN) during normal operation due to its energy recovery feature (see section 6.2.13 for more detail). Configuring the Unidirectional Power Input (bit UPI set to 0x1), which enables the BOS0614 to appear as a resistive load to the power supply (BOS0614 only sinks current), see Figure 15. This is useful when the power delivery network can`t sink current or to reduce RMS current flowing in the PDN. This feature causes the following to happen:

- First, power is drawn from the input source (VBUS) when the amplitude of the output waveform increases.
- Second, energy recovered accumulates on the input capacitor (C_{VDD}) increasing its voltage when the amplitude of the output waveform decreases.

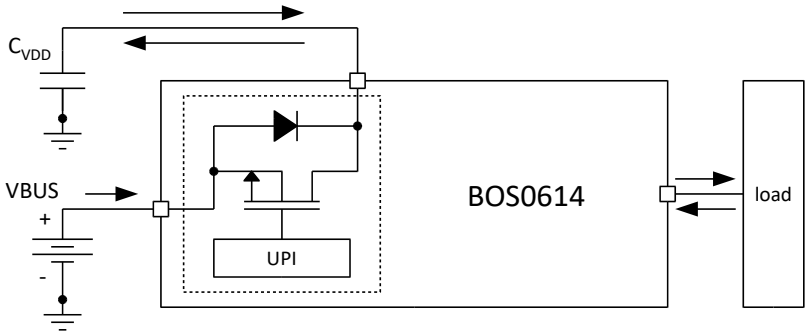


Figure 15: Block diagram of the Unidirectional Power Input (UPI)

As shown on Figure 16, energy accumulation on the input capacitor causes the input voltage (VDD) to increase See section 7.4.5 for details on selecting the input capacitor. The voltage on the input capacitor shall never exceed the VDD maximum operating voltage of 5.5 V.

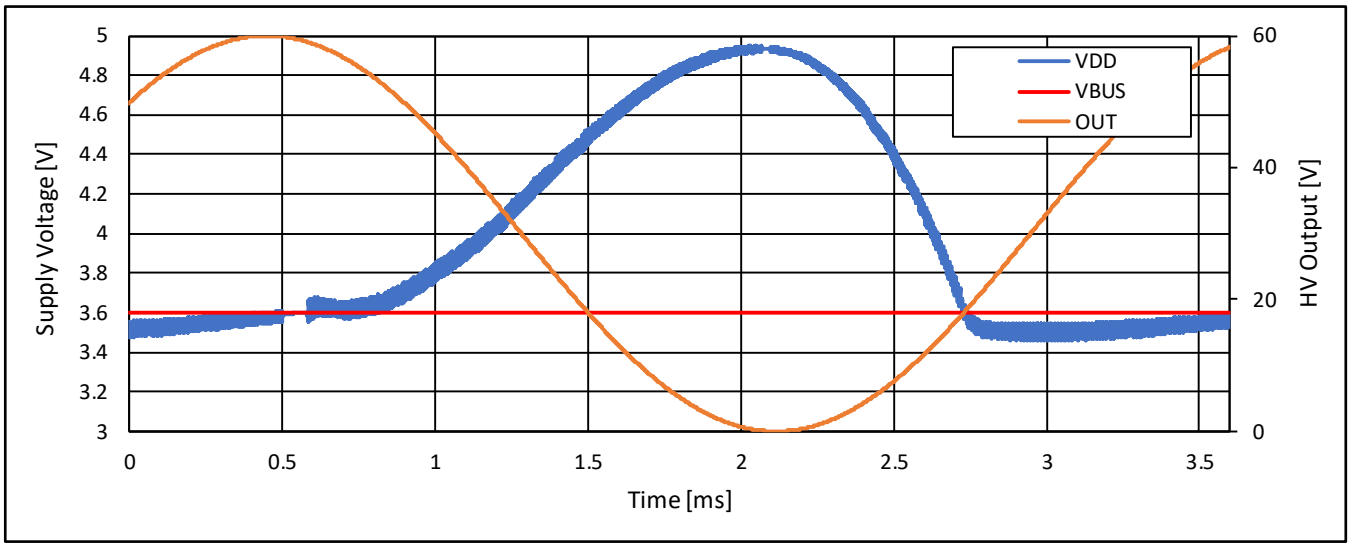


Figure 16: VDD voltage increase during energy recovery when bit UPI is set to 0x1. C_{VDD} = 100 µF, C_L = 400 nF

6.2.15 Fault Behaviour

This section lists the faults and their behaviours.

6.2.15.1 Overvoltage

If an overvoltage condition at one of the output pins OUT0 (F1), OUT1 (E2), OUT2 (E4) or OUT3 (F5) is detected during waveform generation (i.e., voltage higher than approximately 65 V), the following occurs:

- Bit OVV is set
- Bits STATE [1:0] is changed to 0x3 (ERROR state)
- OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) voltage ramp down to VDD

The bit OVV will clear automatically and the BOS0614 state will change for IDLE mode (bits STATE [1:0] set to 0x0) with the following conditions:

- Bit OE is 0x0
- Voltage on OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) is lower than the maximum allowed $V_{OUT(FS)}$

6.2.15.2 Output Short Circuit

The BOS0614 has an output short circuit protection to prevent excessive current to flow because of a shorted load. In case the short circuit condition is detected, the following occurs:

- Bit SC is set
- Bits STATE [1:0] is changed to 0x3 (ERROR state)
- OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) voltage ramp down to VDD

The bit SC will clear automatically and the BOS0614 state will change for IDLE mode (bits STATE [1:0] is 0x0) with the following conditions:

- Bit OE is 0x0
- Voltage on OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) is lower than the maximum allowed $V_{OUT(FS)}$

6.2.15.3 Over Temperature

The BOS0614 has an internal temperature sensor that puts the BOS0614 in ERROR state in case the die junction temperature exceeds 145 °C. In this case, the following occurs:

- Bit OVT is set
- Bits STATE [1:0] is changed to 0x3 (ERROR state)
- OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) voltage ramp down to VDD

Bit OVT will clear automatically and the BOS0614 state will change for IDLE mode (bits STATE [1:0] is 0x0) with the following conditions:

- Bit OE is 0x0
- Voltage on OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) is lower than the maximum allowed $V_{OUT(FS)}$

The low power dissipation of the BOS0614 makes it unlikely that its temperature will reach 145 °C even when it is continuously operated at the maximum C_L in the operating temperature range T_A.

6.2.15.4 Brownout

The BOS0614 has internal brownout protections and if V_{REG} goes below 1 V, the following occurs:

- The chip issues a reset signal, and all registers are set to their default values

When V_{REG} goes back to its specified operating voltage, the BOS0614 state goes into IDLE mode (bits STATE [1:0] is 0x0).

6.2.15.5 Under Voltage

The V_{BUS} is monitored, and its voltage is below 2.875 V during waveform generation the following occurs:

- Bit UVLO is set
- Bits STATE [1:0] is changed to 0x3 (ERROR state)
- OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) voltage ramp down to VDD

Bit UVLO will clear automatically and the BOS0614 state will change for IDLE mode (bits STATE [1:0] is 0x0) with the following conditions:

- Bit OE is 0x0
- Voltage on OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) is lower than the maximum allowed $V_{OUT(FS)}$

6.2.15.6 Current Detection Status

For proper operation, the BOS0614 monitors the current using RP (B1) and RM (A1) pins and R_{SENSE} resistor. If no current is detected during waveform generation, the following occurs:

- Bit IDAC is set
- Bits STATE [1:0] is changed to 0x3 (ERROR state)

Typically, IDAC is set when R_{SENSE} or L_1 is disconnected. Bit IDAC will reset when current is detected.

The BOS0614 will recover from ERROR state and change for IDLE mode (bits STATE [1:0] is 0x0) with the following conditions:

- Bit OE is 0x0
- Voltage on OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) is lower than the maximum allowed $V_{OUT(FS)}$

6.2.16 Output Timeout

Setting bit TOUT to 0x1 enables a timeout mechanism that forces the BOS0614 into SLEEP mode if no new communication has been received within 4 ms while playing a waveform in Direct Mode (bits RAM [1:0] set to 0x0) or FIFO Mode (bit RAM [1:0] set to 0x1). More specifically, the BOS0614 enter into SLEEP mode when the following conditions are met:

- Bit TOUT is set to 0x1.
- Bit OE is set to 0x1.
- Bits RAM [1:0] are set to 0x0 or 0x1.
- The FIFO is empty when using FIFO mode (bits RAM [1:0] set to 0x1).
- BOS0614 did not receive any communication on its digital interface for more than 4 ms.

6.3 Digital Interface

A MIPI I3C slave port enables communication with the BOS0614. I3C is backward compatible with legacy I^2C devices, but I3C bus supports significantly higher speed. It is used to write data to the registers, whose content can also be read back.

6.3.1 General Communication Protocol

The host MCU transfers data using I3C or I^2C standards. Both protocols can do write transactions with the following steps:

- The start bit (0), followed by the 7-bit I^2C address of the BOS0614 (0x2C), followed by the $R/\overline{W}$ bit (0).
- An 8-bit word is sent containing the register address corresponding to the register to write to.
- The register address is followed by two bytes of data to be written. The first byte sent corresponds to the MSBs of the register data and the second byte corresponds to the LSBs of register data. Three cases exist where more than one register can be written:
    1. Register address = 0x00: All subsequent 2-byte words will automatically be written to the REFERENCE register. The communication frame must be stopped to access other registers.
    2. Register address other than 0x00 and STR = 1: The register address will be automatically incremented every two bytes to allow writing multiple registers in the same transmission

frame and reduce the number of bits used in the communication. The communication frame must be stopped to skip register addresses.

3. Register address other than 0x00 and bit STR set to 0x0: After every two bytes of data, a byte of address corresponding to the next target register must be sent.

Both protocols can also do read transactions with the following steps:

- The start bit (0), followed by the 7-bit I²C address of the BOS0614 (0x2C), followed by the $R/\overline{W}$ bit (0).
- Each read request will return two bytes of data corresponding to the register set in BC [7:0].

6.3.2 I3C

The I3C slave functionality implemented in the BOS0614 is based on MIPI® Alliance Specification for I3C℠, version 1.0. I3C is a 2-wire bidirectional serial bus which always has one master and one or more slaves. The two wires are designated SDA and SCL: SDA is a bidirectional data signal, SCL is a clock signal. They connect respectively to BOS0614 SDA and SCL pins.

Table 10: Serial interface pin description

PIN NAME	PIN DESCRIPTION
SDA	Bidirectional Data Signal
SCL	Master Clock Signal

I3C communication is initiated by the master which generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. All I3C communication occurs within a frame. The basic frame begins with a START, followed by the header, the data, and a STOP, see Figure 17. The header following a START allows for bus arbitration. The master uses the header to address slave device(s). Each slave is addressed by a unique 7-bit slave address plus a read-write bit.

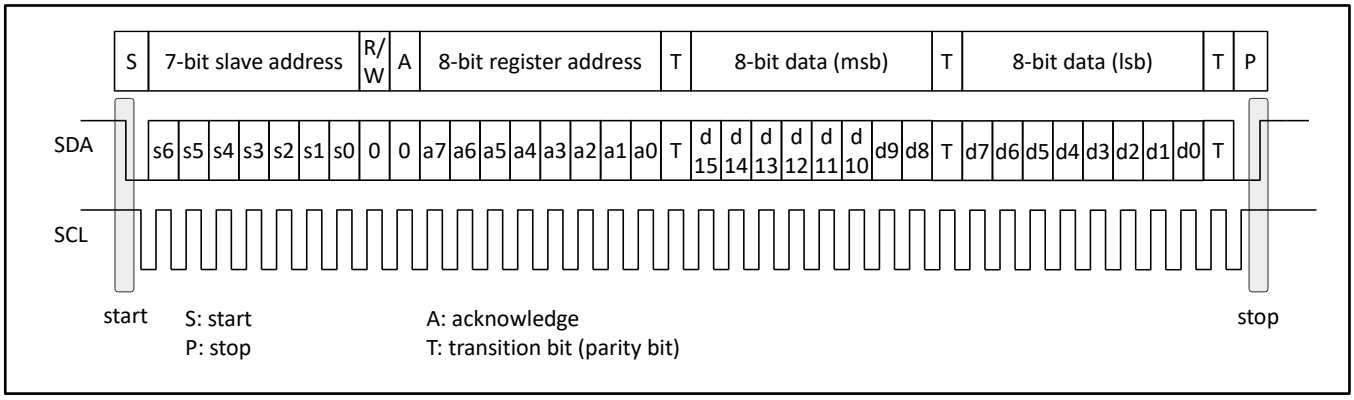


Figure 17: Typical I3C Write communication frame

I3C bus uses transitions on SDA while the clock is at logic high to indicate START and STOP conditions. A high-to-low transition on the SDA signal indicates a START, and a low-to-high transition indicates a STOP. All devices share the same SDA signals through a bidirectional bus using a wired-AND connection. Data transition on SDA must occur during the low time of the clock period.

The BOS0614 I3C slave has a legacy I²C static address (7'h2C) implemented. The BOS0614 will act as an I²C slave using address 7'h2C until it is assigned a dynamic address. Once a dynamic address has been assigned, the BOS0614 will only operate as an I3C Slave unless it is reset.

A 50 ns spike filter is included in the BOS0614. By default, the spike filter is active at power up. To operate in I3C, the broadcast address 0x7E need to be written at I^2C speed. The filter will automatically be deactivated, and the I3C communication speed can be used.

BOS0614 I3C interface is compliant with MIPI® Alliance Specification for $I3C^{SM}$, version 1.0. It features the following:

1. Slave only
2. SDR (Single Data RATE) up to 12.5 MHz
3. I^2C compatibility with static address: 7'h2C
4. Supports basic Common Command Codes (CCC) (see Table 11 for detail)
5. Does not support Hot Join (HJM)
6. Does not support In-Band Interrupt (IBI)
7. Provisional ID = 0x08a206840000
    a. Manufacturer ID = 0x0451
    b. Part ID = 0x0684
    c. Instance ID = 0
    d. Vendor ID = 0
8. Bus Characteristic Register = 0x00
9. Device Characteristic Register = 0x25

Table 11: Common Command Codes (CCC) support

COMMAND NAME	TYPE	CODE	DESCRIPTION
ENEC	Broadcast	0x00	Enable events command
DISEC	Broadcast	0x01	Disable events command
ENTAS0	Broadcast	0x02	Enter activity state 0
ENTAS1	Broadcast	0x03	Enter activity state 1
ENTAS2	Broadcast	0x04	Enter activity state 2
ENTAS3	Broadcast	0x05	Enter activity state 3
RSTDAA	Broadcast	0x06	Reset dynamic address assignment
ENTDAA	Broadcast	0x07	Enter dynamic address assignment
ENEC	Direct	0x80	Enable events command
DISEC	Direct	0x81	Disable events command
ENTAS0	Direct	0x82	Enter activity state 0
ENTAS1	Direct	0x83	Enter activity state 1
ENTAS2	Direct	0x84	Enter activity state 2
ENTAS3	Direct	0x85	Enter activity state 3
RSTDAA	Direct	0x86	Reset dynamic address assignment
SETNEWDA	Direct	0x88	Set new dynamic address
GETPID	Direct	0x8D	Get provisional ID
GETBCR	Direct	0x8E	Get bus characteristics register
GETDCR	Direct	0x8F	Get device characteristics register
GETSTATUS	Direct	0x90	Get device status
GETHDRCAP	Direct	0x95	Get HDR Capability

The BOS0614 will operate as an I3C Slave only after it is assigned a dynamic address by the master. Address assignment (command ENTDAA) must be performed with I^2C timing or a dummy write to

address 0x7E must be performed prior to ENTDAA to clear the 50 ns spike filter and enable communication at I3C speed.

A typical write sequence from power up is the following:

1. Send start condition with broadcast address 0x7E at I²C speed to clear I²C spike filter
2. ENTDAA
3. Wake-up the chip with a dummy write
4. Configure registers as needed

6.3.3 I²C

The BOS0614 acts by default as an I²C slave using its static address (7'h2C). Figure 18 shows a basic data-transfer sequence with I²C static addressing. Following a START, the master device generates the 7-bit slave address and the read-write (R/W) bit to communicate with a slave device. The slave device then holds the SDA signal low during the next clock period to indicate acknowledgment to the master. When this acknowledgment occurs, the master transmits the next byte(s) of the sequence.

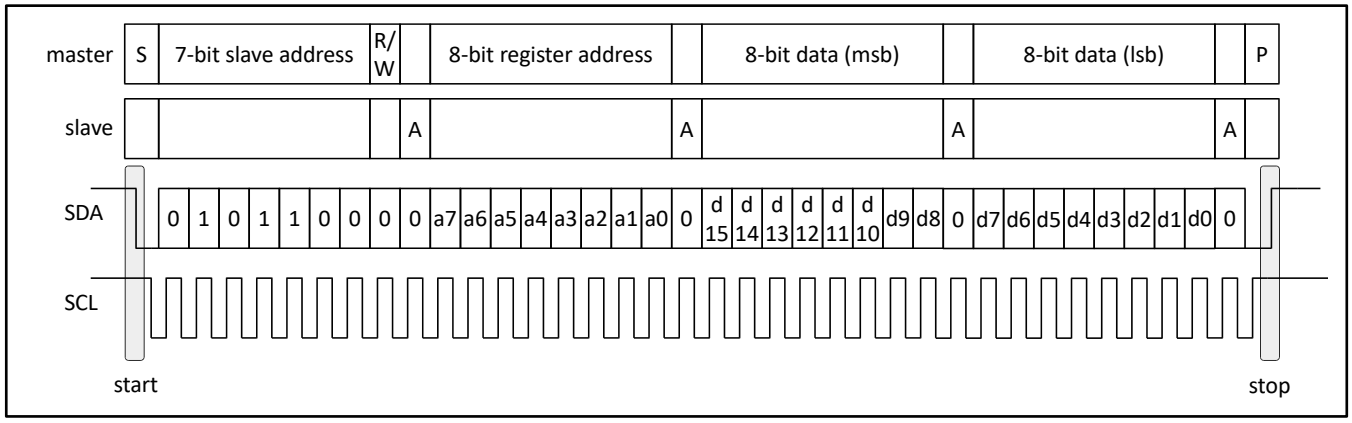


Figure 18: Basic data transfer write sequence with I²C static addressing

Figure 19 lists the possible communication sequences in I²C mode. MSB is always sent first.

A typical write sequence from power up is the following:

1. Write with static address 0x2C with dummy data to wake-up the BOS0614
2. Configure registers as needed

A 50 ns spike filter is included in the BOS0614. By default, the spike filter is active at power up.

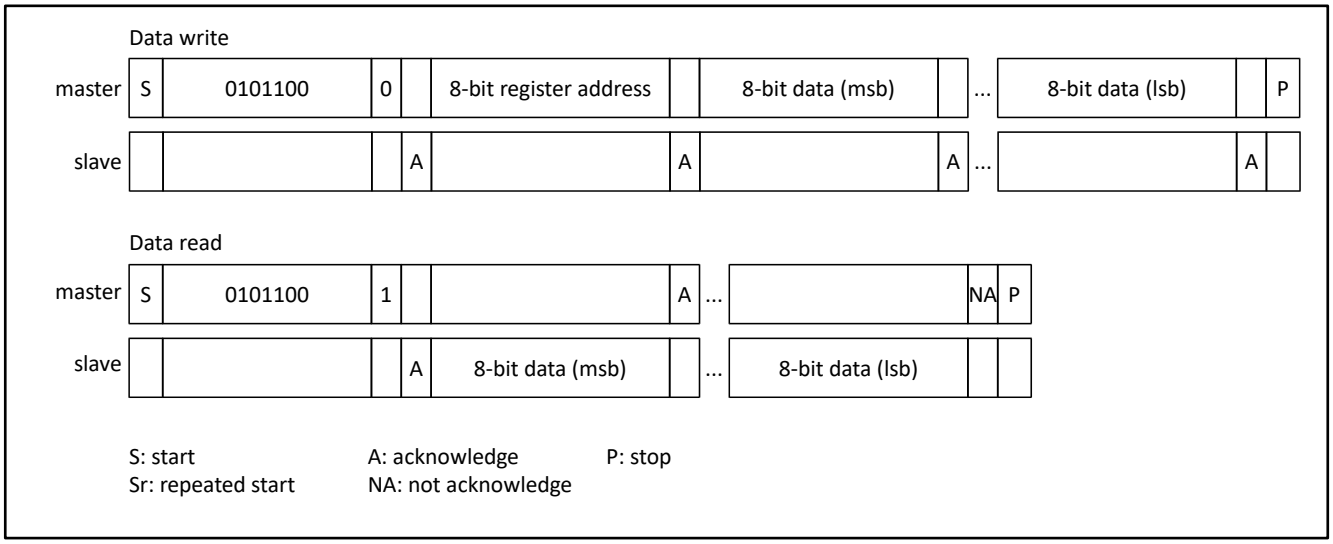


Figure 19: All possible data-transfer sequences with I²C static addressing

6.4 Direct Mode

In Direct mode (bits RAM [1:0] set to 0x0), the haptic waveform samples are played as they are sent from the host MCU to the REFERENCE register. The rate at which the data is read to generate the haptic waveform is set by bits PLAY [2:0]. Data management and synchronization can be facilitated by setting bits GPIO3-0 [3:0] to 0x6 to allow the corresponding GPIO to generate an interruption that notifies the MCU when the BOS0614 is ready to receive the next sample. Interpolation between user samples is done to generate the output waveform.

When bits RAM [1:0] is set to 0x0 to use Direct mode, the RAM is not used and its content previously written using RAM Playback mode (section 6.6) or RAM Synthesis mode (section 6.7) is preserved.

Bit PC must be set to 0x0 when using Direct mode.

6.4.1 Typical Operation Sequence

The following sequence use Direct mode to play haptic waveforms:

1. Set bits CONFIG.RAM [1:0] to 0x0 to select Direct mode.
2. Set bit TC.PC to 0x0
3. Set bits GPIOx [3:0] to 0x6
4. Set bit CONFIG.OE to 0x1
5. Write a waveform sample to the REFERENCE register.
6. On a GPIOx pin falling edge, go to step 5. to send the next waveform sample to the device.

6.5 FIFO Mode

In FIFO mode (bits RAM [1:0] set to 0x1), the waveform playback is set in a 1024-sample FIFO. The FIFO entries are appended every time waveform data is written in the REFERENCE register. Digital samples are represented as 12-bit unsigned values. If bit OE is set to 0x1, the FIFO entries are read automatically out of the FIFO at a rate set by bits PLAY [2:0]. For waveform playback streaming, the FIFO data write rate must match the readout rate of the waveform playback (set by bits PLAY [2:0]) to always keep valid data inside the FIFO. If the FIFO becomes empty, bit EMPTY is set and the FIFO maintains the last valid data, keeping the waveform in a steady state.

Burst data transfers can be used to minimize the communication interface usage. Packets of 16-bit words can be sent in the same I^2C payload to be written in the FIFO. Bit FULL is set when the FIFO becomes full and cannot accept more data. Bits FIFO_SPACE [9:0] can be read prior to verify space available before sending new data.

Waveforms should begin and end with 0 V amplitude. In case bit OE is set to 0x0 or bit RST is set to 0x1 during waveform playback, the output will be ramped down automatically to 0 V.

The FIFO mode uses the RAM space to implement the FIFO. Using the FIFO mode overwrites any waveform previously programmed using RAM Playback and RAM Synthesis modes. They must be reprogrammed before they can be used again.

Bit PC must be set to 0x0 when using FIFO mode.

6.5.1 Typical Operation Sequence

The following sequence use FIFO mode to play haptic waveforms:

1. Set bits CONFIG.RAM [1:0] to 0x1 to select FIFO mode.
2. Set bit TC.PC to 0x0
3. Set bit CONFIG.OE to 0x1 to enable the output.
4. Read bits FIFO_STATE.FIFO_SPACE to determine space available in FIFO for new data.
5. Write as much 12-bit waveform data as possible according to space available in FIFO into the REFERENCE register.
6. Repeat steps 3 and 4 until the desired waveform is completed.

In the above example, the output is enabled, and the FIFO is filled afterwards. It is also possible to preload the waveform in the FIFO before enabling the output, and then add samples to the FIFO as needed.

6.6 RAM Playback Mode

In RAM Playback mode (bits RAM [1:0] set to 0x2), a point-by-point waveform is defined by storing all the amplitude samples in chronological order in the RAM using BURST_RAM_WRITE command. The waveform is played when the output is enabled (bit OE is set to 0x1).

6.6.1 RAM Programming

The samples are written to the RAM using BURST RAM WRITE command. More than one waveform can be stored in the RAM. The 2 kB RAM can store up to 1024 words of 16-bit. Each word is defined by 16-bit data in the same format as the REFERENCE register in Direct and FIFO modes: the enabled channels are defined with bits [15:12] and the waveform amplitude by bits [11:0]. Start and end addresses are defined using the RAM_PLAYBACK command and indicate the samples to be fetched when the playback is initiated.

When playback starts, the data is read out sequentially at the sample rate set by bits PLAY [2:0].

Once the waveform has been played, it must be rearmed to be played again by writing the RAM start and end addresses again using the RAM_PLAYBACK command. The waveform will immediately start if these addresses are set while bit OE is 0x1.

No waveform should be playing while programming RAM to avoid unexpected behaviour.

6.6.2 Typical Operation Sequence

The following sequence shows how to use RAM Playback mode to play haptic waveforms:

1. Set bits CONFIG.RAM [1:0] to 0x2 to select RAM playback mode.
2. Write waveform data to the RAM using BURST RAM WRITE command. See section 6.6.3 for a detailed example.
3. Write the start and end addresses using RAM PLAYBACK command.
4. There are multiple ways to start playback:
    a. *Immediate start:* If CONFIG.OE is set to 0x1, the waveform will start to play immediately after the start and end addresses are programmed using RAM PLAYBACK command. No other action or event is required. Care must be taken to ensure any previous waveform finished playing before the memory is reprogrammed.
    b. *Intentional start:* If CONFIG.OE is set to 0x0, setting CONFIG.OE to 0x1 will start playback.
    c. *Sensing detection:* With bit AUTOP and AUTOR of any of the sensing channel (registers 0x07, 0x0B, 0x0F and 0x13), playback will start automatically when the detection conditions are met.
    d. *Triggered start:* Playback is started upon a GPIO trigger. This feature can be enabled on every GPIO by setting SENSECONFIG.EXT_TRIG bit to 0x1 and setting the desired channel GPIO to 0x7 in the GPIO register.

6.6.3 RAM Playback Example

In RAM Playback, waveform samples need to be first stored in the RAM to be fetched later. A typical RAM programming sequence is presented in Figure 20 which consist of programming a waveform using 10 samples to be played on channels 0 and 1. The bit OE is set to 0x1 to start playing immediately after the start and end addresses are programmed.

I²C Communication Sequence

Transaction 1	
Code	Description / Configure RAM Playback Mode
0x2C	I²C address
0x05	Select CONFIG register
0x2497	Set RAM Playback mode

Transaction 2	
Code	Description / Configure Burst RAM Write
0x2C	I²C address
0x00	Select REFERENCE register to use WFS commands
0x0014	WFS command : BURST RAM WRITE
0x0000	Set RAM START ADDRESS
0x000A	Set DATA COUNT (10 samples to be written starting at RAM address 0x0000)
0x3000	Sample data, enable channels 0 and 1
0x3800	Sample data, enable channels 0 and 1
0x380C	Sample data, enable channels 0 and 1
0x3819	Sample data, enable channels 0 and 1
0x3825	Sample data, enable channels 0 and 1
0x3832	Sample data, enable channels 0 and 1
0x383E	Sample data, enable channels 0 and 1
0x384B	Sample data, enable channels 0 and 1
0x3857	Sample data, enable channels 0 and 1
0x3864	Sample data, enable channels 0 and 1

Transaction 3	
Code	Description / Set RAM Playback Start and End Addresses
0x2C	I²C address
0x00	Select REFERENCE register to use WFS commands
0x0013	WFS command : RAM PLAYBACK
0x0000	Set RAM START ADDRESS
0x0009	Set RAM END ADDRESS

RAM Content

RAM Address	*Channels*	*Samples*
0x0000	0x3	0x000
0x0001	0x3	0x800
0x0002	0x3	0x80C
0x0003	0x3	0x819
0x0004	0x3	0x825
0x0005	0x3	0x832
0x0006	0x3	0x83E
0x0007	0x3	0x84B
0x0008	0x3	0x857
0x0009	0x3	0x864

WFS Register Content

WFS Register Address		
0x0013	0x00	0x000
	0x00	0x009

Figure 20: RAM Playback Setup Example

6.7 RAM Synthesis Mode

In RAM Synthesis mode (bits RAM [1:0] set to 0x3), sine wave parameters used to generate simple to complex waveforms are stored in RAM using:

1) SLICEs, written in the RAM using the RAM ACCESS command. Each SLICE contains a group of parameters used to produce a sine wave of defined amplitude, frequency, and number of cycles. It may also be ramped up and down (as shown in Figure 24). See section 6.7.1.1 for more details.
2) WAVEs, written in the RAM using the RAM ACCESS command. A WAVE defines a series of SLICEs to be played successively. All SLICEs of a WAVE must be written in order and contiguously in the RAM. See section 6.7.1.2 for more details.
3) SEQUENCER, configured using the SEQUENCER command. The SEQUENCER is used to store up to 15 WAVE addresses in RAM (called WAVEFORM_IDs). The WAVES may all be played sequentially, or in any contiguous subsets, down to a single WAVEFORM_ID. See section 6.7.1.3 for more details.

The RAM SYNTHESIS command defines the start and end WAVEFORM_IDs from the WAVEFORM_IDs list stored in the SEQUENCER command.

Once the waveform has been played, it can be played again by setting the start and end WAVEFORM_IDs again in the RAM SYNTHESIS command. The waveform will immediately start playing if the WAVEFORM_IDs in the RAM SYNTHESIS command are set while OE is set to 0x1.

No waveform should be playing while programming RAM to avoid unexpected behaviour.

6.7.1 RAM Programming

The WAVE and SLICE data are stored in RAM, as shown in Figure 21. WAVE and SLICE blocks can be arranged in any order in RAM but must not overlap.

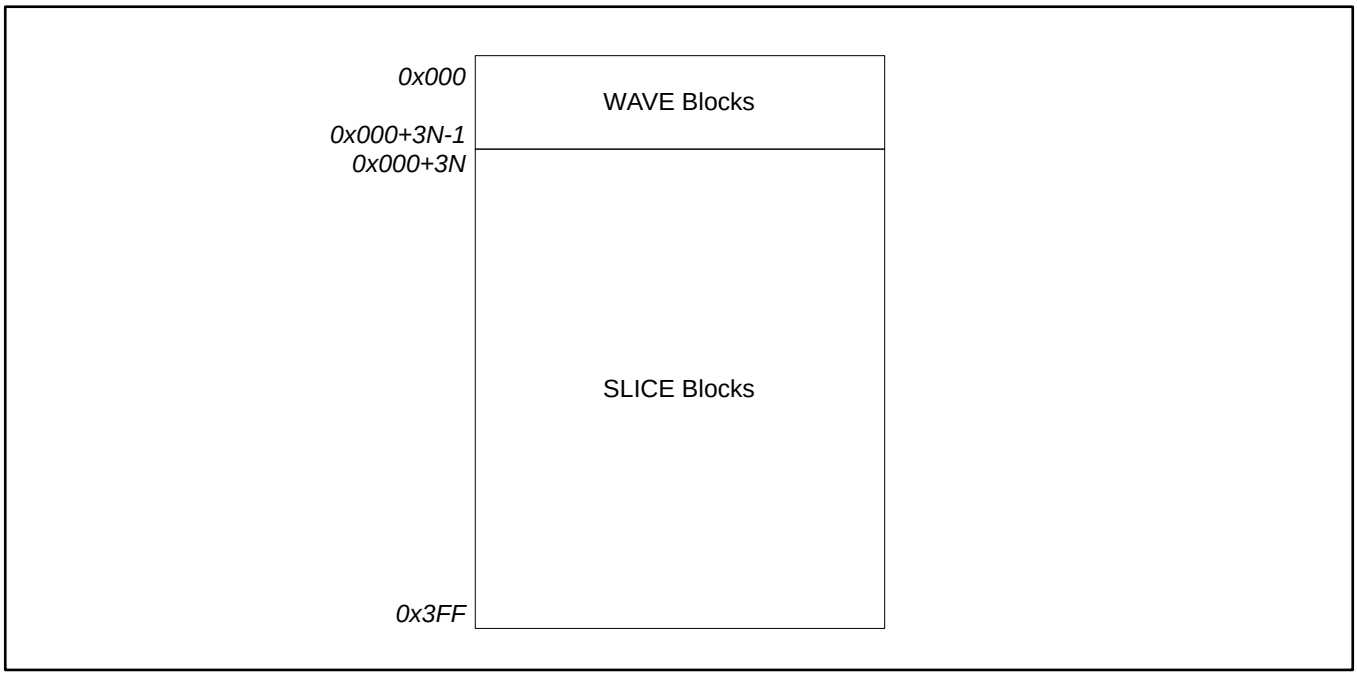


Figure 21: Example of N WAVE blocks followed with SLICEs organized in RAM.

6.7.1.1 SLICE Blocks

SLICE blocks in the RAM contains the parameters used to synthesize sine waveforms. Each SLICE block contains three words grouping nine parameters as described in Figure 22 and Table 12. Figure 23 shows an example on how several SLICEs can be organized in RAM. Figure 24 illustrates an example of how these parameters shape a SLICE waveform. Many SLICES may be successively played to form more complex waveforms.

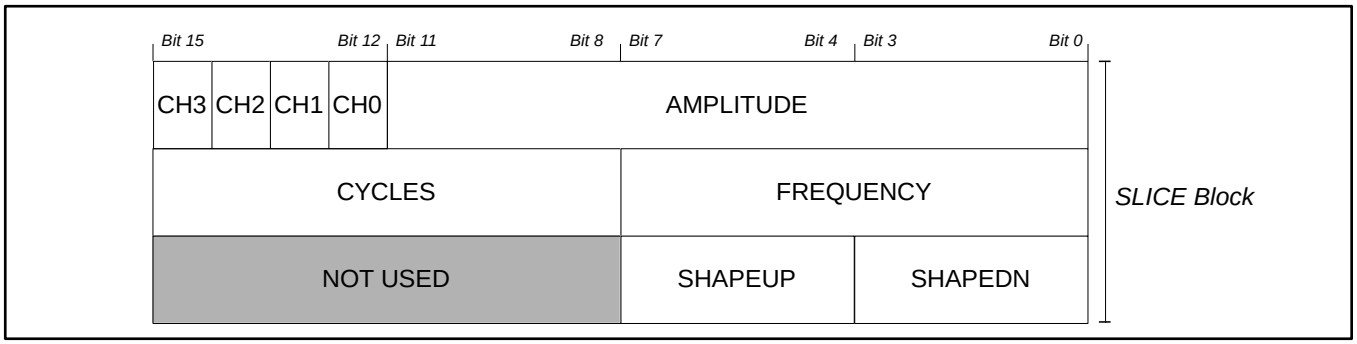


Figure 22: Sine Wave SLICE Block

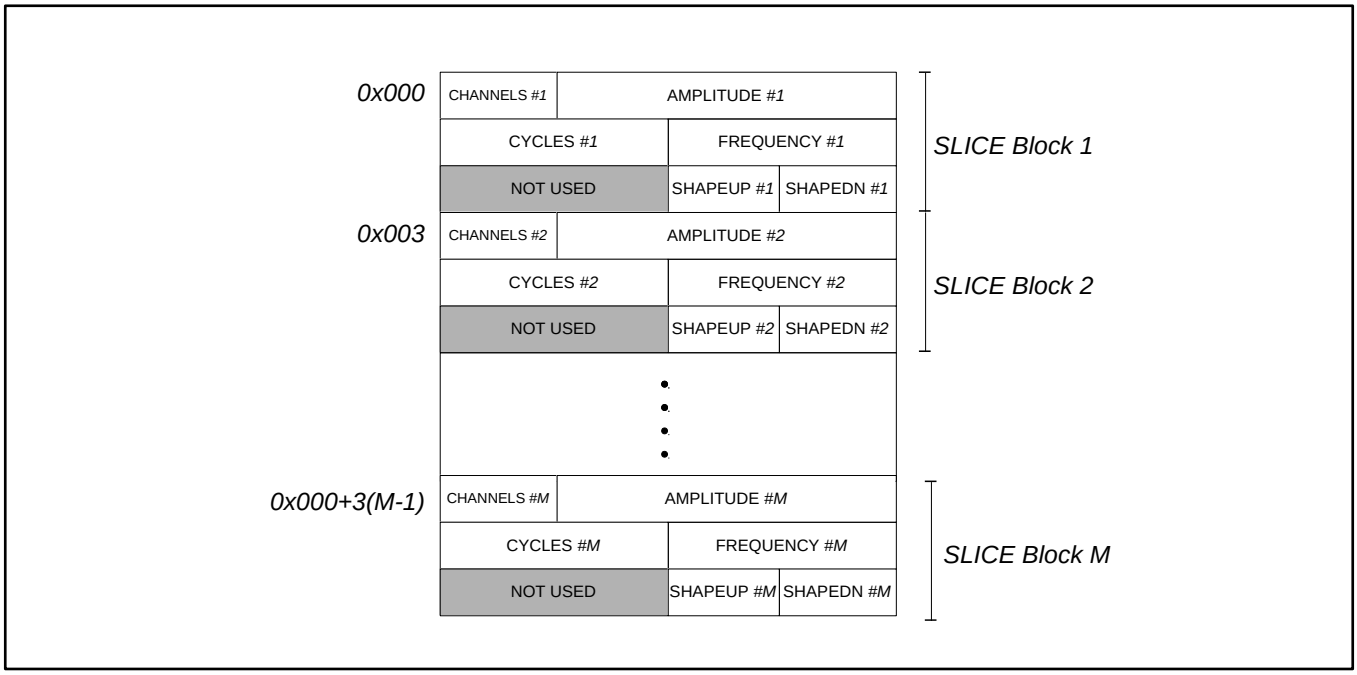


Figure 23: Example of M SLICE Blocks organized in RAM

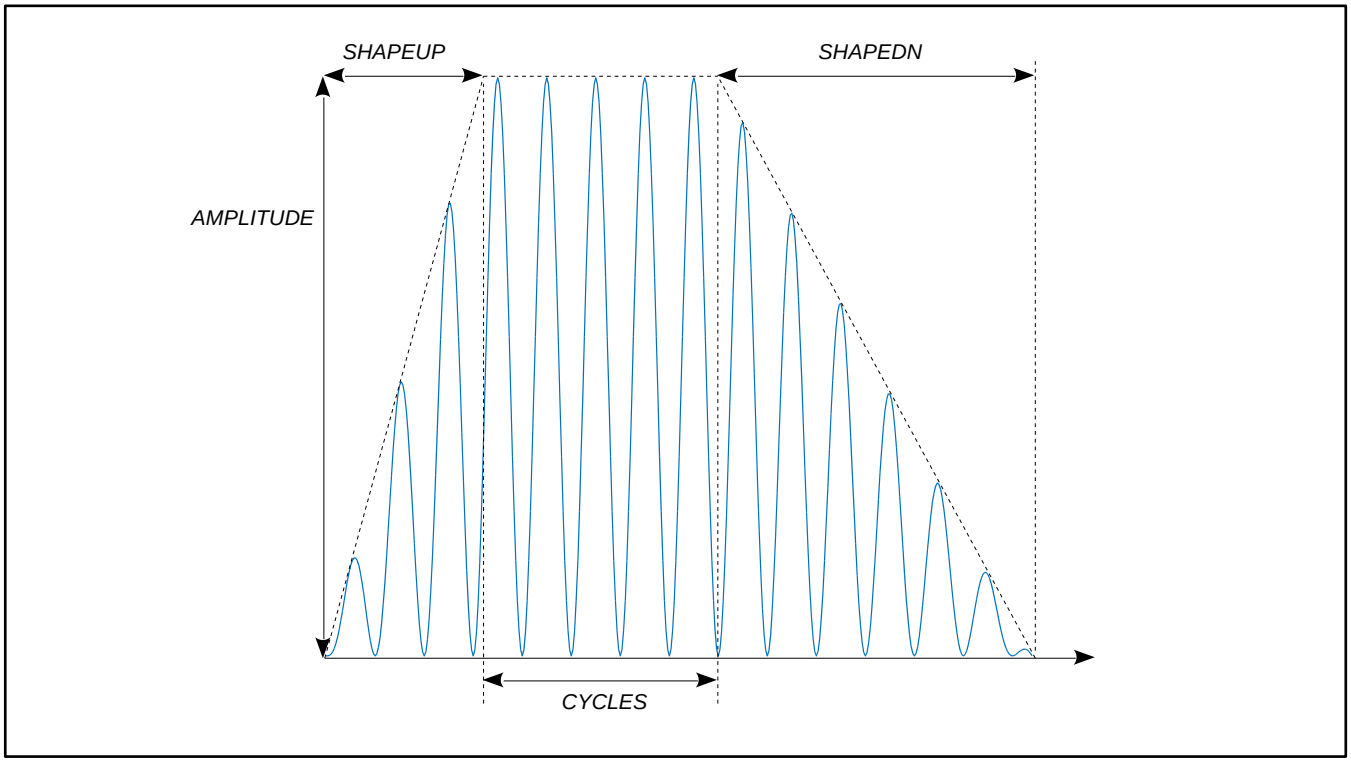


Figure 24: Sine wave SLICE parameters illustration

Table 12: Sine wave SLICE Parameters

WORD	NAME	DESCRIPTION
1[15] 1[14] 1[13] 1[12]	CH3 CH2 CH1 CH0	Indicates which channel outputs the waveform is played on. 1: Data will be played on the channel 0: Channel is inactive
1[11:0]	AMPLITUDE	Voltage = Full-scale output voltage × AMPLITUDE /4095 Full-scale output voltage = 60 V This AMPLITUDE value calculation is valid only for RAM Synthesis mode (bits RAM [1:0] set to 0x3).
2[15:8]	CYCLES	CYCLES refers to the number of times a full sine wave period will be repeated, excluding SHAPEUP/SHAPEDN ramp times. CYCLES value must be greater than 0.
2[7:0]	FREQUENCY	The waveform synthesizer has a frequency resolution of 3.9 Hz. FREQUENCY value must be greater than 0. The synthesized sine wave frequency will be: $\text{Synthesized sine wave frequency (Hz)} = 3.9 \times FREQUENCY$
3[7:4] 3[3:0]	SHAPEUP SHAPEDN	SHAPEUP sets the ramp-up time of the waveform from 0 V to AMPLITUDE. SHAPEDN sets the ramp-down time of the waveform from AMPLITUDE to 0 V. SHAPEUP and SHAPEDN values (in ms) must be greater than the length of a cycle (in ms). The ramp-up or ramp-down duration is added to the total SLICE waveform duration, which is calculated as follow: $\text{SLICE waveform duration (ms)} = SHAPEUP + \frac{CYCLES}{3.9 \times FREQUENCY} + SHAPEDN$ 0x0: No shape 0x1: 32 ms 0x2: 64 ms 0x3: 96 ms 0x4: 128 ms 0x5: 160 ms 0x6: 192 ms 0x7: 224 ms 0x8: 256 ms 0x9: 512 ms 0xA: 768 ms 0xB: 1024 ms 0xC: 1280 ms 0xD: 1536 ms 0xE: 1792 ms 0xF: 2048 ms

6.7.1.2 WAVE Blocks

As shown in Figure 25 and Figure 26, each WAVE block in RAM contains three words:

1. The SLICE START ADDRESS, which is the RAM address of the first SLICE block first word.
2. The SLICE END ADDRESS, which is the RAM address of the last SLICE block third word.
3. The WAVE CYCLE COUNT is the number of times the WAVE block is repeated.

SLICEs to be played sequentially must be placed in order and contiguously in the RAM.

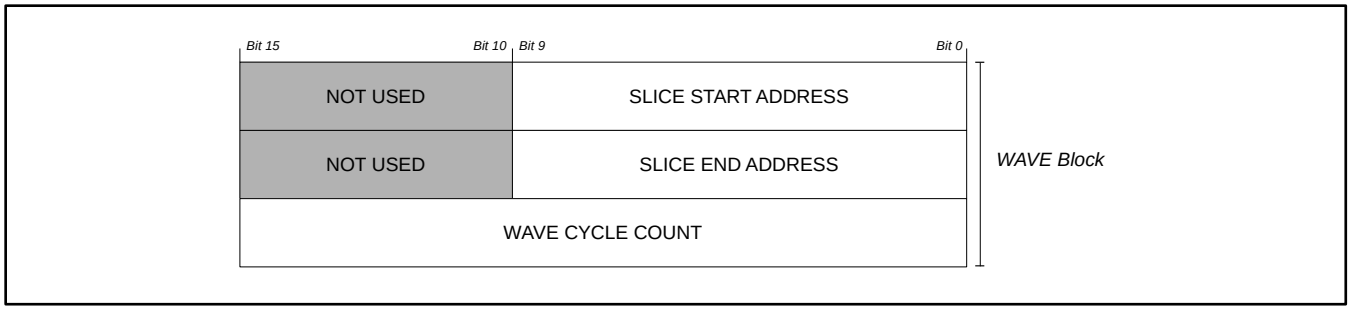


Figure 25: WAVE Block

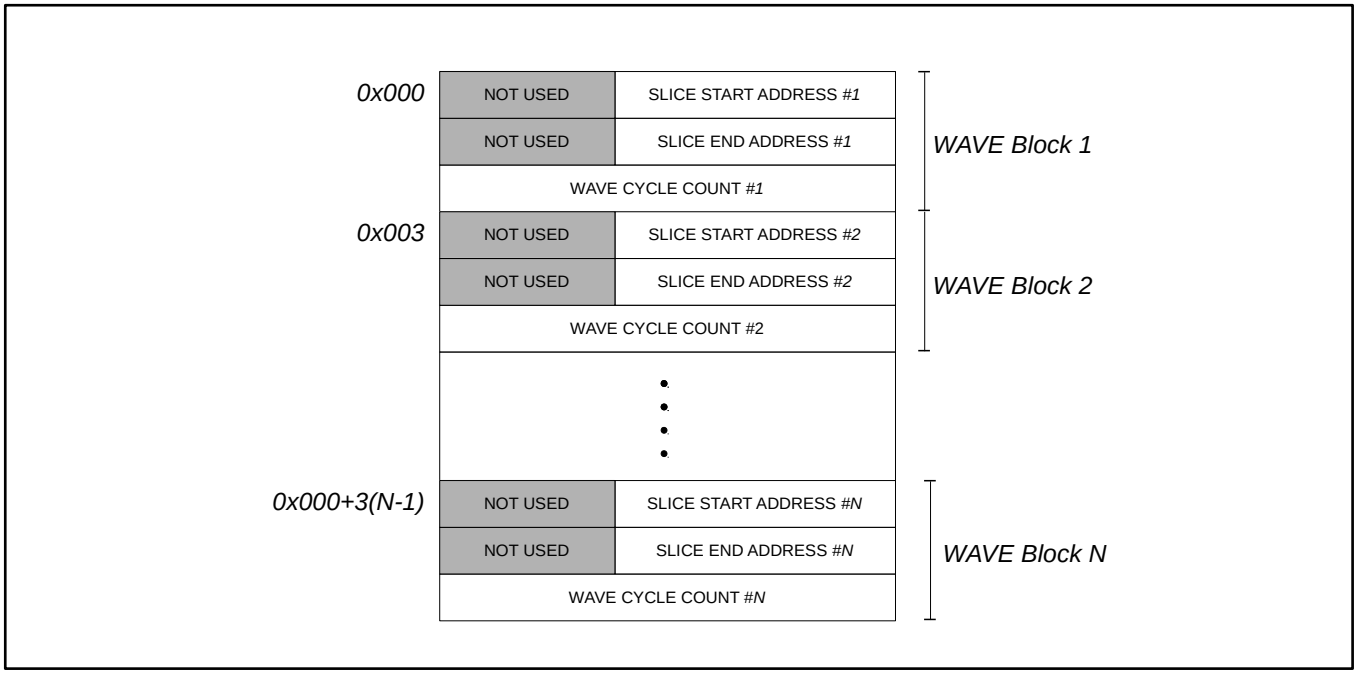


Figure 26: Example of N WAVE Blocks in RAM organized in RAM

6.7.1.3 SEQUENCER

The SEQUENCER stores up to 15 WAVEFORM_IDs to be played sequentially, named WAVEFORM_ID 0 to 14 using the SEQUENCER command. Each WAVEFORM_ID contains the address in memory of a WAVE block to play.

To program the WAVEFORM_IDs, first write the SEQUENCER address 0x0002. Then write all 15 WAVEFORM_IDs sequentially. Unused WAVEFORM_IDs may be written with any address. All 15 WAVEFORM_ID values must be written.

Various sets of waveform sequences can be played. The start and end WAVEFORM_IDs to play among the 15 WAVEFORM_IDs are defined in the RAM SYNTHESIS command. The largest sequence to be played will cover the 15 WAVEs, from WAVEFORM_ID 0 to 14. The smallest sequence is when the start address is equal to the end address and thus only one WAVEFORM_ID is played. Figure 27 shows an example where the waveform starts at SEQUENCER WAVEFORM_ID 3 and ends after playing SEQUENCER WAVEFORM_ID 6.

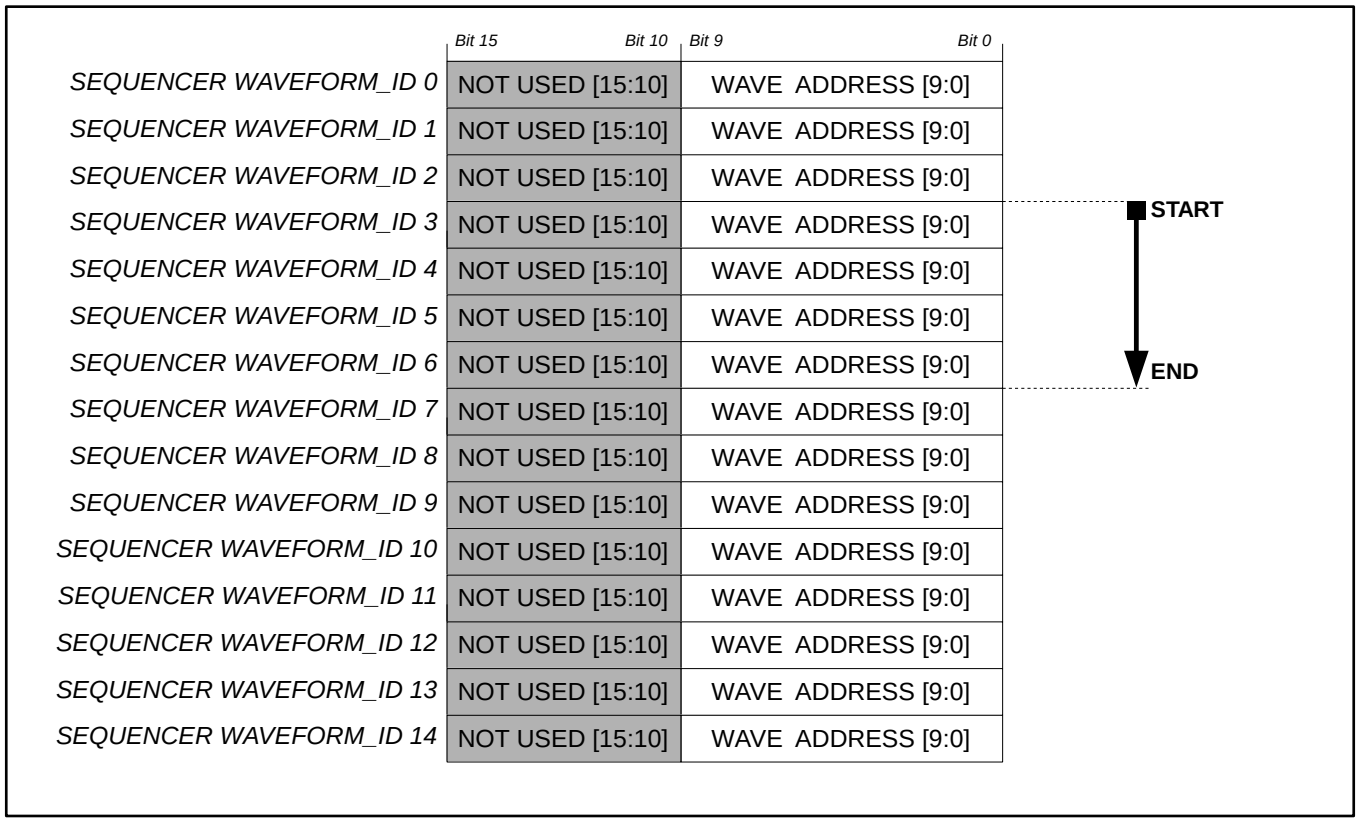


Figure 27: Sequencer example where waveform start at WAVEFORM_ID 3 and ends at 6.

6.7.2 Typical Operation Sequence

The following sequence use RAM Synthesis mode to play haptic waveforms:

1. Set bits CONFIG.RAM [1:0] to 0x3 to select RAM Synthesis mode.
2. Write 0x00 to use WFS commands.
3. Use RAM ACCESS command to write the WAVE blocks and SLICE blocks in RAM. Multiple write sequences might be needed to program the waveform addresses and slices, see section 6.7.3 for some examples.
4. Write the WAVEFORM_IDs using the SEQUENCER command, which correspond to the desired WAVE block RAM addresses.
5. Write start and end WAVEFORM_IDs that will be played using RAM SYNTHESIS command.
6. There are multiple ways to start playback:
    e. *Immediate start:* If CONFIG.OE is set to 0x1, the waveform will start to play immediately after the start and end addresses are programmed using the RAM SYNTHESIS command. No other action or event is required.
    f. *Intentional start:* If CONFIG.OE = 0, setting CONFIG.OE to 1 will start playback.
    g. *Sensing detection:* With bit AUTOP and AUTOR of any of the sensing channel (registers 0x07, 0x0B, 0x0F and 0x13), playback will start automatically when the detection conditions are met.
    h. *Triggered start:* Playback is started upon a GPIO trigger. This feature can be enabled on every GPIO by setting SENSECONFIG.EXT_TRIG bit to 0x1 and setting the desired channel GPIO to 0x7 in the GPIO register.

6.7.3 RAM Synthesis Mode Examples

Figure 28 to Figure 32 gives two examples showing how to program in RAM a waveform to play on channel 0:

- Example 1 uses only 1 SLICE and 1 WAVE programmed with a single communication transaction.
- Example 2 uses 4 SLICEs and 3 WAVEs programmed with a communication transaction for each WFS command.

Both examples use OE set to 0x1 to start playing immediately after the start and end WAVEFORM_IDs are programmed using RAM SYNTHESIS command.

I²C Communication Sequence

Transaction 1 :	
Code	Description / Configure RAM Synthesis Mode
0x2C	I²C address
0x05	Select CONFIG register
0x2697	Set RAM Synthesis Mode

Code	Description / Program one WAVE in RAM
0x0001	WFS command : RAM ACCESS
0x0000	Set RAM start address for WAVE block programming
0x0100	WAVE Data : Set RAM start address of first SLICE
0x0102	WAVE Data : Set RAM end address of last SLICE
0x0001	WAVE Data : Set WAVE cycle count (played once)

Code	Description / Program one SLICE in RAM
0x0001	WFS command : RAM ACCESS
0x0100	Set RAM start address for SLICE block programming
0x1FFF	SLICE Data : Set AMPLITUDE (full-scale), channel 0
0x0480	SLICE Data : Set CYCLES (4) and FREQUENCY (500 Hz)
0x0000	SLICE Data : Set SHAPEUP and SHAPEDN (0 ms)

Code	Description / Program Sequencer Entries
0x0002	WFS command : SEQUENCER
0x0000	SEQUENCER_W0 : WAVE block address
0x0000	SEQUENCER_W1 : Any value
0x0000	SEQUENCER_W2 : Any value
0x0000	SEQUENCER_W3 : Any value
0x0000	SEQUENCER_W4 : Any value
0x0000	SEQUENCER_W5 : Any value
0x0000	SEQUENCER_W6 : Any value
0x0000	SEQUENCER_W7 : Any value
0x0000	SEQUENCER_W8 : Any value
0x0000	SEQUENCER_W9 : Any value
0x0000	SEQUENCER_W10 : Any value
0x0000	SEQUENCER_W11 : Any value
0x0000	SEQUENCER_W12 : Any value
0x0000	SEQUENCER_W13 : Any value
0x0000	SEQUENCER_W14 : Any value

Code	Description / Set Start and End Sequencer Entries
0x0012	WFS command : RAM SYNTHESIS
0x0000	Set START and END WAVEFORM_ID to 0x0

RAM Content

RAM Address	WAVE	
0x0000	0x00	0x100
0x0001	0x00	0x102
0x0002	0x0001	

RAM Content

RAM Address	SLICE		
0x0100	0x1	0xFFF	
0x0101	0x04	0x80	
0x0102	0x00	0x0	0x0

Sequencer Content

SEQUENCER_W0	0x00	0x000
SEQUENCER_W1	0x00	0x000
SEQUENCER_W2	0x00	0x000
SEQUENCER_W3	0x00	0x000
SEQUENCER_W4	0x00	0x000
SEQUENCER_W5	0x00	0x000
SEQUENCER_W6	0x00	0x000
SEQUENCER_W7	0x00	0x000
SEQUENCER_W8	0x00	0x000
SEQUENCER_W9	0x00	0x000
SEQUENCER_W10	0x00	0x000
SEQUENCER_W11	0x00	0x000
SEQUENCER_W12	0x00	0x000
SEQUENCER_W13	0x00	0x000
SEQUENCER_W14	0x00	0x000

WFS Register Content

WFS Register Address			
0x0012	0x0	0x0	0x00

Figure 28: RAM synthesis mode setup example 1

I²C Communication Sequence

Transaction 1	
Code	Description / Configure RAM Synthesis Mode
0x2C	I²C address
0x05	Select CONFIG register
0x2697	Set RAM Synthesis Mode

Transaction 2	
Code	Description / Program WAVE #1 in RAM
0x2C	I²C address
0x00	Select REFERENCE register to use WFS command
0x0001	WFS command : RAM ACCESS
0x0000	Set RAM start address for WAVE block programming
0x0100	WAVE #1 Data : Set RAM start address of SLICE #1
0x0102	WAVE #1 Data : Set RAM end address of SLICE #1
0x000E	WAVE #1 Data : Set WAVE cycle count (14 times)

RAM Content

RAM Address	*WAVE #1*	
0x0000	0x00	0x100
0x0001	0x00	0x102
0x0002	0x000E	

Transaction 3	
Code	Description / Program SLICE #1 in RAM
0x2C	I²C address
0x00	Select REFERENCE register to use WFS command
0x0001	WFS command : RAM ACCESS
0x0100	Set RAM start address for SLICE block programming
0x1FFF	SLICE #1 Data : Set AMPLITUDE (full scale), enable channel 0
0x01FF	SLICE #1 Data : Set CYCLES (1) and FREQUENCY (995 Hz)
0x0000	SLICE #1 Data : Set SHAPEUP and SHAPEDN (0 ms)

RAM Content

RAM Address	*SLICE #1*		
0x0100	0x1	0xFFF	
0x0101	0x01	0xFF	
0x0102	0x00	0x0	0x0

Transaction 4	
Code	Description / Program WAVE #2 in RAM
0x2C	I²C address
0x00	Select REFERENCE register to use WFS command
0x0001	WFS command : RAM ACCESS
0x0003	Set RAM start address for WAVE block programming
0x0200	WAVE #2 Data : Set RAM start address of SLICE #2
0x0202	WAVE #2 Data : Set RAM end address of SLICE #2
0x001D	WAVE #2 Data : Set WAVE cycle count (29 times)

RAM Content

RAM Address	*WAVE #2*	
0x0003	0x00	0x200
0x0004	0x00	0x202
0x0005	0x001D	

Figure 29: RAM synthesis mode setup example 2

I²C Communication Sequence

Transaction 5	
Code	Description / Program SLICE #2 in RAM
0x2C	I²C address
0x00	Select REFERENCE register to use WFS command
0x0001	WFS command : RAM ACCESS
0x0200	Set RAM start address for SLICE block programming
0x1CCC	SLICE #2 Data : Set AMPLITUDE (106.6V), enable channel 0
0x1033	SLICE #2 Data : Set CYCLES (16) and FREQUENCY (200 Hz)
0x0021	SLICE #2 Data : Set SHAPEUP (64 ms) and SHAPEDN (32 ms)

RAM Content

RAM Address	SLICE #2		
0x0200	0x1	0xCCC	
0x0201	0x10	0x33	
0x0202	0x00	0x2	0x1

Transaction 6	
Code	Description / Program WAVE #3 in RAM
0x2C	I²C address
0x00	Select REFERENCE register to use WFS command
0x0001	WFS command : RAM ACCESS
0x0006	Set RAM start address for WAVE block programming
0x0203	WAVE #3 Data : Set RAM start address of SLICE #3
0x0208	WAVE #3 Data : Set RAM end address of SLICE #4
0x01EE	WAVE #3 Data : Set WAVE cycle count (494 times)

RAM Content

RAM Address	WAVE #3	
0x0006	0x00	0x203
0x0007	0x00	0x208
0x0008	0x01EE	

Transaction 7	
Code	Description / Program SLICE #3 in RAM
0x2C	I²C address
0x00	Select REFERENCE register to use WFS command
0x0001	WFS command : RAM ACCESS
0x0203	Set RAM start address for SLICE block programming
0x1AAA	SLICE #3 Data : Set AMPLITUDE (88.8V), channel 0
0x0A1A	SLICE 3 Data : Set CYCLES (10), FREQUENCY (100 Hz)
0x0012	SLICE #3 Data : Set SHAPEUP (32 ms) and SHAPEDN (64 ms)

RAM Content

RAM Address	SLICE #3		
0x0203	0x1	0xAAA	
0x0204	0x0A	0x1A	
0x0205	0x00	0x1	0x2

Transaction 8	
Code	Description / Program SLICE #4 in RAM
0x2C	I²C address
0x00	Select REFERENCE register to use WFS command
0x0001	WFS command : RAM ACCESS
0x0206	Set RAM start address for SLICE block programming
0x1000	SLICE #4 Data : Set AMPLITUDE (0 V), enable channel 0
0x1F1A	SLICE #4 Data : Set CYCLES (31) and FREQUENCY (100 Hz)
0x0000	SLICE #4 Data : Set SHAPEUP (0 ms) and SHAPEDN (0 ms)

RAM Content

RAM Address	SLICE #4		
0x0206	0x1	0x000	
0x0207	0x1F	0x1A	
0x0208	0x00	0x0	0x0

Figure 30: RAM synthesis mode setup example 2 (continued)

I²C Communication Sequence

Transaction 9	
Code	Description / Program Sequencer Entries
0x2C	I²C address
0x00	Select REFERENCE register to use WFS command
0x0002	WFS command : SEQUENCER
0x0000	SEQUENCER_W0 value : WAVE #1 block address
0x0003	SEQUENCER_W1 value : WAVE #2 block address
0x0006	SEQUENCER_W2 value : WAVE #3 block address
0x0000	SEQUENCER_W3 value
0x0000	SEQUENCER_W4 value
0x0000	SEQUENCER_W5 value
0x0000	SEQUENCER_W6 value
0x0000	SEQUENCER_W7 value
0x0000	SEQUENCER_W8 value
0x0000	SEQUENCER_W9 value
0x0000	SEQUENCER_W10 value
0x0000	SEQUENCER_W11 value
0x0000	SEQUENCER_W12 value
0x0000	SEQUENCER_W13 value
0x0000	SEQUENCER_W14 value

Sequencer Content

SEQUENCER_W0	0x00	0x000
SEQUENCER_W1	0x00	0x003
SEQUENCER_W2	0x00	0x006
SEQUENCER_W3	0x00	0x000
SEQUENCER_W4	0x00	0x000
SEQUENCER_W5	0x00	0x000
SEQUENCER_W6	0x00	0x000
SEQUENCER_W7	0x00	0x000
SEQUENCER_W8	0x00	0x000
SEQUENCER_W9	0x00	0x000
SEQUENCER_W10	0x00	0x000
SEQUENCER_W11	0x00	0x000
SEQUENCER_W12	0x00	0x000
SEQUENCER_W13	0x00	0x000
SEQUENCER_W14	0x00	0x000

Transaction 10	
Code	Description / Set Start and End Sequencer Entries
0x2C	I²C address
0x00	Select REFERENCE register to use WFS command
0x0012	WFS command : RAM SYNTHESIS
0x2000	Set START WAVEFORM_ID to 0x0 and END WAVEFORM_ID to 0x2

WFS Register Content

WFS Register Address			
0x0012	0x2	0x0	0x00

Figure 31: RAM synthesis mode setup example 2 (continued)

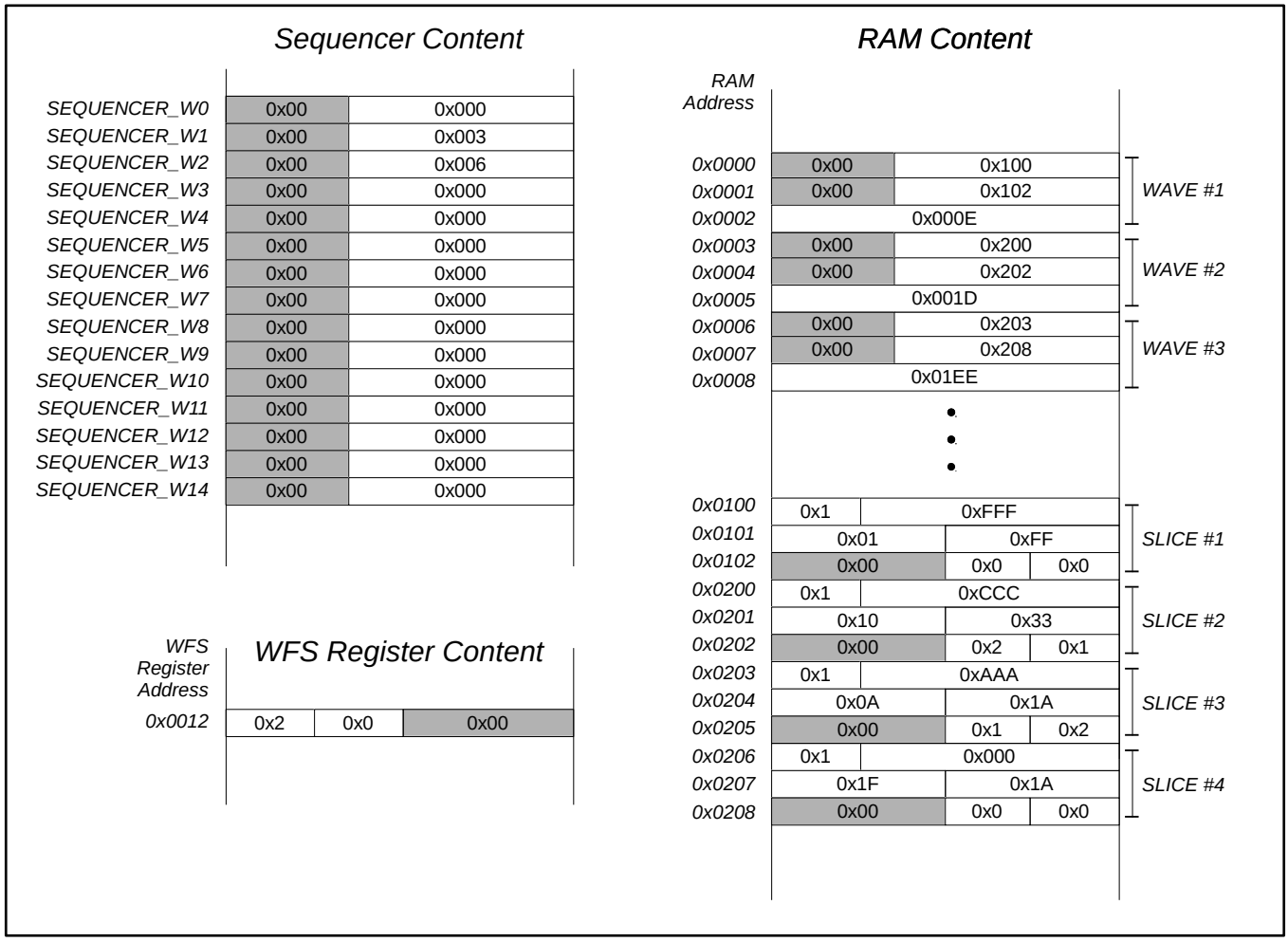


Figure 32: RAM Synthesis mode setup example 2 RAM summary

6.8 Piezo Actuator Sensing

The digital front-end gives access to internal registers (addresses 0x06 to 0x1F) to configure the pins OUT0 (F1), OUT1 (E2), OUT2 (E4) and OUT3 (F5) to sense the signals of up to four piezo actuators which can trigger detection events and haptic waveform playback.

This section details the sensing configuration and three (3) typical detection event usages: (1) automatic haptic playback, (2) GPIOs interruptions and (3) polling of sensing status registers. For detailed instructions on using BOS0614 sensing features, please refer to the application notes on Boréas website.

6.8.1 Sensing Configuration

The sensing of each OUTx channel is enabled using SENSECONFIG [3:0] bits. Four mechanisms can trigger a detection event on each OUTx independently:

- T1 and T2: Absolute voltage amplitude on OUTx. The amplitude threshold values are set in the SENSExP and SENSExR registers respectively (see Table 15) and are used to trigger detection flags T1x and T2x available in SENSESTATUS register.
- S1 and S2: Variation of voltage with time, i.e., slope. The two (2) slope thresholds are set with bits SLOPE1 [6:0] (S1) and SLOPE2 [6:0] (S2) in SENSExS registers (see Table 15) and are used to trigger detection flags S1x and S2x available in SENSESTATUS register.

Each trigger mechanism (T1, T2, S1 and S2) can be enabled independently in the sense configuration registers for each channel (*SENSEx-Sensing Configuration* column in Table 15). Depending on which trigger mechanism (T1, T2, S1 or S2) are enabled in the SENSEx register (0x07, 0x0B, 0x0F and 0x13), a detection event will be triggered based on the conditions listed in Table 13 for actuator press events and Table 14 actuator release events. The condition where bit SENSEx.T1 is set to 0x0, bit SENSEx.S1 is set to 0x0, bit SENSEx.T2 is set to 0x0 and bit SENSEx.S2 is set to 0x1 works well to emulate mechanical button by playing haptic waveform on piezo button press and piezo button release.

The typical configuration sequence is as follows:

1. If needed, run the sensing calibration with the following sequence:
    1. Set SENSECONFIG.CH0 / CH1 / CH2 / CH3 bits to 0x0.
    2. Wait 10 ms.
    3. Set SENSECONFIG.CH0 bit to 0x1.
    4. Run sensing calibration by setting bit SENSECONFIG.CAL to 0x1.
    5. Wait the calibration to finish by polling SENSECONFIG.CAL. The calibration duration is approximately set by bits CONFIG.SHORT [1:0].
2. Configure the sensing conditions using registers 0x06 to 0x16.
3. Enable sensing on the desired channel using SENSECONFIG [3:0] bits.

Table 13: Press event triggering conditions configuration, where x is the channel number

Bit SENSEx.T1 Value	Bit SENSEx.S1 Value	Condition to trigger a press event
0x0	0x0	(S1x & T1x) | T2x = 1
0x1	0x0	T1x = 1
0x0	0x1	S1x = 1
0x1	0x1	S1x & T1x = 1

Table 14: Release event triggering conditions configuration, where x is the channel number

Bit SENSEx.T2 Value	Bit SENSEx.S2 Value	Condition to trigger a release event
0x0	0x0	(S2x & T2x) | T1x = 1
0x1	0x0	T2x = 1
0x0	0x1	S2x = 1
0x1	0x1	S2x & T2x = 1

Table 15: Sense registers for all 4 channels: haptic waveform feedback and trigger conditions

CHANNEL	REGISTER ADDRESS			
	SENSEx Registers-Sensing Configuration	SENSExP Registers-Press Absolute Voltage Parameters (T1)	SENSExR Registers-Release Absolute Voltage Parameters (T2)	SENSExS Registers-Slope Parameters (S1 and S2)
0	0x07	0x08	0x09	0x0A
1	0x0B	0x0C	0x0D	0x0E
2	0x0F	0x10	0x11	0x12
3	0x13	0x14	0x15	0x16

6.8.2 Detection Event Usage – Automatic Haptic playback

Haptic feedback can be generated automatically upon a detection event, with minimum intervention from the MCU. The waveform played is configured using the SENSEx.WVP [2:0] and SENSEx.WVR [2:0] bits of each channel (registers 0x07, 0x0B, 0x0F and 0x13) and the waveform synthesizer. A variety of

waveforms defined in the waveform synthesizer can thus be automatically played upon detection. See section 6.7 for more detail on the waveform synthesizer.

The Table 16 lists the sequencer content played on the channel output for each WVP [2:0] and WVR [2:0] value selected:

- Column WVP [2:0] / WVR [2:0]: Value of either SENSEx.WVP [2:0] or SENSEx.WVR [2:0] in the selected register (0x07, 0x0B, 0x0F or 0x13)
- Column START WAVEFORM_ID: Sequencer WAVEFORM_ID of the beginning waveform
- Column END WAVEFORM_ID: Sequencer WAVEFORM_ID of the end waveform
- Column MAX SEGMENTS: Maximum number of sequencer WAVEFORM_IDs used for the selected WVP [2:0] / WVR [2:0] value.

To use less than the maximum number of segments available for the selected WVP [2:0] / WVR [2:0] setting, set the latter WAVEFORM_ID values to 0x000. For instance, if only 1 segment is needed with WVP [2:0] = 0x7, set the SEQUENCER WAVEFORM_ID 11 with the desired WAVE block address and set SEQUENCER WAVEFORM_ID 12, 13 and 14 to 0x000 (see section 6.7.1.3).

Table 16: Bits WVP [2:0] and WVR [2:0] details

WVP [2:0] / WVR [2:0]	START WAVEFORM_ID	END WAVEFORM_ID	MAX SEGMENTS
0x0	0	0	1
0x1	1	1	1
0x2	2	2	1
0x3	3	3	1
0x4	4	5	2
0x5	6	7	2
0x6	8	10	3
0x7	11	14	4

Automatic haptic effects for press and release are respectively activated using bits AUTOP and AUTOR of the selected channel (register 0x07, 0x0B, 0x0F or 0x13). Trigger conditions are selected using bits S1, T1, S2, T2 as described is section 6.8.1.

6.8.3 Detection Event Usage – GPIO Interruptions

GPIOs pins can generate interruptions to notify the MCU a detection event occurred on their associated channel by setting GPIO3-0 [3:0] bits to 0x1.

6.8.4 Detection Event Usage – Polling

For maximum flexibility in building custom sensing algorithms, the following information can be polled by the MCU:

- IC status: register IC_STATUS (0x01)
- Embedded sensing trigger mechanism states: register SENSESTATUS (0x17)
- Processed sensing voltage of each channel: registers SENSEDATA0 (0x18) to SENSEDATA3 (0x1B)
- Raw sensing data of each channel: registers SENSERAW0 (0x1C) to SENSERAW0 (0x1F)

6.9 Main Register Map

Table 17 summarized the main register map and section 6.9.1 details the main registers.

Table 17: Main register map

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00 REFERENCE	CH3	CH2	CH1	CH0	REFERENCE [11:0]											
0x01 IC_STATUS	RSVD	SENSE ALL	PRESS_RELEASE [3:0]				STATE [1:0]		OVV	OVT	MAX_ POWER	IDAC	UVLO	SC	FULL	EMPTY
0x02 READ	RSVD								BC [7:0]							
0x03 GPIO	GPIO3 [3:0]				GPIO2 [3:0]				GPIO1 [3:0]				GPIO0[3:0]			
0x04 TC	RSVD				POL	PC	TCP [4:0]					TCR [4:0]				
0x05 CONFIG	SC	OD	SHORT [1:0]		STR	RAM [1:0]		TOUT	UPI	RST	LOCK	OE	DS	PLAY [2:0]		
0x06 SENSECONFIG	EXT_ TRIG	ZPS_ SENS	ZPS	SEQ	SCOMP [1:0]		SCOMPAUTO[1:0]		SAMP[1:0]		SAME	CAL	CH3	CH2	CH1	CH0
0x07 SENSE0	RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1
0x08 SENSE0P	REP [2:0]			AB	THRESHOLD [11:0]											
0x09 SENSE0R	REP [2:0]			AB	THRESHOLD [11:0]											
0x0A SENSE0S	ABS2	SLOPE2 [6:0]							ABS1	SLOPE1 [6:0]						
0x0B SENSE1	RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1
0x0C SENSE1P	REP [2:0]			AB	THRESHOLD [11:0]											
0x0D SENSE1R	REP [2:0]			AB	THRESHOLD [11:0]											
0x0E SENSE1S	ABS2	SLOPE2 [6:0]							ABS1	SLOPE1 [6:0]						
0x0F SENSE2	RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1
0x10 SENSE2P	REP [2:0]			AB	THRESHOLD [11:0]											
0x11 SENSE2R	REP [2:0]			AB	THRESHOLD [11:0]											
0x12 SENSE2S	ABS2	SLOPE2 [6:0]							ABS1	SLOPE1 [6:0]						
0x13 SENSE3	RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1
0x14 SENSE3P	REP [2:0]			AB	THRESHOLD [11:0]											
0x15 SENSE3R	REP [2:0]			AB	THRESHOLD [11:0]											
0x16 SENSE3S	ABS2	SLOPE2 [6:0]							ABS1	SLOPE1 [6:0]						
0x17 SENSESTATUS	S23	S13	T23	T13	S22	S12	T22	T12	S21	S11	T21	T11	S20	S10	T20	T10
0x18 SENSEDATA0	SENSEDATA [15:0]															

Address	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x19 SENSEDATA1	SENSEDATA [15:0]															
0x1A SENSEDATA2	SENSEDATA [15:0]															
0x1B SENSEDATA3	SENSEDATA [15:0]															
0x20 KPA	RSVD				SB [1:0]		FSWMAX [1:0]		KPA [7:0]							
0x21 KP_KI	RSVD	KIBASE [3:0]				KP [10:0]										
0x22 DEADTIME	AD_ SENSE	RSVD			DHS [6:0]							DLS [4:0]				
0x23 PARCAP	PARCAP [7:0]								I_ON_SCALE [7:0]							
0x24 SUP_RISE	RSVD			CP5	LP	VBUS [4:0]					TI_RISE [5:0]					
0x25 TRIM	TRIMRW [1:0]		RSVD				TRIM_OSC [6:0]							TRIM_REG [2:0]		
0x26 CHIPID	CHIPID [15:0]															
0x27	RSVD															
0x28 VFEEDBACK	RSVD		CH3	CH2	CH1	CH0	VFEEDBACK[9:0]									
0x29 FIFO_STATE	RSVD			ERROR	FULL	EMPTY	FIFO_SPACE[9:0]									
0x2A AUTO_STATE	RSVD				PRESS_RELEASE[3:0]				RQS_ PLAY	WAVE[2:0]			PLAY_CHANNELS[3:0]			
0x2B RAM_DATA	RAM_DATA [15:0]															
0x2C SENSE_OFFSET	RSVD							SENSE_OFFSET [8:0]								

Figure 33, Figure 34 and Figure 35 presents 3 different I^2C communication sequence examples using either a single communication transaction by main register access, a single communication transaction to access several main registers or the use of bit STR to access several main registers.

Transaction 1	
Code	Description / Access to register 1
0x2C	I²C address
0x00	Main register 1 address
0x0000	Expected word for register 1

Transaction 2	
Code	Description / Access to register 2
0x2C	I²C address
0x00	Main register 2 address
0x0000	Expected word for register 2

Transaction 3	
Code	Description / Access to register 3
0x2C	I²C address
0x00	Main register 3 address
0x0000	Expected word for register 3

Figure 33: Generic I²C communication sequence example to access a main register using a transaction

Transaction 1	
Code	Description / Access to register 1
0x2C	I²C address
0x00	Main register 1 address
0x0000	Expected word for register 1

Code	Description / Access to register 2
0x00	Main register 2 address
0x0000	Expected word for register 2

Code	Description / Access to register 3
0x00	Main register 3 address
0x0000	Expected word for register 3

Figure 34: Generic I²C communication sequence example to access several main registers using a single transaction

Transaction 1	
Code	Description / Access to register 0x0Z
0x2C	I²C address
0x0Z	Main register address
0x0000	Expected word for register 0x0Z

Code	Description / Access to register 0x0Z+1
0x0000	Expected word for register 0x0Z+1

Code	Description / Access to register 0x0Z+2
0x0000	Expected word for register 0x0Z+2

Figure 35: Generic I²C communication sequence example to access several main registers with bit STR set to 0x1

6.9.1 Main Register Map Details

Table 18: REFERENCE register details with RAM in modes 0 and 1.

ADDRESS: 0x00 REFERENCE (RAM [1:0] mode 0, 1)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH3	CH2	CH1	CH0	REFERENCE [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	CH3	0x0	R/W	Plays wave on channel 3. 1: Data will be played on the channel 0: Channel is inactive
14	CH2	0x0	R/W	Plays wave on channel 2. 1: Data will be played on the channel 0: Channel is inactive
13	CH1	0x0	R/W	Plays wave on channel 1. 1: Data will be played on the channel 0: Channel is inactive
12	CH0	0x0	R/W	Plays wave on channel 0. 1: Data will be played on the channel 0: Channel is inactive
11:0	REFERENCE [11:0]	0X00	R/W	Input of the RAM/FIFO. Desired amplitude of the output in 12-bit unsigned format. BOS0614 will work with a lower-resolution waveform: shift data left to align MSBs. The amplitude in volts is determined by: $$Amplitude\ (V) = \frac{\text{REFERENCE}\ [11:0]}{2^{12}-1} \times V_{ref} \times FB_{ratio}$$ Where V_{ref} = 3.6 V is the ADC input range and FB_{ratio} = 19 is the feedback ratio. *V* should always be smaller or equal to 60 V, so amplitude value should not exceed 3593 (0xE09).

**The bits CH3, CH2, CH1, CH0 can only be changed when bits REFERENCE [11:0] are set to 0x000, if not, the change will be ignored by the controller.*

Table 19: REFERENCE register details with RAM in modes 2 and 3.

ADDRESS: 0x00 REFERENCE (RAM mode 2, 3)															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA [15:0]															

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:0	DATA [15:0]	0x0	R/W	Input data for the Waveform Synthesizer (WFS), see section 6.10 for more detail. Channels can be selected with the content of bits [15:12] with bit CONFIG.SC set to 0x1.

Table 20: IC STATUS register details.

ADDRESS: 0x01 IC STATUS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	SENSEALL	PRESS_RELEASE [3:0]				STATE		OVV	OVT	MAX_POWER	IDAC	UVLO	SC	FULL	EMPTY

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
14	SENSEALL	0x1	R	General state of the sense channels. 0x1: No detection event on any channel. 0x0: At least one sense channel has a detection event triggered

ADDRESS: 0x01 IC STATUS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	SENSE ALL	PRESS_RELEASE [3:0]				STATE		OVV	OVT	MAX_ POWER	IDAC	UVLO	SC	FULL	EMPTY

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
13	PRESS_RELEASE [3]	0x0	R	State of sense channel 3 (OUT3). 0x1: Actuator is pressed 0x0: Actuator is released
12	PRESS_RELEASE [2]	0x0	R	State of sense channel 2 (OUT2). 0x1: Actuator is pressed 0x0: Actuator is released
11	PRESS_RELEASE [1]	0x0	R	State of sense channel 1 (OUT1). 0x1: Actuator is pressed 0x0: Actuator is released
10	PRESS_RELEASE [0]	0x0	R	State of sense channel 0 (OUT0). 0x1: Actuator is pressed 0x0: Actuator is released
9:8	STATE [1:0]	0x0	R	Power state of the BOS0614. STATE [1:0] = 0x3 indicates that one of the following errors occurred: OVV, OVT, IDAC, UVLO or SC. 0x0: IDLE 0x1: CALIBRATION 0x2: RUN 0x3: ERROR
7	OVV	0x0	R	Overvoltage fault bit. 0x1: Output voltage exceeded approximately 65 V. 0x0: Output voltage is OK
6	OVT	0x0	R	Over-temperature fault bit. 0x1: Over-temperature detected on the IC 0x0: IC temperature is OK
5	MAX_POWER	0x0	R	Indicates if maximum amount of power is used. 0x1: Maximum power, distortion likely 0x0: Amount of power is acceptable Conditions where MAX_POWER flag is raised should be avoided as the device reliability and life may be reduced.
4	IDAC	0x0	R	IDAC status bit. 0x1: Problem with current detection 0x0: No problem with current detection A problem with the IDAC most likely indicates that R_{sense} or L_1 is disconnected.
3	UVLO	0x0	R	Under-voltage fault bit. 0x1: V_{DD} under-voltage detected while trying to output a waveform 0x0: V_{DD} is OK
2	SC	0x0	R	Piezo Load Short circuit fault bit. 0x1: Short circuit detected on the piezo load 0x0: No short circuit detected on the load
1	FULL	0x0	R	Indicates whether the FIFO is full. 0x1: Full 0x0: Not full

ADDRESS: 0x01 IC STATUS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	SENSE ALL	PRESS_RELEASE [3:0]				STATE		OVV	OVT	MAX_ POWER	IDAC	UVLO	SC	FULL	EMPTY

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
0	EMPTY	0x1	R	In Direct mode(RAM bits set to 0x0), indicates when new data is needed: 0: New data needed 1: Wait before sending new data In FIFO mode (RAM bits set to 0x1), indicates when FIFO is empty: 0: FIFO is empty 1: FIFO is not empty In RAM Synthesis or RAM playback mode (RAM bits set to 0x2 or 0x3), indicates when the haptic waveform has finished playing: 0: Waveform done 1: Waveform is not done

Table 21: READ register details

ADDRESS: 0x02 READ															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								BC [7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
7:0	BC [7:0]	0x26	R/W	Address of internal register whose content is returned on communication bus.

Table 22: GPIO register details

ADDRESS: 0x03 GPIO															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO3 [3:0]				GPIO2 [3:0]				GPIO1 [3:0]				GPIO0 [3:0]			

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:12	GPIO3 [3:0]	0x0	R/W	Determines the GPIO3 behaviour. By setting GPIO3 [3:0] to 0x7 and setting bit EXT_TRIG to 0x1, the GPIO3 will act as an *input* to trigger haptic waveforms on channel 3 (more detail in section 6.2.10). The following GPIO3 [3:0] values determine the information output on GPIO3: 0x0: State of sense channel 3: 1: Actuator is released 0: Actuator is pressed 0x1: Detection event status on channel 3: 1: No detection event triggered on channel 3 0: Detection event triggered on channel 3 0x2: Detection event status of any channel: 1: No detection event triggered in any channel 0: Detection event triggered on at least one channel 0x3: Indicates whether the waveform is done or the FIFO empty (state of EMPTY bit): 1: Waveform is not done, FIFO is not empty 0: Waveform done, FIFO is empty 0x4: Indicates is the BOS0614 is in Error state, i.e., bits STATE [1:0] are 0x3: 1: No error detected 0: Error detected 0x5: Indicates if maximum. amount of power is used (same as bit MAX_POWER): 1: Amount of power is acceptable 0: Maximum power, distortion likely 0x6: In Direct Mode (bit RAM [1:0] set to 0x0), indicates when next data is needed by generating a pulse of minimum 0.5 µs: 1: Wait before sending new data 0: New data needed (pulse of minimum 0.5 µs) 0x7: When bit EXT_TRIG is set to 0x0, the GPIO3 indicates whether an Automatic Haptic Playback (see section 6.8.2) has been requested on any channel (same as bit RQS_PLAY): 1: Automatic Haptic Playback triggered 0: No Automatic Haptic Playback triggered

ADDRESS: 0x03 GPIO															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO3 [3:0]				GPIO2 [3:0]				GPIO1 [3:0]				GPIO0 [3:0]			

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:8	GPIO2 [3:0]	0x0	R/W	Determines the GPIO2 behaviour. By setting GPIO2 [3:0] to 0x7 and setting bit EXT_TRIG to 0x1, the GPIO2 will act as an *input* to trigger haptic waveforms on channel 2 (more detail in section 6.2.10). The following GPIO2 [3:0] values determine the information output on GPIO3: 0x0: State of sense channel 2: 1: Actuator is released 0: Actuator is pressed 0x1: Detection event status on channel 2: 1: No detection event triggered on channel 2 0: Detection event triggered on channel 2 0x2: Detection event status of any channel: 1: No detection event triggered in any channel 0: Detection event triggered on at least one channel 0x3: Indicates whether the waveform is done or the FIFO empty (state of EMPTY bit): 1: Waveform is not done, FIFO is not empty 0: Waveform done, FIFO is empty 0x4: Indicates is the BOS0614 is in Error state, i.e., bits STATE [1:0] are 0x3: 1: No error detected 0: Error detected 0x5: Indicates if maximum. amount of power is used (same as bit MAX_POWER): 1: Amount of power is acceptable 0: Maximum power, distortion likely 0x6: In Direct Mode (bit RAM [1:0] set to 0x0), indicates when next data is needed by generating a pulse of minimum 0.5 µs: 1: Wait before sending new data 0: New data needed (pulse of minimum 0.5 µs) 0x7: When bit EXT_TRIG is set to 0x0, the GPIO2 indicates whether an Automatic Haptic Playback (see section 6.8.2) has been requested on any channel (same as bit RQS_PLAY): 1: Automatic Haptic Playback triggered 0: No Automatic Haptic Playback triggered

ADDRESS: 0x03 GPIO															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO3 [3:0]				GPIO2 [3:0]				GPIO1 [3:0]				GPIO0 [3:0]			

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
7:4	GPIO1 [3:0]	0x0	R/W	Determines the GPIO1 behaviour. By setting GPIO1 [3:0] to 0x7 and setting bit EXT_TRIG to 0x1, the GPIO1 will act as an *input* to trigger haptic waveforms on channel 1 (more detail in section 6.2.10). The following GPIO1 [3:0] values determine the information output on GPIO1: 0x0: State of sense channel 1: 1: Actuator is released 0: Actuator is pressed 0x1: Detection event status on channel 1: 1: No detection event triggered on channel 1 0: Detection event triggered on channel 1 0x2: Detection event status of any channel: 1: No detection event triggered in any channel 0: Detection event triggered on at least one channel 0x3: Indicates whether the waveform is done or the FIFO empty (state of EMPTY bit): 1: Waveform is not done, FIFO is not empty 0: Waveform done, FIFO is empty 0x4: Indicates is the BOS0614 is in Error state, i.e., bits STATE [1:0] are 0x3: 1: No error detected 0: Error detected 0x5: Indicates if maximum. amount of power is used (same as bit MAX_POWER): 1: Amount of power is acceptable 0: Maximum power, distortion likely 0x6: In Direct Mode (bit RAM [1:0] set to 0x0), indicates when next data is needed by generating a pulse of minimum 0.5 µs: 1: Wait before sending new data 0: New data needed (pulse of minimum 0.5 µs) 0x7: When bit EXT_TRIG is set to 0x0, the GPIO1 indicates whether an Automatic Haptic Playback (see section 6.8.2) has been requested on any channel (same as bit RQS_PLAY): 1: Automatic Haptic Playback triggered 0: No Automatic Haptic Playback triggered

ADDRESS: 0x03 GPIO															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GPIO3 [3:0]				GPIO2 [3:0]				GPIO1 [3:0]				GPIO0 [3:0]			

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
3:0	GPIO0 [3:0]	0x0	R/W	Determines the GPIO0 behaviour. By setting GPIO0 [3:0] to 0x7 and setting bit EXT_TRIG to 0x1, the GPIO0 will act as an *input* to trigger haptic waveforms on channel 0 (more detail in section 6.2.10). The following GPIO0 [3:0] values determine the information output on GPIO0: 0x0: State of sense channel 0: 1: Actuator is released 0: Actuator is pressed 0x1: Detection event status on channel 0: 1: No detection event triggered on channel 0 0: Detection event triggered on channel 0 0x2: Detection event status of any channel: 1: No detection event triggered in any channel 0: Detection event triggered on at least one channel 0x3: Indicates whether the waveform is done or the FIFO empty (state of EMPTY bit): 1: Waveform is not done, FIFO is not empty 0: Waveform done, FIFO is empty 0x4: Indicates is the BOS0614 is in Error state, i.e., bits STATE [1:0] are 0x3: 1: No error detected 0: Error detected 0x5: Indicates if maximum. amount of power is used (same as bit MAX_POWER): 1: Amount of power is acceptable 0: Maximum power, distortion likely 0x6: In Direct Mode (bit RAM [1:0] set to 0x0), indicates when next data is needed by generating a pulse of minimum 0.5 µs: 1: Wait before sending new data 0: New data needed (pulse of minimum 0.5 µs) 0x7: When bit EXT_TRIG is set to 0x0, the GPIO0 indicates whether an Automatic Haptic Playback (see section 6.8.2) has been requested on any channel (same as bit RQS_PLAY): 1: Automatic Haptic Playback triggered 0: No Automatic Haptic Playback triggered

Table 23: TC register details

ADDRESS: 0x04 TC															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				POL	PC	TCP [4:0]					TCR [4:0]				

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11	POL	0x1	R/W	Sets GPIO input trigger polarity. 0x1: Trigger pulse is active high 0x0: Trigger pulse is active low
10	PC	0x1	R/W	Shorts the piezo by shorting sensing switch for the duration specified by TCP [4:0] and TCR [3:0]. This feature is used to dissipate momentum energy from the piezo. 0x1: Short piezo at end of waveform 0x0: Do not short piezo at the end of the waveform PC can be set to 0x1 only in RAM Playback and RAM Synthesis modes. In FIFO and Direct modes, bit PC must be set to 0x0 to avoid unexpected results.
9:5	TCP [4:0]	0x5	R/W	Sets the output shorting duration after the end of a waveform for a button press event ($t_{short\text{-}press}$) in milliseconds, determined by: $t_{short-press} = TCP[4:0] \times 3.2\ ms$
4:0	TCR [4:0]	0x5	R/W	Sets the output shorting duration after the end of a waveform for a button release event ($t_{short\text{-}release}$) in milliseconds, determined by: $t_{short-release} = TCR[4:0] \times 3.2\ ms$

Table 24: CONFIG register details

ADDRESS: 0x05 CONFIG															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC	OD	SHORT [1:0]		STR	RAM [1:0]		TOUT	UPI	RST	LOCK	OE	DS	PLAY [2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	SC	0x0	R/W	Sets the behaviour of the channel selection when playing from RAM for RAM Playback mode (bits RAM=0x2) and RAM Synthesis mode (bits RAM=0x3). 0x0: Channels are selected as read in RAM 0x1: Channels are selected with the content of bits [15:12] of REFERENCE register.
14	OD	0x0	R/W	Sets the GPIOs output type. 0x0: Open-drain 0x1: Push-Pull
13:12	SHORT [1:0]	0x2	R/W	Sets the duration of the piezo zeroing for auto-calibration. 0x0: 200 µs 0x1: 350 µs 0x2: 500 µs 0x3: 1000 µs
11	STR	0x0	R/W	Enables automatic incrementing of the register address during communication. Allows the writing of several consecutive registers using only the address of the first register (see Figure 35). 1: Address auto-increment every two bytes 0: User provides one byte of address at every two bytes Regardless the STR bit value, an address of 0x00 (REFERENCE register) will not automatically increment address for more efficient writes to the FIFO or Waveform Synthesizer.

ADDRESS: 0x05 CONFIG															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SC	OD	SHORT [1:0]		STR	RAM [1:0]		TOUT	UPI	RST	LOCK	OE	DS	PLAY [2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
10:9	RAM [1:0]	0x1	R/W	Sets playback mode. 0x0: Direct Mode (RAM not used) 0x1: FIFO Mode 0x2: RAM Playback Mode 0x3: RAM Synthesis Mode
8	TOUT	0x0	R/W	Enables the timeout of the waveform playing in FIFO mode or Direct mode. A timeout occurs and the BOS0614 automatically go to SLEEP mode after 4 ms in the following conditions: • Bit RAM [1] is 0x0 • Bit OE is 0x1 • The FIFO is empty • No data (sample) has been received on the digital interface. 0x1: Enable 0x0: Disable
7	UPI	0x1	R/W	Enables the Unidirectional Power Input. 0x1: Enable 0x0: Disable
6	RST	0x0	R/W	Software reset. The controller resets internal registers to default values and goes into IDLE mode. 0x1: RESET 0x0: Normal operation
5	LOCK	0x0	R/W	Write-protect registers. No registers are write-protected if bit OE is 0x0 whatever bit LOCK value. 0x1: All registers are write-protected except CONFIG and REFERENCE register when bit OE is set to 0x1 0x0: Disable
4	OE	0x0	R/W	Enables waveform playback. 0x1: Enable 0x0: Disable
3	DS	0x0	R/W	Sets the power mode when not playing waveforms (OE = 0). 0x1: SLEEP 0x0: IDLE
2:0	PLAY [2:0]	0x7	R/W	Determines the rate at which data is read to create output waveforms: 0x0: 1024 ksps 0x1: 512 ksps 0x2: 256 ksps 0x3: 128 ksps 0x4: 64 ksps 0x5: 32 ksps 0x6: 16 ksps 0x7: 8 ksps

Table 25: SENSECONFIG register details

ADDRESS: 0x06 SENSECONFIG															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXT_ TRIG	ZPS_ SENS	ZPS	SEQ	SCOMP [1:0]		SCOMPAUTO [1:0]		SAMP[1:0]		SAME	CAL	CH3	CH2	CH1	CH0

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	EXT_TRIG	0x0	R/W	Allows GPIO to trigger a press/release haptic waveform feedback as defined in the corresponding WVP [2:0] and WVR [2:0] registers. External trigger polarity is set by POL. 0x1: External trigger activated for channel with GPIO = 0x7 0x0: No external trigger considered.
14	ZPS_SENS	0x0	R/W	Sets sensitivity of the ZPS wakeup signal. 0x1: Low sensitivity 0x0: High sensitivity
13	ZPS	0x0	R/W	Sets if a ZPS detection need a valid sensing detection to be considered as a valid press. 0x1: A ZPS detection is recognized as a press (not recommended, see section 10) 0x0: A ZPS detection will also need a valid sensing detection to be recognized as a press
12	SEQ	0x0	R/W	Sets if more than one channel with auto triggering can play waveforms at the same time. 0x0: Only one channel plays waveforms at a same time. 0x1: Simultaneous channels can play waveforms at the same time.
11:10	SCOMP [1:0]	0x0	R/W	Sets time between zeroing of output channels to null the effect of discharge on the sensed channels. 0x0: 100 ms 0x1: 50 ms 0x2: 25 ms 0x3: 12.5 ms
9:8	SCOMPAUTO [1:0]	0x1	R/W	Changes the behaviour of SCOMP after the end of a waveform play: 0x0: Value of SCOMP is always used 0x1: 12.5 ms, 25 ms, 50 ms 0x2: 2×12.5 ms, 25 ms, 50 ms 0x3: 4×12.5 ms, 2 × 25 ms, 50 ms
7:6	SAMP [1:0]	0x3	R/W	Sets the reset point of sense voltage to: 0x0: +/-150 mV 0x1: +/-200 mV 0x2: +/-250 mV 0x3: +/-300 mV Default value is recommended.
5	SAME	0x1	R/W	Enables the use of the same configuration for all active sensing channels. 0x1: Enable (SENSE0X registers (0x07-0x0A) are used) 0x0: Disable
4	CAL	0x0	R/W	Calibrates internal sense interface. The sense interface should be calibrated prior to use the sensing feature (see section 6.8) by setting CAL bit to 0x1. The device needs to be calibrated only once after reset or power-up. 0x1: Internal sense interface will be calibrated, bit is self-clear 0x0: Disable

ADDRESS: 0x06 SENSECONFIG															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EXT_ TRIG	ZPS_ SENS	ZPS	SEQ	SCOMP [1:0]		SCOMPAUTO [1:0]		SAMP[1:0]		SAME	CAL	CH3	CH2	CH1	CH0

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
3	CH3	0x1	R/W	Enables channel 3 sensing. 0x1: Enable sensing 0x0: Disable sensing
2	CH2	0x1	R/W	Enables channel 2 sensing. 0x1: Enable sensing 0x0: Disable sensing
1	CH1	0x1	R/W	Enables channel 1 sensing. 0x1: Enable sensing 0x0: Disable sensing
0	CH0	0x1	R/W	Enables channel 0 sensing. 0x1: Enable sensing 0x0: Disable sensing

Table 26: SENSE0 register details

ADDRESS: 0x07 SENSE0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:9	WVR [2:0]	0x0	R/W	Sets the waveform in WFS to be played when an actuator release detection event occurs. See Table 16 for more detail.
8:6	WVP [2:0]	0x0	R/W	Sets the waveform in WFS to be played when an actuator press detection event occurs. See Table 16 for more detail.
5	AUTOR	0x0	R/W	Enables the automatic waveform start (defined with SENSE0.WVR [2:0]) upon either (1) a piezo actuator release detection event for channel 0 (conditions detailed in the list below and in Table 14) or (2) an external trigger event occurred on GPIO0 (as detailed in section 6.2.10). 0x1: Enable 0x0: Disable Piezo actuator release condition for detection triggering: If SENSE0.T2 = 0 & SENSE0.S2 = 0, will start on (S20 & T20) | T10* If SENSE0.T2 = 1 & SENSE0.S2 = 0, will start on T20 If SENSE0.T2 = 0 & SENSE0.S2 = 1, will start on S20 If SENSE0.T2 = 1 & SENSE0.S2 = 1, will start on S20 & T20
4	AUTOP	0x0	R/W	Enables the automatic waveform start (defined with SENSE0.WVP [2:0]) upon either (1) a piezo actuator press detection event for channel 0 (conditions detailed in the list below and in Table 13) or (2) an external trigger event occurred on GPIO0 (as detailed in section 6.2.10). 0x1: Enable 0x0: Disable Piezo actuator press condition for detection triggering: If SENSE0.T1 = 0 & SENSE0.S1 = 0, will start on (S10 & T10) | T20* If SENSE0.T1 = 1 & SENSE0.S1 = 0, will start on T10 If SENSE0.T1 = 0 & SENSE0.S1 = 1, will start on S10 If SENSE0.T1 = 1 & SENSE0.S1 = 1, will start on S10 & T10

ADDRESS: 0x07 SENSE0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
3	S2	0x1	R/W	Enables the comparison of the channel 0 sensed voltage slope to the SENSE0S SLOPE2 [6:0] for S20 detection triggering. 0x1: Enable 0x0: Disable
2	S1	0x0	R/W	Enables the comparison of the channel 0 sensed voltage slope to the SENSE0S SLOPE1 [6:0] for S10 detection triggering. 0x1: Enable 0x0: Disable
1	T2	0x0	R/W	Enables the comparison of the channel 0 sensed voltage amplitude to the SENSE0R THRESHOLD [11:0] for T20 detection triggering. 0x1: Enable 0x0: Disable
0	T1	0x1	R/W	Enables the comparison of the channel 0 sensed voltage amplitude to the SENSE0P THRESHOLD [11:0] for T10 detection triggering. 0x1: Enable 0x0: Disable

*Configuration where S2, T2, S1, T1 are all set to 0x0 may result in unexpected behaviour.

Table 27: SENSE0P register details

ADDRESS: 0x08 SENSE0P															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REP [2:0]			AB	THRESHOLD [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:13	REP [2:0]	0x5	R/W	Sets the time during which the amplitude of the sensed voltage needs to be above/below THRESHOLD [11:0] to set T10 detection flag on channel 0. 0x0:1 µs 0x1:100 µs 0x2: 500 µs 0x3: 1 ms 0x4: 2 ms 0x5: 4 ms 0x6: 8 ms 0x7: 16 ms
12	AB	0x0	R/W	Sets if sensed voltage amplitude should be above/below the THRESHOLD [11:0] to set T10 detection flag on channel 0. 0x1: Below 0x0: Above
11:0	THRESHOLD [11:0]	0x1A6	R/W	Sets the amplitude required to set T10 detection flag on channel 0. The required amplitude in volts is determined by: $Amplitude\ (V) = THRESHOLD[11:0] \times 1.66\ mV$ THRESHOLD [11:0] is a signed decimal value.

Table 28: SENSE0R register details

ADDRESS: 0x09 SENSE0R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REP [2:0]			AB	THRESHOLD [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:13	REP [2:0]	0x0	R/W	Sets the time during which the amplitude of the sensed voltage needs to be above/below THRESHOLD [11:0] to set T20 detection flag on channel 0. 0x0:1 µs 0x1:100 µs 0x2: 500 µs 0x3: 1 ms 0x4: 2 ms 0x5: 4 ms 0x6: 8 ms 0x7: 16 ms
12	AB	0x0	R/W	Sets if sensed voltage amplitude should be above/below the THRESHOLD [11:0] to set T20 detection flag on channel 0. 0x1: Below 0x0: Above
11:0	THRESHOLD [11:0]	0x000	R/W	Sets the amplitude required to set T20 detection flag on channel 0. The required amplitude in volts is determined by: $$Amplitude\ (V) = THRESHOLD[11:0] \times 1.66\ mV$$ THRESHOLD [11:0] is a signed decimal value.

Table 29: SENS0S register details

ADDRESS: 0x0A SENSE0S															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS2	SLOPE2 [6:0]							ABS1	SLOPE1 [6:0]						

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	ABS2	0x1	R/W	Sets if sensed voltage slope value should be above/below the SLOPE2 [6:0] to set S20 detection flag on channel 0. 0x1: Below 0x0: Above
14:8	SLOPE2 [6:0]	0x7B	R/W	Sets signal slope threshold in mV/ms required to set S20 detection flag on channel 0. The slope (S) in mV/ms is determined by: $$S(mV/ms) = SLOPE2[6:0] \times 2.2$$ SLOPE2 [6:0] is a signed decimal value.
7	ABS1	0X0	R/W	Sets if sensed voltage slope value should be above/below the SLOPE1 [6:0] to set S10 detection flag on channel 0. 0x1: Below 0x0: Above
6:0	SLOPE1 [6:0]	0x0	R/W	Set signal slope threshold in mV/ms required to set S10 detection flag on channel 0. The slope (S) in mV/ms is determined by: $$S(mV/ms) = SLOPE1[6:0] \times 2.2$$ SLOPE1 [6:0] is a signed decimal value.

Table 30: SENSE1 register details

ADDRESS: 0x0B SENSE1																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:9	WVR [2:0]	0x0	R/W	Sets waveform in WFS to be played when an actuator release detection event occurs. See Table 16 for more detail.
8:6	WVP [2:0]	0x0	R/W	Sets waveform in WFS to be played when an actuator press detection event occurs See Table 16 for more detail.
5	AUTOR	0x0	R/W	Enables the automatic waveform start (defined with SENSE1.WVR [2:0]) upon either (1) a piezo actuator release detection event for channel 1 (conditions detailed in the list below and in Table 14) or (2) an external trigger event occurred on GPIO1 (as detailed in section 6.2.10). 0x1: Enable 0x0: Disable Piezo actuator release condition for detection triggering: If SENSE1.T2 = 0 & SENSE1.S2 = 0, will start on (S21 & T21) | T11* If SENSE1.T2 = 1 & SENSE1.S2 = 0, will start on T21 If SENSE1.T2 = 0 & SENSE1.S2 = 1, will start on S21 If SENSE1.T2 = 1 & SENSE1.S2 = 1, will start on S21 & T21
4	AUTOP	0x0	R/W	Enables the automatic waveform start (defined with SENSE1.WVP [2:0]) upon either (1) a piezo actuator press detection event for channel 1 (conditions detailed in the list below and in Table 13) or (2) an external trigger event occurred on GPIO1 (as detailed in section 6.2.10). 0x1: Enable 0x0: Disable Piezo actuator press condition for detection triggering: If SENSE1.T1 = 0 & SENSE1.S1 = 0, will start on (S11 & T11) | T21* If SENSE1.T1 = 1 & SENSE1.S1 = 0, will start on T11 If SENSE1.T1 = 0 & SENSE1.S1 = 1, will start on S11 If SENSE1.T1 = 1 & SENSE1.S1 = 1, will start on S11 & T11
3	S2	0x1	R/W	Enables the comparison of the channel 1 sensed voltage slope to the SENSE1S SLOPE2 [6:0] for S21 detection triggering. 0x1: Enable 0x0: Disable
2	S1	0x0	R/W	Enables the comparison of the channel 1 sensed voltage slope to the SENSE1S SLOPE1 [6:0] for S11 detection triggering. 0x1: Enable 0x0: Disable
1	T2	0x0	R/W	Enables the comparison of the channel 1 sensed voltage amplitude to the SENSE1R THRESHOLD [11:0] for T21 detection triggering. 0x1: Enable 0x0: Disable
0	T1	0x1	R/W	Enables the comparison of the channel 1 sensed voltage amplitude to the SENSE1P THRESHOLD [11:0] for T11 detection triggering. 0x1: Enable 0x0: Disable

*Configuration where S2, T2, S1, T1 are all set to 0x0 may result in unexpected behaviour.

Table 31: SENSE1P register details

ADDRESS: 0x0C SENSE1P															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REP [2:0]			AB	THRESHOLD [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:13	REP [2:0]	0x5	R/W	Sets the time during which the amplitude of the sensed voltage needs to be above/below THRESHOLD [11:0] to set T11 detection flag on channel 1. 0x0:1 µs 0x1:100 µs 0x2: 500 µs 0x3: 1 ms 0x4: 2 ms 0x5: 4 ms 0x6: 8 ms 0x7: 16 ms
12	AB	0x0	R/W	Sets if sensed voltage amplitude should be above/below the THRESHOLD [11:0] to set T11 detection flag on channel 1. 0x1: Below 0x0: Above
11:0	THRESHOLD [11:0]	0x1A6	R/W	Sets amplitude required to set T11 detection flag on channel 1. The required amplitude in volts is determined by: $$Amplitude\ (V) = THRESHOLD[11:0] \times 1.66\ mV$$ THRESHOLD [11:0] is a signed decimal value.

Table 32: SENSE1R register details

ADDRESS: 0x0D SENSE1R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REP [2:0]			AB	THRESHOLD [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:13	REP [2:0]	0x0	R/W	Sets the time during which the amplitude of the sensed voltage needs to be above/below THRESHOLD [11:0] to set T21 detection flag on channel 1. 0x0:1 µs 0x1:100 µs 0x2: 500 µs 0x3: 1 ms 0x4: 2 ms 0x5: 4 ms 0x6: 8 ms 0x7: 16 ms
12	AB	0x0	R/W	Sets if sensed voltage amplitude should be above/below the THRESHOLD [11:0] to set T21 detection flag on channel 1. 0x1: Below 0x0: Above
11:0	THRESHOLD [11:0]	0x000	R/W	Sets amplitude required to set T21 detection flag on channel 1. The required amplitude in volts is determined by: $$Amplitude\ (V) = THRESHOLD[11:0] \times 1.66\ mV$$ THRESHOLD [11:0] is a signed decimal value.

Table 33: SENSE1S register details

ADDRESS: 0x0E SENSE1S															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS2	SLOPE2 [6:0]							ABS1	SLOPE1 [6:0]						

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	ABS2	0x1	R/W	Sets if sensed voltage slope value should be above/below the SLOPE2 [6:0] to set S21 detection flag on channel 1. 0x1: Below 0x0: Above
14:8	SLOPE2 [6:0]	0x7B	R/W	Sets signal slope threshold in mV/ms required to set S21 detection flag on channel 1. The slope (S) in mV/ms is determined by: $S(mV/ms) = SLOPE2[6:0] \times 2.2$ SLOPE2 [6:0] is a signed decimal value.
7	ABS1	0X0	R/W	Sets if sensed voltage slope value should be above/below the SLOPE1 [6:0] to set S11 detection flag on channel 1. 0x1: Below 0x0: Above
6:0	SLOPE1 [6:0]	0x0	R/W	Sets signal slope threshold in mV/ms required to set S11 detection flag on channel 1. The slope (S) in mV/ms is determined by: $S(mV/ms) = SLOPE1[6:0] \times 2.2$ SLOPE1 [6:0] is a signed decimal value.

Table 34: SENSE2 register details

ADDRESS: 0x0F SENSE2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:9	WVR [2:0]	0x0	R/W	Sets waveform in WFS to be played when an actuator release detection event occurs. See Table 16 for more detail.
8:6	WVP [2:0]	0x0	R/W	Sets waveform in WFS to be played when an actuator press detection event occurs. See Table 16 for more detail.
5	AUTOR	0x0	R/W	Enables the automatic waveform start (defined with SENSE2.WVR [2:0]) upon either (1) a piezo actuator release detection event for channel 2 (conditions detailed in the list below and in Table 14) or (2) an external trigger event occurred on GPIO2 (as detailed in section 6.2.10). 0x1: Enable 0x0: Disable Piezo actuator release condition for detection triggering: If SENSE2.T2 = 0 & SENSE2.S2 = 0, will start on (S22 & T22) | T12* If SENSE2.T2 = 1 & SENSE2.S2 = 0, will start on T22 If SENSE2.T2 = 0 & SENSE2.S2 = 1, will start on S22 If SENSE2.T2 = 1 & SENSE2.S2 = 1, will start on S22 & T22

ADDRESS: 0x0F SENSE2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
4	AUTOP	0x0	R/W	Enables the automatic waveform start (defined with SENSE2.WVP [2:0]) upon either (1) a piezo actuator press detection event for channel 2 (conditions detailed in the list below and in Table 13) or (2) an external trigger event occurred on GPIO2 (as detailed in section 6.2.10). 0x1: Enable 0x0: Disable Piezo actuator press condition for detection triggering: If SENSE2.T1 = 0 & SENSE2.S1 = 0, will start on (S12 & T12) | T22* If SENSE2.T1 = 1 & SENSE2.S1 = 0, will start on T12 If SENSE2.T1 = 0 & SENSE2.S1 = 1, will start on S12 If SENSE2.T1 = 1 & SENSE2.S1 = 1, will start on S12 & T12
3	S2	0x1	R/W	Enables the comparison of the channel 2 sensed voltage slope to the SENSE2S SLOPE2 [6:0] for S22 detection triggering. 0x1: Enable 0x0: Disable
2	S1	0x0	R/W	Enables the comparison of the channel 2 sensed voltage slope to the SENSE2S SLOPE1 [6:0] for S12 detection triggering. 0x1: Enable 0x0: Disable
1	T2	0x0	R/W	Enables the comparison of the channel 2 sensed voltage amplitude to the SENSE2R THRESHOLD [11:0] for T22 detection triggering. 0x1: Enable 0x0: Disable
0	T1	0x1	R/W	Enables the comparison of the channel 2 sensed voltage amplitude to the SENSE2P THRESHOLD [11:0] for T12 detection triggering. 0x1: Enable 0x0: Disable

*Configuration where S2, T2, S1, T1 are all set to 0x0 may result in unexpected behaviour.

Table 35: SENSE2P register details

ADDRESS: 0x10 SENSE2P															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REP [2:0]			AB	THRESHOLD [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:13	REP [2:0]	0x5	R/W	Sets the time during which the amplitude of the sensed voltage needs to be above/below THRESHOLD [11:0] to set T12 detection flag on channel 2. 0x0:1 µs 0x1:100 µs 0x2: 500 µs 0x3: 1 ms 0x4: 2 ms 0x5: 4 ms 0x6: 8 ms 0x7: 16 ms
12	AB	0x0	R/W	Sets if sensed voltage amplitude should be above/below the THRESHOLD [11:0] to set T12 detection flag on channel 2. 0x1: Below 0x0: Above
11:0	THRESHOLD [11:0]	0x1A6	R/W	Sets amplitude required to set T12 detection flag on channel 2. The required amplitude in volts is determined by: $$Amplitude\ (V) = THRESHOLD[11:0] \times 1.66\ mV$$ THRESHOLD [11:0] is a signed decimal value.

Table 36: SENSE2R register details

ADDRESS: 0x11 SENSE2R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REP [2:0]			AB	THRESHOLD [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:13	REP [2:0]	0x0	R/W	Sets the time during which the amplitude of the sensed voltage needs to be above/below THRESHOLD [11:0] to set T22 detection flag on channel 2. 0x0:1 µs 0x1:100 µs 0x2: 500 µs 0x3: 1 ms 0x4: 2 ms 0x5: 4 ms 0x6: 8 ms 0x7: 16 ms
12	AB	0x0	R/W	Sets if sensed voltage amplitude should be above/below the THRESHOLD [11:0] to set T22 detection flag on channel 2. 0x1: Below 0x0: Above
11:0	THRESHOLD [11:0]	0x000	R/W	Sets amplitude required to set T22 detection flag on channel 2. The required amplitude in volts is determined by: $$Amplitude\ (V) = THRESHOLD[11:0] \times 1.66\ mV$$ THRESHOLD [11:0] is a signed decimal value.

Table 37: SENSE2S register details

ADDRESS: 0x12 SENSE2S															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS2	SLOPE2 [6:0]							ABS1	SLOPE1 [6:0]						

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	ABS2	0x1	R/W	Sets if sensed voltage slope value should be above/below the SLOPE2 [6:0] to set S22 detection flag on channel 2. 0x1: Below 0x0: Above
14:8	SLOPE2 [6:0]	0x7B	R/W	Signal slope threshold in mV/ms required to set S22 detection flag on channel 2. The slope (S) in mV/ms is determined by: $S(mV/ms) = SLOPE2[6:0] \times 2.2$ SLOPE2 [6:0] is a signed decimal value.
7	ABS1	0X0	R/W	Sets if sensed voltage slope value should be above/below the SLOPE1 [6:0] to set S12 detection flag on channel 2. 0x1: Below 0x0: Above
6:0	SLOPE1 [6:0]	0x0	R/W	Sets signal slope threshold in mV/ms required to set S12 detection flag on channel 2. The slope (S) in mV/ms is determined by: $S(mV/ms) = SLOPE1[6:0] \times 2.2$ SLOPE1 [6:0] is a signed decimal value.

Table 38: SENSE3 register details

ADDRESS: 0x13 SENSE3															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11:9	WVR [2:0]	0x0	R/W	Sets waveform in WFS to be played when an actuator release detection event occurs. See Table 16 for more detail.
8:6	WVP [2:0]	0x0	R/W	Sets waveform in WFS to be played when an actuator press detection event occurs. See Table 16 for more detail.
5	AUTOR	0x0	R/W	Enables the automatic waveform start (defined with SENSE3.WVR [2:0]) upon either (1) a piezo actuator release detection event for channel 3 (conditions detailed in the list below and in Table 14) or (2) an external trigger event occurred on GPIO3 (as detailed in section 6.2.10). 0x1: Enable 0x0: Disable Piezo actuator release condition for detection triggering: If SENSE3.T2 = 0 & SENSE3.S2 = 0, will start on (S23 & T23) | T13* If SENSE3.T2 = 1 & SENSE3.S2 = 0, will start on T23 If SENSE3.T2 = 0 & SENSE3.S2 = 1, will start on S23 If SENSE3.T2 = 1 & SENSE3.S2 = 1, will start on S23 & T23

ADDRESS: 0x13 SENSE3															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				WVR [2:0]			WVP [2:0]			AUTOR	AUTOP	S2	S1	T2	T1

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
4	AUTOP	0x0	R/W	Enables the automatic waveform start (defined with SENSE3.WVP [2:0]) upon either (1) a piezo actuator press detection event for channel 3 (conditions detailed in the list below and in Table 13) or (2) an external trigger event occurred on GPIO3 (as detailed in section 6.2.10). 0x1: Enable 0x0: Disable Piezo actuator press condition for detection triggering: If SENSE3.T1 = 0 & SENSE3.S1 = 0, will start on (S13 & T13) | T23* If SENSE3.T1 = 1 & SENSE3.S1 = 0, will start on T13 If SENSE3.T1 = 0 & SENSE3.S1 = 1, will start on S13 If SENSE3.T1 = 1 & SENSE3.S1 = 1, will start on S13 & T13
3	S2	0x1	R/W	Enables the comparison of the channel 3 sensed voltage slope to the SENSE0S SLOPE2 [6:0] for S23 detection triggering. 0x1: Enable 0x0: Disable
2	S1	0x0	R/W	Enables the comparison of the channel 3 sensed voltage slope to the SENSE3S SLOPE1 [6:0] for S13 detection triggering. 0x1: Enable 0x0: Disable
1	T2	0x0	R/W	Enables the comparison of the channel 3 sensed voltage amplitude to the SENSE3R THRESHOLD [11:0] for T23 detection triggering. 0x1: Enable 0x0: Disable
0	T1	0x1	R/W	Enables the comparison of the channel 3 sensed voltage amplitude to the SENSE3P THRESHOLD [11:0] for T13 detection triggering. 0x1: Enable 0x0: Disable

*Configuration where S2, T2, S1, T1 are all set to 0x0 may result in unexpected behaviour.

Table 39: SENSE3P register details

ADDRESS: 0x14 SENSE3P															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REP [2:0]			AB	THRESHOLD [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:13	REP [2:0]	0x5	R/W	Sets the time during which the amplitude of the sensed voltage needs to be above/below THRESHOLD [11:0] to set T13 detection flag on channel 3. 0x0:1 µs 0x1:100 µs 0x2: 500 µs 0x3: 1 ms 0x4: 2 ms 0x5: 4 ms 0x6: 8 ms 0x7: 16 ms
12	AB	0x0	R/W	Sets if sensed voltage amplitude should be above/below the THRESHOLD [11:0] to set T13 detection flag on channel 3. 0x1: Below 0x0: Above
11:0	THRESHOLD [11:0]	0x1A6	R/W	Sets amplitude required to set T13 detection flag on channel 3. The required amplitude in volts is determined by: $$Amplitude\ (V) = THRESHOLD[11:0] \times 1.66\ mV$$ THRESHOLD [11:0] is a signed decimal value.

Table 40: SENSE3R register details

ADDRESS: 0x15 SENSE3R															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REP [2:0]			AB	THRESHOLD [11:0]											

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:13	REP [2:0]	0x0	R/W	Sets the time during which the amplitude of the sensed voltage needs to be above/below THRESHOLD [11:0] to set T23 detection flag on channel 3. 0x0:1 µs 0x1:100 µs 0x2: 500 µs 0x3: 1 ms 0x4: 2 ms 0x5: 4 ms 0x6: 8 ms 0x7: 16 ms
12	AB	0x0	R/W	Sets if sensed voltage amplitude should be above/below the THRESHOLD [11:0] to set T23 detection flag on channel 3. 0x1: Below 0x0: Above
11:0	THRESHOLD [11:0]	0x000	R/W	Sets amplitude required to set T23 detection flag on channel 3. The required amplitude in volts is determined by: $$Amplitude\ (V) = THRESHOLD[11:0] \times 1.66\ mV$$ THRESHOLD [11:0] is a signed decimal value.

Table 41: SENSE3S register details

ADDRESS: 0x16 SENSE3S															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ABS2	SLOPE2 [6:0]							ABS1	SLOPE1 [6:0]						

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	ABS2	0x1	R/W	Sets if sensed voltage slope value should be above/below the SLOPE2 [6:0] to set S23 detection flag on channel 3. 0x1: Below 0x0: Above
14:8	SLOPE2 [6:0]	0x7B	R/W	Sets signal slope threshold in mV/ms required to set S23 detection flag on channel 3. The slope (S) is determined by: $S\ (mV/ms) = SLOPE2[6:0] \times 2.2$ SLOPE2 [6:0] is a signed decimal value.
7	ABS1	0X0	R/W	Sets if sensed voltage slope value should be above/below the SLOPE1 [6:0] to set S13 detection flag on channel 3. 0x1: Below 0x0: Above
6:0	SLOPE1 [6:0]	0x0	R/W	Sets signal slope threshold in mV/ms required to set S13 detection flag on channel 3. The slope (S) is determined by: $S\ (mV/ms) = SLOPE1[6:0] \times 2.2$ SLOPE1 [6:0] is a signed decimal value.

Table 42: SENSESTATUS register details

ADDRESS: 0x17 SENSESTATUS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S23	S13	T23	T13	S22	S12	T22	T12	S21	S11	T21	T11	S20	S10	T20	T10

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	S23	0x0	R	Comparator status for SLOPE2 [6:0] of channel 3. 0x1: Threshold met 0x0: Threshold not met
14	S13	0x0	R	Comparator status for SLOPE1 [6:0] of channel 3. 0x1: Threshold met 0x0: Threshold not met
13	T23	0x0	R	Comparator status for the release threshold of channel 3. 0x1: Threshold met 0x0: Threshold not met
12	T13	0x0	R	Comparator status for the press threshold of channel 3. 0x1: Threshold met 0x0: Threshold not met
11	S22	0x0	R	Comparator status for SLOPE2 [6:0] of channel 2. 0x1: Threshold met 0x0: Threshold not met
10	S12	0x0	R	Comparator status for SLOPE1 [6:0] of channel 2. 0x1: Threshold met 0x0: Threshold not met
9	T22	0x0	R	Comparator status for the release threshold of channel 2. 0x1: Threshold met 0x0: Threshold not met
8	T12	0x0	R	Comparator status for the press threshold of channel 2. 0x1: Threshold met

ADDRESS: 0x17 SENSESTATUS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S23	S13	T23	T13	S22	S12	T22	T12	S21	S11	T21	T11	S20	S10	T20	T10

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
				0x0: Threshold not met
7	S21	0x0	R	Comparator status for SLOPE2 [6:0] of channel 1. 0x1: Threshold met 0x0: Threshold not met
6	S11	0x0	R	Comparator status for SLOPE1 [6:0] of channel 1. 0x1: Threshold met 0x0: Threshold not met
5	T21	0x0	R	Comparator status for the release threshold of channel 1. 0x1: Threshold met 0x0: Threshold not met
4	T11	0x0	R	Comparator status for the press threshold of channel 1. 0x1: Threshold met 0x0: Threshold not met
3	S20	0x0	R	Comparator status for SLOPE2 [6:0] of channel 0. 0x1: Threshold met 0x0: Threshold not met
2	S10	0x0	R	Comparator status for SLOPE1 [6:0] of channel 0. 0x1: Threshold met 0x0: Threshold not met
1	T20	0x0	R	Comparator status for the release threshold of channel 0. 0x1: Threshold met 0x0: Threshold not met
0	T10	0x0	R	Comparator status for the press threshold of channel 0. 0x1: Threshold met 0x0: Threshold not met

Table 43: SENSEDATA0 register details

ADDRESS: 0x18 SENSEDATA0															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENSEDATA [15:0]															

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:0	SENSEDATA [15:0]	0x0	R	Signed representation of the sensing data (accumulator) on channel 0. The amplitude (V) in volts is determined by: $$Amplitude\ (V) = SENSEDATA[15:0] \times 220\ \mu V$$ Valid range is: -16 384<= SENSEDATA [15:0] < 16 383.

Table 44: SENSEDATA1 register details

ADDRESS: 0x19 SENSEDATA1															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENSEDATA [15:0]															

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:0	SENSEDATA [15:0]	0x0	R	Signed representation of the sensing data (accumulator) on channel 1. The amplitude (V) in volts is determined by: $$Amplitude\ (V) = SENSEDATA[15:0] \times 220\ \mu V$$ Valid range is: -16 384<= SENSEDATA [15:0] < 16 383.

Table 45: SENSEDATA2 register details

ADDRESS: 0x1A SENSEDATA2															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENSEDATA [15:0]															
BITS	NAME			DEFAULT		TYPE	DESCRIPTION								
15:0	SENSEDATA [15:0]			0x0		R	Signed representation of the sensing data (accumulator) on channel 2. The amplitude (V) in volts is determined by: $$Amplitude\ (V) = SENSEDATA[15:0] \times 220\ \mu V$$ Valid range is: -16 384<= SENSEDATA [15:0] < 16 383.								

Table 46: SENSEDATA3 register details

ADDRESS: 0x1B SENSEDATA3															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SENSEDATA [15:0]															
BITS	NAME			DEFAULT		TYPE	DESCRIPTION								
15:0	SENSEDATA [15:0]			0x0		R	Signed representation of the sensing data (accumulator) on channel 3. The amplitude (V) in volts is determined by: $$Amplitude\ (V) = SENSEDATA[15:0] \times 220\ \mu V$$ Valid range is: -16 384<= SENSEDATA [15:0] < 16 383.								

Table 47: KPA register details

ADDRESS: 0x20 KPA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				SB [1:0]		FSWMAX [1:0]		KPA [7:0]							
BITS	NAME			DEFAULT		TYPE	DESCRIPTION								
11:10	SB [1:0]			0x3		R/W	Sets boost converter blanking time. 0x0: 35 ns 0x1: 44 ns 0x2: 53 ns 0x3: 62 ns Default value should work for most applications.								
9:8	FSWMAX [1:0]			0x0		R/W	Sets boost converter maximum switching frequency. 0x0: 1 MHz 0x1: 833 kHz 0x2: 666 kHz 0x3: 500 kHz								
7:0	KPA [7:0]			0x10		R/W	Sets the value of the proportional gain (*KPc*) used in the integrated PI controller, which is calculated by: $$KPc = KP[10:0] + KPA[7:0] \times Amplitude$$ Where $Amplitude$ is REFERENCE [11:0] decimal value.								

Table 48: KP_KI register details

ADDRESS: 0x21 KP_KI															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	KIBASE [3:0]				KP [10:0]										

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
14:11	KIBASE [3:0]	0x3	R/W	Determines the pole location (f_{pole}) of the integrated PI controller. The pole location (f_{pole}) in kHz is determined by: $$f_{pole} = \frac{1024}{2^{KIBASE}}$$
10:0	KP [10:0]	0x080	R/W	Sets the physical value ($Kp_{Physical}$) of the integrated PI controller proportional gain. The physical value ($Kp_{Physical}$) in A/V is determined by: $$Kp_{physical} = \frac{KP[10:0] \times 2^{-14}}{R_{sense}}$$

Table 49: DEADTIME register details

ADDRESS: 0x22 DEADTIME															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD_ SENSE	RSVD			DHS [6:0]							DLS [4:0]				

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15	AD_SENSE	0x1	R/W	Enables segments of the sensed signal to stitch together. When enabled, all sensed voltage segments are accumulated in time to provide a signal proportional to the force on the actuator. 0x1 Enable 0x0 Disable
11:5	DHS [6:0]	0x23	R/W	Sets the delay between Low-Side (LS) switch turns off and High-Side (HS) switch turns on. DHS [6:0] is determined by: $$DHS = \frac{2\pi\sqrt{L_1 \times (C_{sw} + C_{par})}}{4 \times 1.1 \times 10^{-9}}$$ Where C_{sw}=220 pF is the typical IC capacitance of pin SW and C_{par} is the parasitic capacitance of L_1 and PCB layout. DHS [6:0] can be adjusted for optimization.
4:0	DLS [4:0]	0x0A	R/W	Sets the delay between the High-Side (HS) switch turns off and Low-Side (LS) switch turns on and Low-Side (LS) switch turns off and High-Side (HS) switch turns on. The default value should work for most applications, but DLS [4:0] can be adjusted for optimization.

Table 50: PARCAP register details

ADDRESS: 0x23 PARCAP															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARCAP [7:0]								I_ON_SCALE [7:0]							

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:8	PARCAP [7:0]	0x0E	R/W	Internal parameter determined by: $$PARCAP[7:0] = \frac{\sqrt{\frac{C_{sw} + C_{par}}{L_1}}}{2^{-11}} \times R_{sense} \times FB_{ratio}$$ Where C_{sw}=220 pF is the typical IC capacitance of pin SW, C_{par} is the parasitic capacitance of L_1 and PCB layout and FB_{ratio} = 19.
7:0	I_ON_SCALE [7:0]	0x33	R/W	Minimum current required to turn ON HS Switch ($I_{ON_{SCALE}}$), which is determined by: $$I\_ON\_SCALE\ [7:0] = round\left(\frac{Latency}{L_1 \times 2^{-12}} \times R_{sense} \times FB_{ratio}\right)$$ Where *Latency* = 50 ns and FB_{ratio} = 19.

Table 51: SUP_RISE register details

ADDRESS: 0x24 SUP_RISE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			CP5	LP	VBUS [4:0]					TI_RISE [5:0]					

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
12	CP5	0X1	R/W	Enables internal 5 V charge pump. 0x1: Enable 0x0: Disable The CP5 should be disabled only if the BOS0614 is supplied at 5 V.
11	LP	0X1	R/W	Enables low sensing power when sensing is enabled (bits SENSECONFIG [3:0]). 0x1: Enable low power sensing 0x0: Disable low power sensing
10:6	VBUS [4:0]	0X0E	R/W	Digital representation of the supply voltage (V_{BUS}) at pin VBUS, as described by: $$VBUS\ [4:0] = \frac{\left(\frac{V_{BUS}}{0.0166}\right)}{16}$$ For V_{BUS}= 3 V write 0x0B. For V_{BUS}= 3.6 V write 0x0E. For V_{BUS}= 5.0 V write 0x13
5:0	TI_RISE [5:0]	0x0F	R/W	Sets the proportional gain for the offset, determined by: $$\text{TI\_RISE}\ [5:0] = \frac{T_{CLK} \times 31.25}{L_1} \times \frac{FB_{ratio}}{R_{Sense}}$$ Where T_{CLK} =70 ns and FB_{ratio} = 19.

Table 52: TRIM register details

ADDRESS: 0x25 TRIM															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRIMRW [1:0]		RSVD				TRIM_OSC [6:0]							TRIM_REG [2:0]		

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:14	TRIMRW [1:0]	0x0	R/W	Trim control bits allowing the adjustment of the internal clock oscillator frequency (TRIM_OSC [6:0]) and 1.8 V internal regulator voltage (TRIM_REG [2:0]), see Figure 36. Hardware fuses values vary from chip-to-chip. More detail is available in section 6.2.4. TRIMRW [1:0] bits are automatically reset to 0x0 after each operation. 0x0: Default behaviour where Hardware fuses are latched to the Trim Block at power-up 0x1: Resets the Trim Block with the Hardware Fuses and then transfers Trim Block data to TRIM_OSC [6:0] & TRIM_REG [2:0] for reading (wait for 1 ms before reading) 0x2: Transfers Trim Block data to TRIM_OSC [6:0] & TRIM_REG [2:0] for reading (wait for 1 ms before reading) 0x3: Writes TRIM_OSC [6:0] & TRIM_REG [2:0] to Trim Block
13:10	RSVD			Reserved.
9:3	TRIM_OSC [6:0]	0x00	R/W	Oscillator trimming bits in two's complement. Step size is around 120 kHz. Note that changing the internal oscillator frequency may induce circuit malfunction and is not recommended for normal operation. 0x3F: Maximum frequency 0x40: Minimum frequency
2:0	TRIM_REG [2:0]	0x0	R/W	1.8 V Regulator trimming bits in two's complement. Step size is around 22 mV. Note that changing the regulator voltage will affect waveform amplitude and is not recommended for normal operation. 0x3: Maximum voltage 0x4: Minimum voltage

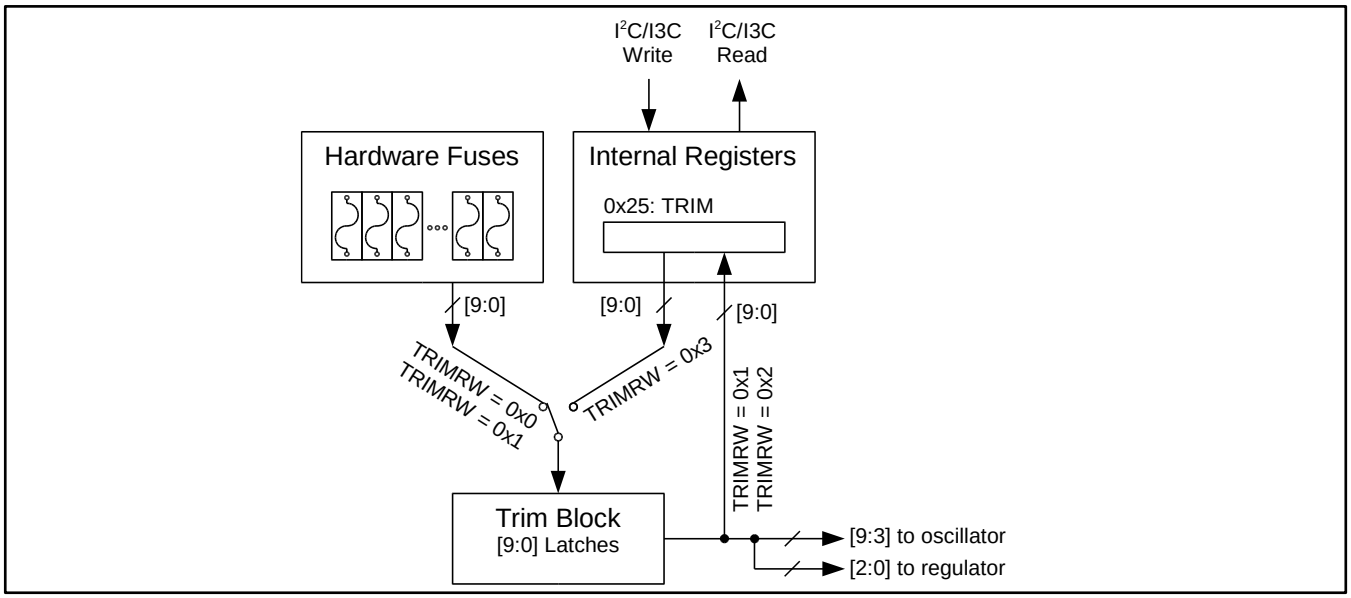


Figure 36: Trim Control Block Diagram

Table 53: CHIPID register details

ADDRESS: 0x26 CHIPID															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHIPID [15:0]															

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
15:0	CHIPID [15:0]	0x0614	R	The BOS0614 identification. CHIPID: 0x0614. Use the I3C chip ID (GETPID) if communicating through I3C. The returned code will be 0x0684 on the I3C interface.

Table 54: VFEEDBACK register details

ADDRESS: 0x28 VFEEDBACK															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		CH3	CH2	CH1	CH0	VFEEDBACK [9:0]									

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
13	CH3	0x0	R	State of output channel 3. 0x1: Channel driven 0x0: Not driven
12	CH2	0x0	R	State of output channel 2. 0x1: Channel driven 0x0: Not driven
11	CH1	0x0	R	State of output channel 1. 0x1: Channel driven 0x0: Not driven
10	CH0	0x0	R	State of output channel 0. 0x1: Channel driven 0x0: Not driven
9:0	VFEEDBACK [9:0]	0x000	R	Voltage measured at HV pin used to drive piezo loads, which is determined by: $$VFEEDBACK\ [9:0] = \frac{V_{HV} \times (2^{10} - 1)}{V_{ref} \times FB_{ratio}}$$ Where $Vref$ = 3.6 V is the ADC input range, $FBratio$ = 19 is the feedback ratio and V_{HV} is the voltage at HV pin.

Table 55: FIFO_STATE

ADDRESS: 0x29 FIFO_STATE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			ERROR	FULL	EMPTY	FIFO_SPACE [9:0]									

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
12	ERROR	0x0	R	Indicates if one of the following errors occurred: OVV, OVT, UVLO or SC. 0x1: An internal error occurred 0x0: No error
11	FULL	0x0	R	Indicates whether the FIFO is full. 0x1: Full 0x0: Not full
10	EMPTY	0x1	R	In Direct mode(RAM bits set to 0x0), indicates when new data is needed: 0: New data needed 1: Wait before sending new data In FIFO mode (RAM bits set to 0x1), indicates when FIFO is empty: 0: FIFO is empty 1: FIFO is not empty In RAM Synthesis or RAM playback mode (RAM bits set to 0x2 or 0x3), indicates when the haptic waveform has finished playing: 0: Waveform done 1: Waveform is not done
9:0	FIFO_SPACE [9:0]	0x00	R	Space available in FIFO for new data. Returns 0x000 when either FULL = 1 or EMPTY = 1.

Table 56: AUTO_STATE register details

ADDRESS: 0x2A AUTO_STATE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				PRESS_RELEASE [3:0]				RQS_ PLAY	WAVE [2:0]			PLAY_CHANNELS [3:0]			

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
11	PRESS_RELEASE[3]	0x0	R	State of sense channel 3. 0x1: Actuator is pressed 0x0: Actuator is released
10	PRESS_RELEASE[2]	0x0	R	State of sense channel 2. 0x1: Actuator is pressed 0x0: Actuator is released
9	PRESS_RELEASE[1]	0x0	R	State of sense channel 1. 0x1: Actuator is pressed 0x0: Actuator is released
8	PRESS_RELEASE[0]	0x0	R	State of sense channel 0. 0x1: Actuator is pressed 0x0: Actuator is released

ADDRESS: 0x2A AUTO_STATE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				PRESS_RELEASE [3:0]				RQS_ PLAY	WAVE [2:0]			PLAY_CHANNELS [3:0]			

BITS	NAME	DEFAULT	TYPE	DESCRIPTION
7	RQS_PLAY		R	Indicates whether an Automatic Haptic Playback (see section 6.8.2) has been requested on any channel. 0x1: Automatic Haptic Playback triggered 0x0: No Automatic Haptic Playback triggered
6:4	WAVE [2:0]	0x0	R	Waveform ID of the wave being played.
3:0	PLAY_ CHANNELS [3:0]	0x0	R	State of the four channels during automatic play. 0x1: Channel driven 0x0: Not driven

Table 57: RAM_DATA register details

ADDRESS: 0x2B RAM_DATA															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM_DATA															
BITS	NAME			DEFAULT		TYPE	DESCRIPTION								
15:0	RAM_DATA			0x0		R	Data present in RAM. To be used in conjunction with the FULL_RAM_READ WFS command.								

Table 58: SENSE_OFFSET register details

ADDRESS: 0x2C SENSE_OFFSET															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							SENSE_OFFSET [8:0]								
BITS	NAME			DEFAULT		TYPE	DESCRIPTION								
8:0	SENSE_OFFSET [8:0]					R	Signed representation of the sense feedback path offset. Use this value to compensate value from SENSERAWx.								

6.10 WFS Command Interpreter

The BOS0614 includes a Waveform Synthesizer (WFS) and a 2 kB on-chip 1024×16 RAM that enable haptic waveform generation using the RAM Playback Mode (bits RAM [1:0] set to 0x2) and RAM Synthesis Mode (bits RAM [1:0] set to 0x3) accessible through REFERENCE register (see section 6.6 and 6.7 for more detail). RAM is programmed using the WFS Command Interpreter and is used to store both RAM Playback and RAM Synthesis configuration data. WFS commands are summarized in Table 59, where word 0 is the command and the following words are the command payload.

Table 59 WFS Commands List

COMMAND	WORD	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RAM ACCESS	0	COMMAND [15:0] = 0x0001															
	1						R/W	ADDRESS [9:0]									
	2	DATA1 [15:0]: required when R/W bit is set to 0x0 for write access															
	3	DATA2 [15:0]: required when R/W bit is set to 0x0 for write access															
	4	DATA3 [15:0]: required when R/W bit is set to 0x0 for write access															
SEQUENCER	0	COMMAND [15:0] = 0x0002															
	1							WAVE ADDRESS [9:0] (WAVEFORM_ID 0)									
	2							WAVE ADDRESS [9:0] (WAVEFORM_ID 1)									
	3							WAVE ADDRESS [9:0] (WAVEFORM_ID 2)									
	…							…									
	15							WAVE ADDRESS [9:0] (WAVEFORM_ID 14)									
RAM SYNTHESIS	0	COMMAND [15:0] = 0x0012															
	1	END WAVEFORM_ID [15:12]				START WAVEFORM_ID [11:8]											
RAM PLAYBACK	0	COMMAND [15:0] = 0x0013															
	1							START ADDRESS [9:0]									
	2							END ADDRESS [9:0]									
BURST RAM WRITE	0	COMMAND [15:0] = 0x0014															
	1							START ADDRESS [9:0]									
	2							DATA COUNT [9:0]									
	3	DATA1 [15:0]															
	…	…															
	2+n	DATAn (n = DATA COUNT [9:0])															
FULL RAM READ	0	COMMAND [15:0] = 0x0015															
FULL RAM READ BREAK	0	COMMAND [15:0] = 0xFF15															

Figure 37 and Figure 38 presents two different I^2C communication sequence examples using either a single communication transaction for each WFS command or a single communication transaction to use several WFS commands. The first word of each WFS command is the command identifier. The number of following words to send depends on the command used.

Transaction 1	
Code	Description / Command 1
0x2C	I²C address
0x00	Select REFERENCE register to use a WFS command
0x0000	WFS command 1
0x0000	Expected word for command 1

Transaction 2	
Code	Description / Command 2
0x2C	I²C address
0x00	Select REFERENCE register to use a WFS command
0x0000	WFS command 2
0x0000	Expected word for command 2

Transaction 3	
Code	Description / Command 3
0x2C	I²C address
0x00	Select REFERENCE register to use a WFS command
0x0000	WFS command 3
0x0000	Expected word for command 3

Figure 37: Generic I²C communication sequence example to use a WFS command with a transaction

Transaction 1	
Code	Description / Command 1
0x2C	I²C address
0x00	Select REFERENCE register to use WFS commands
0x0000	WFS command 1
0x0000	Expected word for command 1

Code	Description / Command 2
0x0000	WFS command 2
0x0000	Expected word for command 2

Code	Description / Command 3
0x0000	WFS command 3
0x0000	Expected word for command 3

Figure 38: Generic I²C communication sequence example to use several WFS commands with a single transaction

6.10.1 RAM ACCESS

Table 60: RAM ACCESS details

COMMAND: 0x0001 RAM ACCESS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND [15:0] = 0x0012															
NOT USED: 0x00					W/R	ADDRESS [9:0]									
DATA1 [15:0]: required when R/W bit is set to 0x0 for write access															
DATA2 [15:0]: required when R/W bit is set to 0x0 for write access															
DATA3 [15:0]: required when R/W bit is set to 0x0 for write access															

BITS	NAME	TYPE	DESCRIPTION
10	R/W	W	0: RAM Write Enable 1: RAM Read Enable
9:0	ADDRESS	W	Write/read start address within the RAM

The RAM ACCESS command is used to do the following:

- In RAM Synthesis mode (RAM [1:0] bits are set to 0x3), program a WAVE or SLICE block to the RAM with the following sequence (as described in Figure 39):
    1. Set bits RAM [1:0] to 0x3 to select RAM Synthesis Mode
    2. Write 0x0001 to the REFERENCE register to use the RAM ACCESS command
    3. Write the following to the REFERENCE register:
        - R/W bit set to 0x0.
        - ADDRESS [9:0] bits set to the RAM start address.
    4. Write the three words of either a WAVE or SLICE block to the REFERENCE register to store in RAM. See section 6.7.1 for details on the content of these words. The RAM address is automatically incremented between each word.
- In either RAM Synthesis or RAM Playback (RAM [1:0] bits are set to either 0x2 or 0x3), read a RAM location with the following sequence (as described in Figure 40):
    1. Set bits RAM [1:0] to 0x3 to select RAM Synthesis Mode
    2. Set bits BC to 0x2B to select RAM_DATA register reading.
    3. Write 0x0001 to REFERENCE register to use the RAM ACCESS command.
    4. Write the following to the REFERENCE register:
        - R/W bit set to 0x1.
        - ADDRESS [9:0] bits set to the RAM address to read.
    5. Read 2 bytes.

Transaction 1 : Set RAM Synthesis Mode	
Code	Description
0x2C+ W	I²C address, write access
0x05	Select CONFIG register
0x2697	Set RAM Synthesis Mode

Transaction 2 : Use RAM ACCESS Command	
Code	Description
0x2C+ W	I²C address
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : RAM ACCESS
0x0063	Set RAM start address 0x063 for write access
0x0100	DATA 1
0x0102	DATA 2
0x000E	DATA 3

Figure 39: I²C communication sequence for RAM write using RAM ACCESS command

Transaction 1 : Set RAM Synthesis Mode	
Code	Description
0x2C+ W	I²C address, write access
0x05	Select CONFIG register
0x2697	Set RAM Synthesis Mode

Transaction 2 : Configure Broadcast	
Code	Description
0x2C+ W	I²C address, write access
0x02	Select READ register
0x002B	Set bit BC for RAM_DATA reading

Transaction 3 : Use RAM ACCESS Command	
Code	Description
0x2C+ W	I²C address, write access
0x00	Select REFERENCE register to access to WFS Register
0x0001	WFS command : RAM ACCESS
0x0463	Set RAM address 0x063 for read access

Transaction 4 : Set the RAM SYNTHESIS WRITE register	
Code	Description
0x2C+ R	I²C address, read access
0x0000	Read 2-byte

Figure 40: RAM ACCESS sequence for RAM read

6.10.2 SEQUENCER

Table 61: SEQUENCER command details

COMMAND: 0x0002 SEQUENCER															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND [15:0] = 0x0002															
NOT USED: 0x00						WAVE ADDRESS [9:0] (WAVEFORM_ID 0)									
NOT USED: 0x00						WAVE ADDRESS [9:0] (WAVEFORM_ID 1)									
…						…									
NOT USED: 0x00						WAVE ADDRESS [9:0] (WAVEFORM_ID 14)									

BITS	NAME	TYPE	DESCRIPTION
9:0	WAVE ADDRESS	W	A WAVE ADDRESS is the address of a WAVE block in the RAM. The SEQUENCER can store up to 15 different WAVE ADDRESS in WAVEFORM_ID 0 to WAVEFORM_ID 14 registers.

The SEQUENCER is composed of 15 registers numbered 0x0 to 0xE (WAVEFORM_ID 0 to WAVEFORM_ID 14). Each WAVEFORM_ID contains a WAVE block RAM address. The SEQUENCER command is used to store WAVE block address into each of the 15 WAVEFORM_ID of the SEQUENCER.

The communication sequence to program the WAVEFORM_IDs into the SEQUENCER includes the following:

- Write 0x0002 to the REFERENCE register to use SEQUENCER command.
- Write 15×10-bit words to the REFERENCE register to set the WAVEFORM_ID 0 to WAVEFORM_ID 14 in ascending order to the SEQUENCER. It is not possible to write a single WAVEFORM_ID register. All 15 WAVEFORM_ID must be written. The WAVEFORM_ID registers that are not used may be assigned to any value.

Note that the communication sequence assumes that bits RAM [1:0] are set to 0x3.

6.10.3 RAM SYNTHESIS

Table 62: RAM SYNTHESIS command details

COMMAND: 0x0012 RAM SYNTHESIS															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND [15:0] = 0x0012															
END WAVEFORM_ID [3:0]				START WAVEFORM_ID [3:0]				NOT USED: 0x00							

BITS	NAME	TYPE	DESCRIPTION
15:12	END WAVEFORM_ID	W	Set the END WAVEFORM_ID number (numbered 0x0 to 0xE, see SEQUENCER command) pointing to the last WAVE block to play.
11:8	START WAVEFORM_ID	W	Set the START WAVEFORM_ID number (numbered 0x0 to 0xE, see SEQUENCER command) pointing to the first WAVE block to play.

In RAM Synthesis (bits RAM [1:0] set to 0x3), the SEQUENCER will play all WAVE blocks starting from START WAVEFORM_ID up to END WAVEFORM_ID.
Any write with the RAM SYNTHESIS command indicates that the waveform from START WAVEFORM_ID up to END WAVEFORM_ID is ready to be played. If bit OE is already set to 0x1, the waveform will start to play immediately after the RAM SYNTHESIS command is written. If the bit AUTOP or AUTOR of any sensing channel (registers 0x07, 0x0B, 0x0F and 0x13) is used, the waveform will be automatically played upon a detection event. See section 6.8.2 for more detail.
The communication sequence to use the RAM SYNTHESIS command includes the following:

1. Write 0x0012 to REFERENCE register to use the RAM SYNTHESIS command.
2. Write the following to REFERENCE register:
    - Bits 15:12 with END WAVEFORM_ID number (0x0 to 0xE).
    - Bits 11:8 with START WAVEFORM_ID number (0x0 to 0xE).

Note that the communication sequence assumes that bits RAM [1:0] are set to 0x3.

6.10.4 RAM PLAYBACK

Table 63: RAM PLAYBACK command details

COMMAND: 0x0013 RAM PLAYBACK															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND [15:0] = 0x0013															
NOT USED: 0x00						START ADDRESS [9:0]									
NOT USED: 0x00						END ADDRESS [9:0]									

BITS	NAME	TYPE	DESCRIPTION
9:0	START ADDRESS	W	Set the RAM start addresses for fetching RAM Playback samples.
9:0	END ADDRESS	W	Set the RAM end address for fetching RAM Playback samples, which is the last sample read during playback.

The start and end addresses entered with the RAM PLAYBACK command indicate the location in RAM of the samples to be fetched when the RAM Playback is initiated. The 16-bit samples in RAM use the same format as for the direct MODE (see section 6.4) and FIFO mode (see section 6.5) and includes the following:

- Bits [15:12] are the enabled channels.
- Bits [11:0] are the waveform amplitude, as given in by the equation given in Table 18.

The samples in RAM are written using BURST RAM WRITE command.

The use of the RAM PLAYBACK command indicates that the waveform is ready to be played. Thus, if OE bit is set 0x1, the waveform will start to play. When using bit AUTOP or AUTOR of any channel (registers 0x07, 0x0B, 0x0F and 0x13), the BOS0614 will automatically start playing upon a detection event. See section 6.8.2 for more detail.

The communication sequence to program the START and END ADDRESS using the RAM PLAYBACK command includes the following:

1. Write waveform data in RAM using BURST RAM WRITE command.
2. Write 0x0013 to the REFERENCE register to use the RAM PLAYBACK command.
3. Write the START ADDRESS word to the REFERENCE register.
4. Write the END ADDRESS word to the REFERENCE register.

Note that the communication sequence assumes that bits RAM [1:0] are set to 0x2.

6.10.5 BURST RAM WRITE

Table 64: BURST RAM WRITE command details

COMMAND: 0x0014 BURST RAM WRITE															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND [15:0] = 0x0014															
NOT USED: 0x00						START ADDRESS [9:0]									
NOT USED: 0x00						DATA COUNT [9:0]									
DATA [15:0]															

BITS	NAME	TYPE	DESCRIPTION
9:0	START ADDRESS	W	10-bit address from where to start writing in the RAM with the following constraint: 0 ≤ START ADDRESS ≤ 1023
9:0	DATA COUNT	W	The number of data words to be written on the RAM with the following constraint: DATA COUNT has a maximum value of 1023. DATA COUNT ≤ 1023 – START ADDRESS
15:0	DATA	W	Data to be written in the RAM using the same format as the REFERENCE register.

The BURST RAM WRITE command is used to write multiple words to the RAM when using the RAM Playback Mode (bits RAM [1:0] are set to 0x2). The maximum value allowed to be written in RAM is 3593 (0xE09) which correspond to 60 V at output channels.

The communication sequence to write to RAM using the BURST RAM WRITE WFS command includes the following:

1. Write 0x0014 to the REFERENCE register to use the BURST RAM WRITE command.
2. Write the RAM START ADDRESS word to the REFERENCE register.
3. Write the DATA_COUNT word to the REFERENCE register.
4. Write the number of DATA [15:0] words equal to DATA COUNT. RAM write address is incremented automatically between words.

Note that the communication sequence assumes that bits RAM [1:0] are set to 0x2.

6.10.6 FULL RAM READ

Table 65: FULL RAM READ command details

COMMAND: 0x0015 FULL RAM READ															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND [15:0] = 0x0015															

In RAM Synthesis or RAM Playback mode (bits RAM [1:0] set to 0x2 or 0x3), the FULL RAM READ command is used to read the full RAM content on the communication interface. The device will stay in this mode until all the 1024 RAM addresses have been read or until the FULL RAM READ BREAK command is used.

The communication sequence to use the FULL RAM READ command includes the following:

1. Set bits BC to 0x2B to select RAM_DATA reading.
2. Write 0x0015 to REFERENCE register to use the FULL RAM READ command.
3. Write 0x0000 (or any value except 0xFF15) to REFERENCE register.
4. Read 2 bytes
5. Repeat step 3) and 4) until the last RAM address or until using the FULL RAM READ BREAK command. The RAM address is automatically incremented.

Note that the communication sequence assumes that bits RAM [1:0] are set to 0x2 or 0x3.

6.10.7 FULL RAM READ BREAK

Table 66: FULL RAM READ BREAK command

COMMAND: 0xFF15 FULL RAM READ BREAK															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMMAND [15:0] = 0xFF15															
The FULL RAM READ BREAK command 0xFF15 is used to stop the RAM content reading loop started with the FULL RAM READ command.															

7 Implementation

7.1 Typical Schematics

The Figure 41 and Figure 42 presents the typical schematics for non-UPI and UPI configuration.

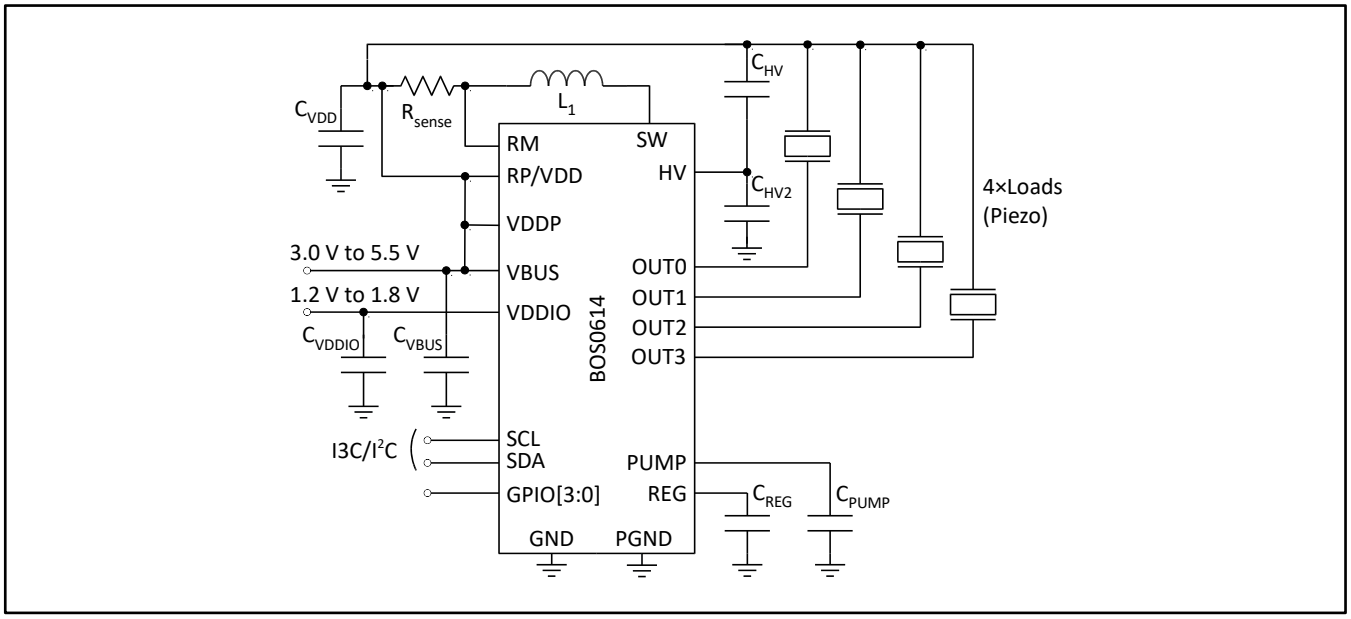


Figure 41: Typical schematic (non-UPI configuration)

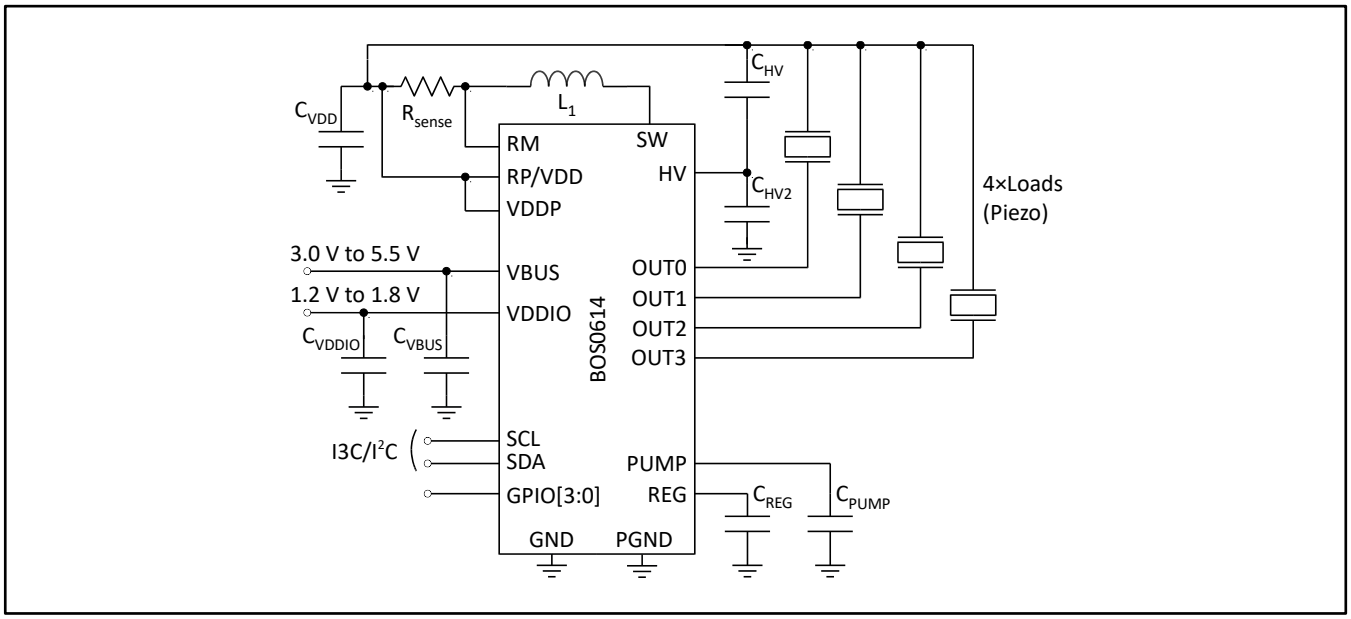


Figure 42: Typical schematic with UPI configuration.

7.2 External Components

The Table 67 lists the recommended components required for a typical application with UPI configuration and a Li-ion battery (3.3 to 4.2 V) connected to V_{BUS} used to drive a single 400 nF load at 60 V.

A Bill of Material (BoM) Calculator, available at www.boreas.ca, can also be used to determine the components for a specific application.

Table 67: Recommended external components for an output voltage of 60 V and 400 nF load (one channel) with Li-ion battery

COMPONENT	DESCRIPTION	TYPICAL VALUE
C_{VBUS}	Input capacitor	100nF
C_{VDD}	Supply decoupling capacitor	100 µF
C_{VDDIO}	VDDIO decoupling capacitor	100 nF
C_{REG}	Regulator capacitor	100 nF
C_{PUMP}	Voltage pump capacitor	100 nF
C_{HV}	Output capacitor to VDD	20 nF (1)
C_{HV2} (2)	Output capacitor to PGND	1.5 nF
R_{sense}	Current sense resistor	130 mΩ, 500 mW
L_1	Inductor	10 µH

(1) C_{HV} is 5% of the maximum load, which is the maximum load capacitance driven at the same time. If four identical actuators are connected to the four channels, but no more than two actuators are driven at the same time, the maximum load is the addition of the capacitance of two actuators.
(2) The recommended CHV2 type is X7R / 100 V in a 0603 package.

7.3 Initialization

7.3.1 Power-Up Sequence with an Active Host MCU

With a powered-up and active MCU connected to its digital interface, the BOS0614 can be powered-up with the following sequence:

1. Apply power to the BOS0614 device.
2. Wait 10 ms for the BOS0614 to perform its initialisation sequence and enter SLEEP mode.
3. Wake-up from SLEEP by writing on the I^2C/I3C bus.
4. Wait 50 µs for the BOS0614 to reach IDLE mode.
5. Program the main registers to the appropriate values according to your application.
6. If required, write data in RAM.
7. BOS0614 is ready for waveform playback.

7.3.2 Power-Up Sequence with the Piezo Actuator Sensing

The default parameters of the BOS0614 allow the device to power-up using a piezo actuator sensed signal, without the need of any active MCU connected to its digital interface. This feature is useful when

the BOS0614 is used to replace power buttons. In this case, the BOS0614 can be powered-up with the following sequence:

1. Apply power to the BOS0614 device.
2. Wait 10 ms for the BOS0614 to performs its initialisation sequence and enter SLEEP mode.
3. Wake-up from SLEEP by pressing on one connected piezo actuator with enough force to trigger a press event (see the main register map in section 6.9 for default values). The corresponding GPIO will be pulled down and no haptic feedback will be triggered.
4. Hold the button for as long as needed to power-up your system.
5. Program the main registers to the appropriate values according to your application.
6. If required, write data in RAM.
7. BOS0614 is ready for waveform playback.

7.3.3 Start-Up Sequence

Once the BOS0614 is powered up, it can wake-up from SLEEP mode with either a MCU communication or a Zero Power Sensing (configuration is detailed in section 6.2.9).

The following start-up sequence applies when waking-up with a MCU communication:

1. Wake-up from SLEEP by writing on the I^2C/I3C bus. The data will wake-up the IC but will not have any effect on the configuration of the registers.
2. Wait 50 µs for the BOS0614 to reach IDLE mode.
3. Do the two following consecutive writes:
    - Set bit OE to 0x1
    - Set bit OE to 0x0
4. Program the main registers to the appropriate values according to your application (optional).
5. Write data in RAM (optional).
6. BOS0614 is ready for waveform playback.

The following start-up sequence applies when waking-up with Zero Power Sensing:

1. Write a valid data to the IC within 100 ms of the actuator release, or the BOS0614 will return to SLEEP mode.
2. Program the main registers to the appropriate values according to your application (optional).
3. Write data in RAM (optional).
4. BOS0614 is ready for waveform playback.

7.4 Design Methodology: Selection of Component

This section details the methodology to properly select the circuit components.

Piezoelectric actuators are subject to capacitance increase as a function of the voltage applied on it. If this capacitance increase is not specified in the actuator datasheet, assume a 50% over the voltage range and use this increased capacitance value in all calculations in this section.

Note that the calculations presented in this section provide approximate values of parameters and the values measured in practice could be different.

7.4.1 Load Selection

The BOS0614 is designed to drive simultaneously on all its channels a total effective load ($Z_{L\text{-}TOT}$) of up to 468 Ω at 60 V with a 3 V supply voltage (V_{DD}). Each channel has been optimized to drive a maximum effective load of 935 Ω with same conditions. Larger load can be driven if the waveform amplitude is

reduced or the supply voltage increased (V_{DD}), as shown in Figure 13. The conditions must be selected so as not to exceed the maximum peak transient current per channel ($I_{pk\text{-}OUT}$) of 1 A, and the maximum current in L_1 (I_{pk}) of 2 A which is equivalent to the sum of the peak transient current ($I_{pk\text{-}OUT}$) of all channels that is limited by R_{sense} (see section 7.4.4 for R_{sense} selection).

You can use the following procedure to estimate the maximum peak current on a channel using the desired conditions (the peak current could be higher in practice):

1. Determine the output signal maximum frequency (f_{OUT}), e.g., 300 Hz
2. Determine the maximum amplitude of the waveform (V_{pk}), e.g., 60 V
3. Determine the minimum supply voltage (V_{DD}) value during operation (consider the voltage drop on V_{DD} line), e.g., 3 V
4. Determine the maximum load to drive on the channel (C_L), e.g., 800 nF
5. Calculate the maximum power transfer point:

$$V_{out}(V) = \frac{V_{pk}}{2}(1 + \sin(30)) + V_{DD} \quad (1)$$

$$\overline{I_{out}}\,(A) = \pi f_{OUT} C_L V_{pk} \cos(30) \quad (2)$$

6. Calculate the average input current using:

$$\overline{I_{in}}\,(A) = 1.5 \times \frac{V_{out}\overline{I_{out}}}{V_{DD}} \quad (3)$$

7. Calculate the inductor peak current:

$$I_{pk-OUT}\,(A) = 1.5 \times \overline{I_{IN}} \quad (4)$$

7.4.2 C_{HV} Selection

Regardless of the type of waveform played, the required C_{HV} capacitance is determined by the total load capacitance of all output channels ($C_{L\text{-}TOT}$) using the following:

$$C_{HV} = 5\%\ C_{L-TOT} \quad (5)$$

The C_{HV} capacitor should have a voltage rating at least equivalent to the maximum amplitude of the waveform (e.g., a C_{HV} capacitor with a minimum voltage rating of 60 V is required to play a 60 V waveform).

7.4.3 L_1 Selection

A 10 µH inductor (L_1) is recommended, but the BOS0614 can use several inductor types. The minimum saturation current of the inductor must be greater than the peak current at SW pin (I_{pk}) which is equivalent to the sum of the peak transient current ($I_{pk\text{-}OUT}$) of all channels, as calculated in section 7.4.1.

Select the inductor with the smallest DCR value possible.

7.4.4 *R_{sense}* Selection

R_{sense} component limits the current injected to the BOS0614 power converter. The *R_{sense}* value must be selected to enable a current range appropriate for the peak current at SW pin (I_{pk}) determined in section 7.4.1. R_{sense} is determined by:

$$R_{sense} = \frac{0.256\ (V)}{I_{pk}} \quad (6)$$

The power rating of R_{sense} must be chosen according to your application requirements. The RMS current in the resistor will be much lower than the current limit set. Table 68 shows an example of conservative power ratings for different I_{pk} current.

Table 68: Inductor peak current limit, min/max values

R_{sense} (mΩ)	I_{PK} (A)	POWER RATING (W)	COMMENT
130	2	0.5	Minimum allowed value
250	1	0.25	
500	0.5	0.125	

7.4.5 Input Capacitor (C_{VDD})

An input capacitor (C_{VDD}) must be placed next to the inductor because of the power converter current requirement. A low-ESR capacitor C_{VDD} of at least 10 µF is recommended.

If the Unidirectional Power Input (UPI) mode is enabled (UPI bit set to 0x1), the energy recovered from the load in reverse mode accumulates on C_{VDD}. Energy accumulation on C_{VDD} causes the input voltage to increase. This voltage increase must not cause the total C_{VDD} voltage to exceed the maximum recommended V_{DD} of 5.5 V. The minimum C_{VDD} capacitance value can be determined by:

$$C_{VDD} = \frac{C_{load} V_{pk}^2}{V_{DD\_max}^2 - V_{BUS\_max}^2} \quad (7)$$

Select a capacitor with an effective capacitance close to the calculated C_{VDD} value. Note that tantalum capacitors are preferred over ceramic capacitors which generally have a high DC bias characteristic that significantly reduces the effective capacitance. Note that if the calculated C_{VDD} capacitance is too large, which would require large capacitor footprint, it could be replaced by a 10 µF C_{VDD} in parallel with a Zener diode that would drain the excess charges.

7.4.6 Validating Components Choice

The MAX_POWER bit can be monitored to validate if the components choice allows a peak current I_{pk} high enough. If MAX_POWER bit is 0x1, it means the peak current calculated is too low and the selected components might need to be changed. It is important to note that a higher inductor DCR will decrease the BOS0614 efficiency and lead to a higher effective I_{pk} requirement.

Sizing the system to operate over a wide range of conditions requires bigger passive components (C_{VDD}, L_1 and R_{sense}) to accommodate higher peak current. Thus, defining the operating conditions is important

in applications where space and cost are critical. For example, to reduce the BOM, one could do the following:

- Limit the haptic amplitude when using a lower V_{DD} supply voltage.
- Limit the number of channels playing haptic at the same time.
- Decrease the output signal frequency.

7.5 Design Methodology: Programming

Many operational settings are adjustable through the digital front end. This section presents the typical parameters that can be adjusted to adapt the BOS0614 to a specific design.

7.5.1 Loop Controller

The BOS0614 implements a proportional-integral (PI) control loop feedback that can be optimized if required with the following parameters:

- Set proportional gain: KP [10:0]
- Set proportional gain term related to waveform amplitude: KPA [7:0]
- Set integral term: KIBASE [3:0]

Table 69 shows the recommended loop controller parameters for a 1.6 µF load operating at up to 60 V and 300 Hz with L_1=10 µH inductor and R_{SENSE}= 130 mΩ. While it is possible to work with the same set of parameters for 1 to 4 active channels, performance can be optimized by adjusting the loop controller parameters to the number of simultaneous active channels.

Table 69: Loop controller parameters

PARAMETER	RECOMMENDED VALUE	COMMENT
KP [10:0]	128 (0x80), default	KP [10:0] could be reduced when using small load.
KPA [7:0]	16 (0x10), default	KPA [7:0] could be reduced when using small load.
KIBASE [3:0]	3 (0x3), default	KIBASE [3:0] could be increased to 3 or 4 when using a larger inductor.

7.5.2 Power Efficiency

The power efficiency of the BOS0614 and haptic waveform integrity can be optimized by configuring the internal controller and the switching timing of the internal power MOSFETs (Low-Side and High-Side switch). This can be done by modifying the following registers based on selected inductor value (L_1) and current sense limit (R_{sense}):

- Set proportional gain: KP [10:0]
- Set the nominal supply voltage (V_{BUS}) of the design with VBUS [4:0]
- Adjust power switch deadtime with bits DHS [6:0] and DLS [4:0]
- Adjust minimum current required to turn-on HS with bits I_ON_SCALE [7:0]
- Adjust typical capacitance value on pin SW with bits PARCAP [7:0]
- Adjust proportional gain for the offset with TI_RISE [5:0]

8 PCB Layout Example

Figure 43 presents a 4-layer PCB layout example based on the following considerations:

- Recommended layers are: Top, GND plane, Power plane (split with V_{DD} and V_{BUS}), Bottom
- Close placement of components L_1, R_{sense} and C_{VDD} to minimize the area of the high current loop formed by these components
- L_1 is a TDK Corporation VLS4012HBX series inductor with 4×4 mm package
- C_{VDD} capacitor is a 1206 (3216 metric) package, adequate for UPI configuration
- Components C_{HV} and C_{HV2} are respectively in 0805 (2012 metric) and 0603 (1608 metric) packages
- Components C_{PUMP}, C_{REG}, C_{VDDIO} and C_{VBUS} are in 0402 (1005 metric) package
- Component R_{SENSE} is in 0805 (2012 metric) package
- Traces connecting L_1, R_{SENSE} and C_{VDD} are as wide as possible to minimize resistance, and multiple vias are used, when possible, to reduce both via resistance and inductance
- All signal lines are 6 mils (0.152 mm) wide, minimum spacing of 6 mils
- All other lines are 8 mils (0.203 mm) wide, minimum spacing of 6 mils
- Requires 0.15 mm vias and Via-in-Pad technology for vias inside U1

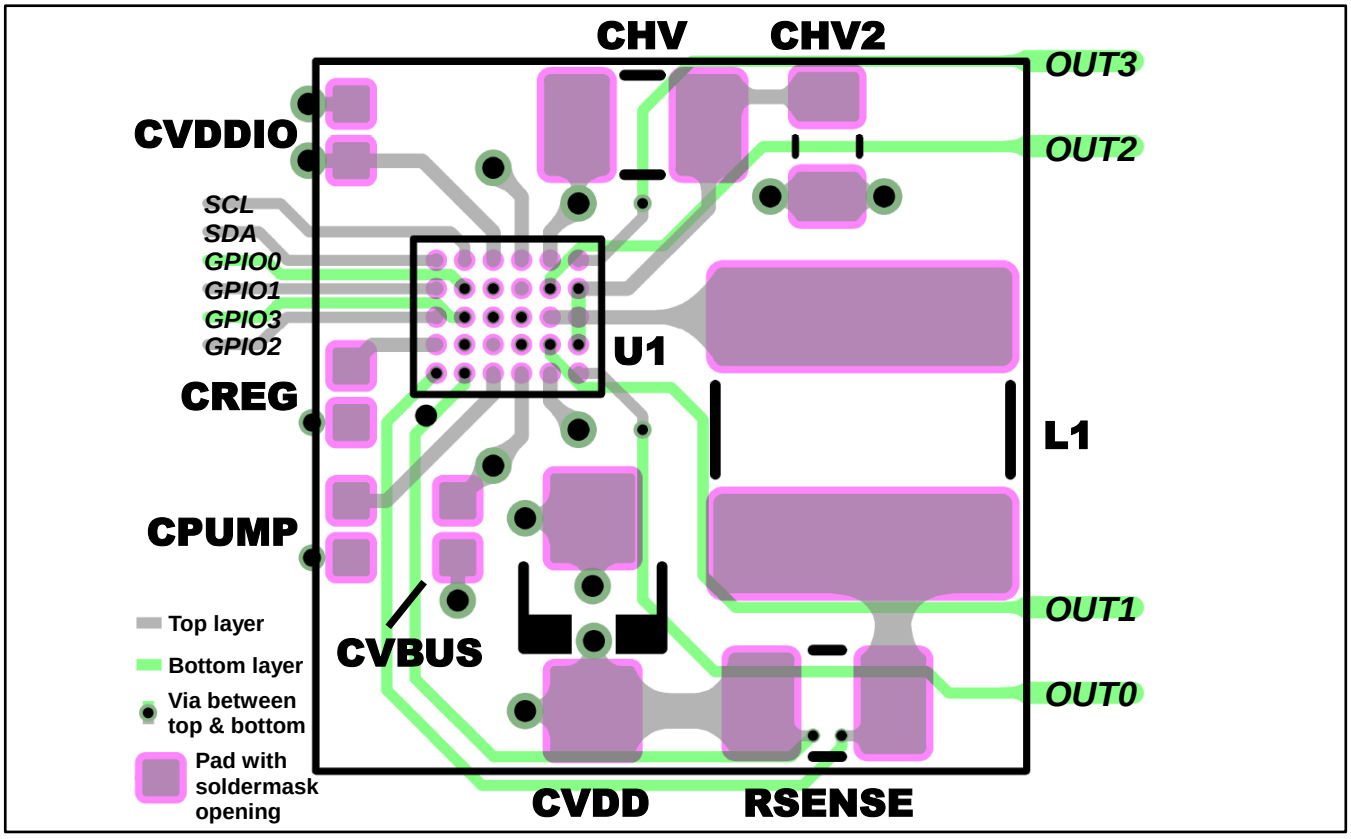


Figure 43: Typical configuration PCB layout example

9 Mechanical Information

9.1 WLCSP Package Description

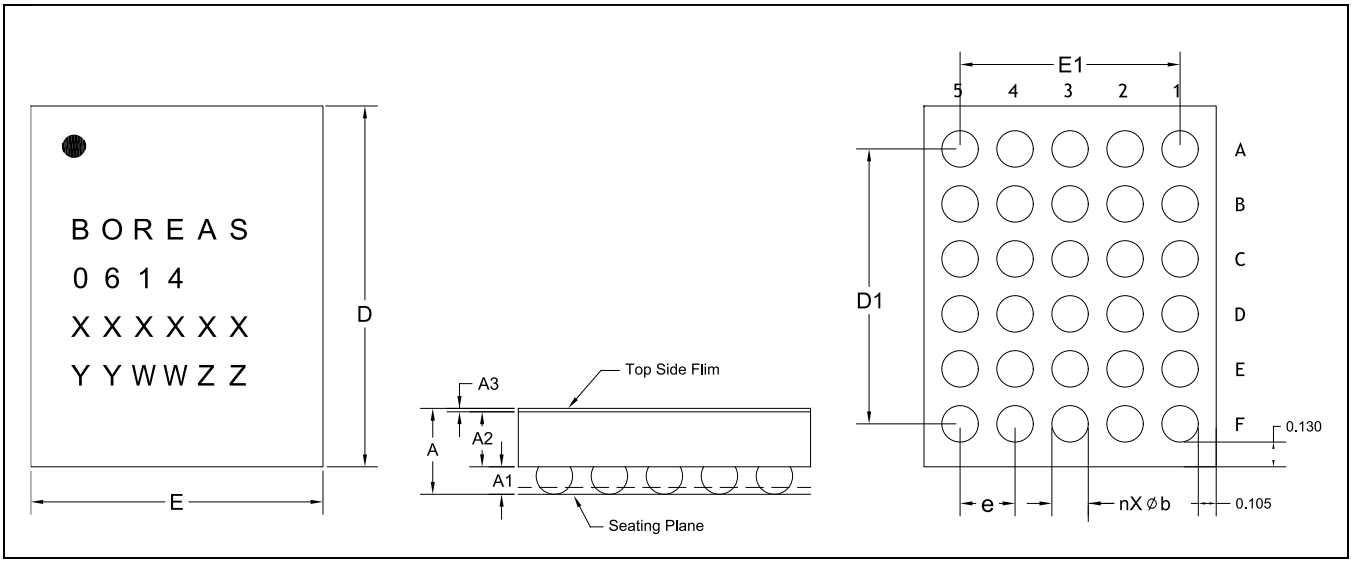


Figure 44: WLCSP 30B 2.1mm × 2.5mm package outline drawing with top, side and bottom view

Table 70: WLCSP 30B 2.1mm × 2.5mm package dimensions

SYMBOL	MILLIMETERS			MILS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.585	0.625	0.665	23.0	24.6	26.2
A1	0.180	0.200	0.220	7.1	7.9	8.7
A2	0.380	0.400	0.420	15.0	15.7	16.5
A3	0.022	0.025	0.028	0.9	1.0	1.1
E	2.055	2.075	2.095	80.9	81.7	82.5
D	2.505	2.525	2.545	98.6	99.4	100.2
E1	1.60 BSC			63.0 BSC		
D1	2.00 BSC			78.7 BSC		
e	0.40 BSC			15.7 BSC		
b	0.245	0.265	0.285	9.6	10.4	11.2

BSC: Basic Spacing between Center.

Four lines are branded on the package:

(1) Company Name: BOREAS
(2) Device Marking / Product Name: 0614
(3) Wafer Batch Number (XXXXXX)
(4) Assembly Date (YYWW, year and week) with Assembly House Code (ZZ)

9.2 WLCSP Package Soldering Footprint

The use of non-solder mask defined (NSMD) pads is recommended, with 0.05 mm solder mask expansion as shown in Figure 45.

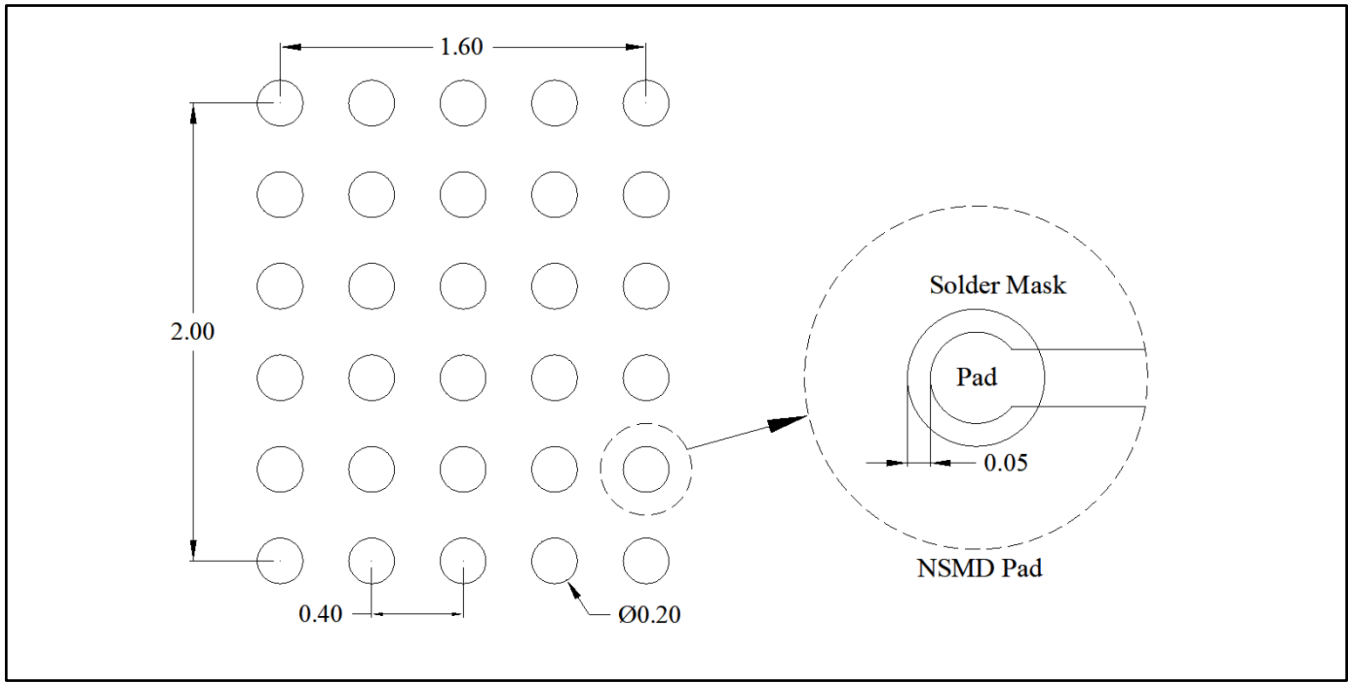


Figure 45: WLCSP 30B 2.1mm × 2.5mm soldering footprint (NOT TO SCALE)

9.3 WLCSP Reflow

BOS0614 supports JEDEC J-STD-020D.1 reflow profile using SAC405 bumps. The profile must be optimized for specific PCB assembly conditions.

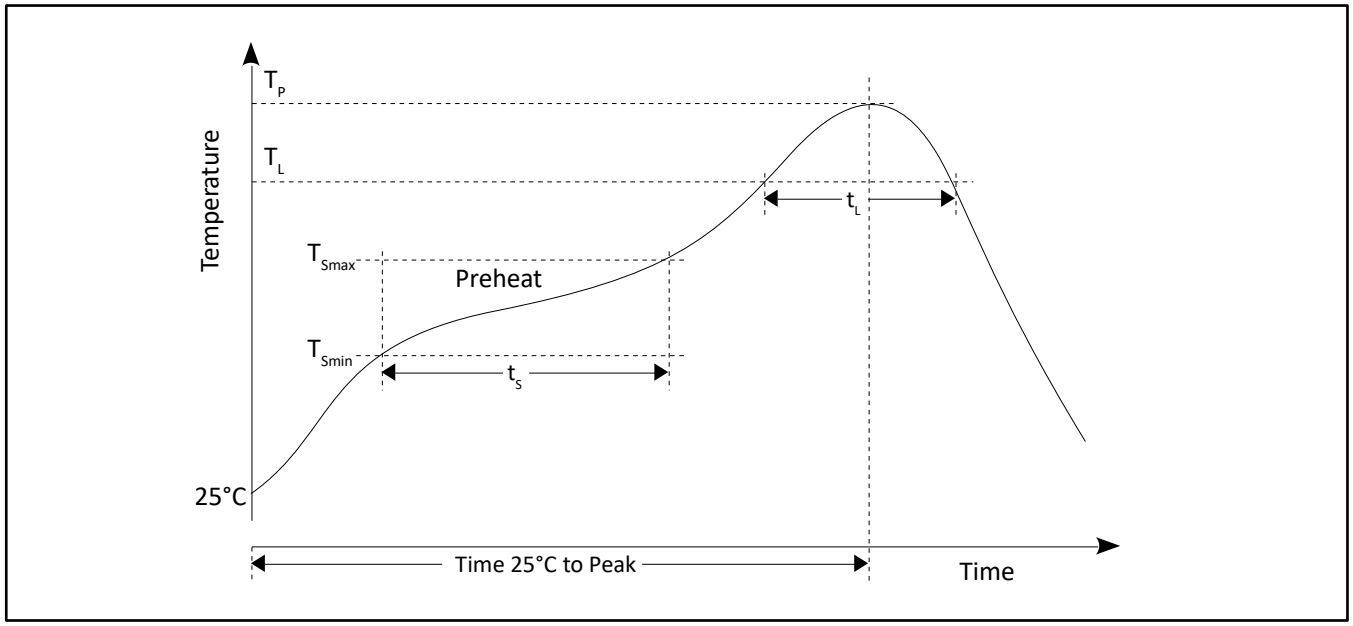


Figure 46: WLCSP reflow profile

Table 71: Reflow profile parameters

PARAMETER	DESCRIPTION	VALUE
T_{Smin}	Preheat minimum temperature	150°C
T_{Smax}	Preheat maximum temperature	200°C
t_S	Time from T_{Smin} to T_{Smax}	60-120 s
	Ramp-up rate from T_L to T_P	3°C/s max
T_L	Liquidus temperature	217°C
T_P	Peak package temperature	260°C
t_L	Time above T_L	60-150 s
	Ramp-down rate from T_P to T_L	6°C/s max
	Time 25 °C to peak temperature	8 min max

9.4 Tape and Reel Specifications

9.4.1 BOS0614 12 mm Tape Specification

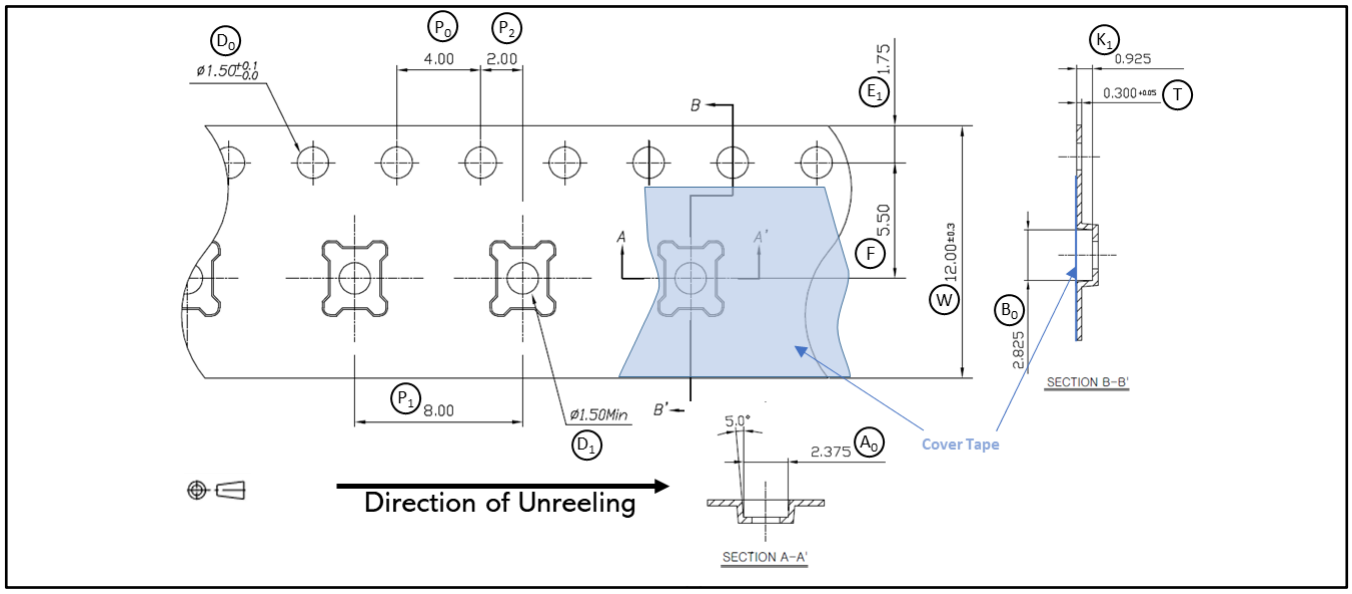


Figure 47: 12 mm embossed carrier tape dimensions (NOT TO SCALE)

Table 72: Constant dimensions for embossed 12 mm carrier tape – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE	W	Ø D_0	D_1 MIN.	E_1	P_0	P_2	T
12 mm	12.00 ± 0.30	1.5 + 0.1 - 0.0	1.50	1.75 ± 0.10	4.00 ± 0.10	2.00 ± 0.10	0.30 ± 0.05

Table 73: Variable dimensions for embossed 12 mm carrier tape – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE	W	F	P_1	A_0	B_0	K_1
12 mm	12.00 ± 0.30	5.50 ± 0.10	8.00 ± 0.10	2.375 ± 0.10	2.825 ± 0.10	0.925 ± 0.10

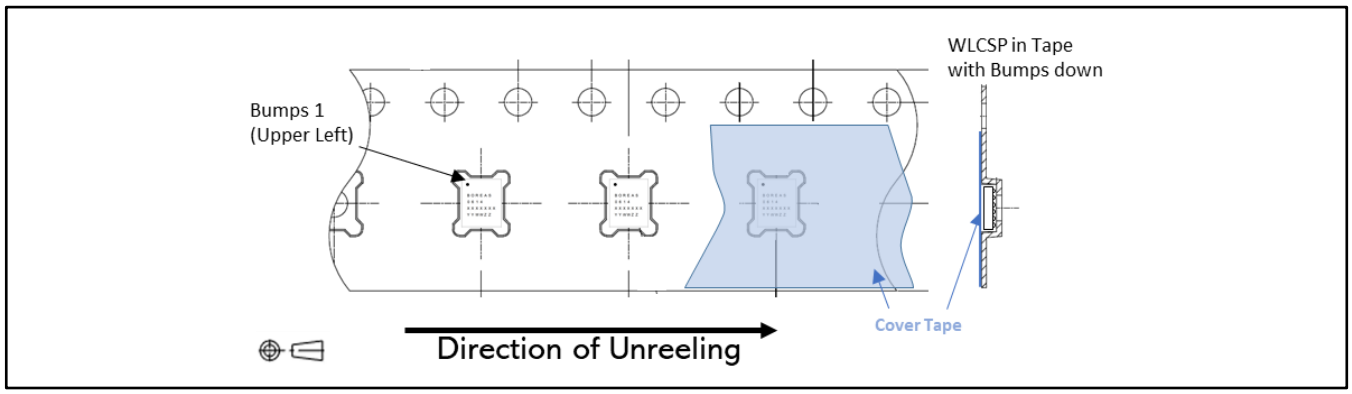


Figure 48: BOS0614 product orientation on 12 mm embossed carrier tape (NOT TO SCALE)

9.4.2 BOS0614CW 330 mm (13”) Reel Specifications (7” Hub)

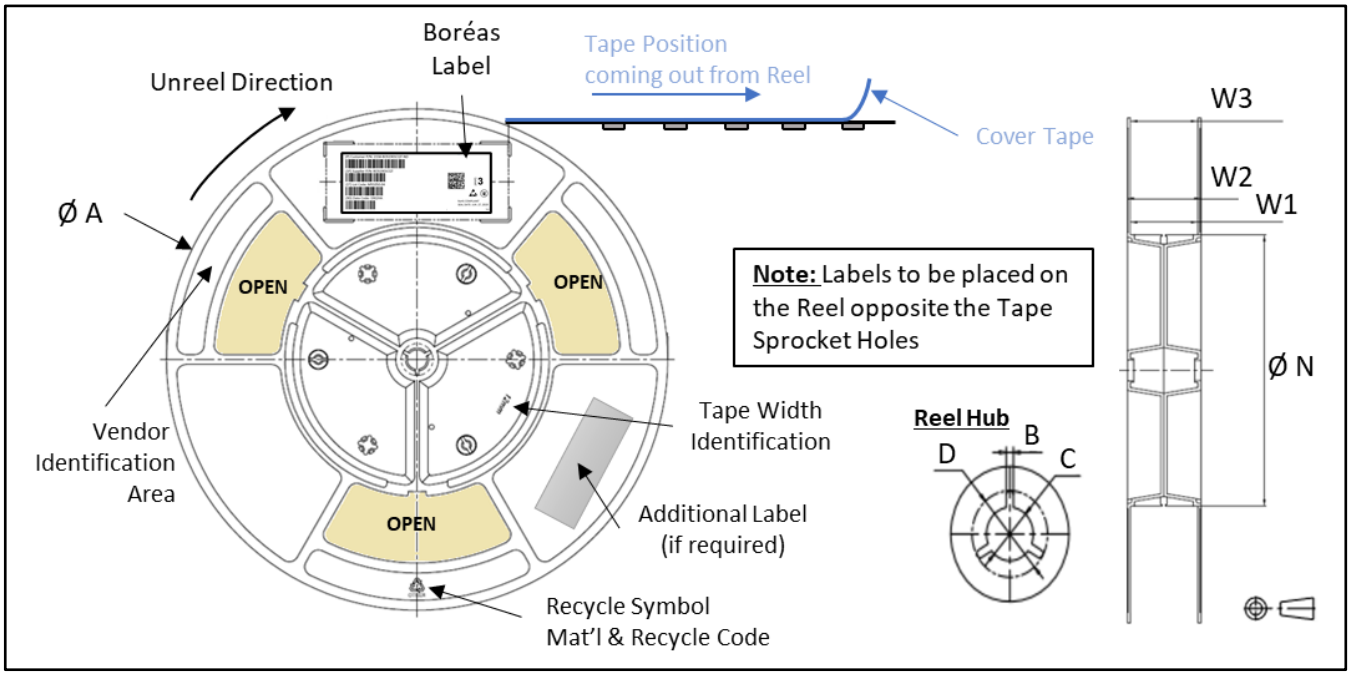


Figure 49: Reel outline drawing (NOT TO SCALE)

Table 74: Constant 330 mm (13”) reel dimensions – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE W	REEL SIZE Ø A	B MIN.	Ø C	Ø D MIN.
12.00 ± 0.30	330.0 ± 2.0 (13”)	1.5	13.0 + 0.5 - 0.2	20.2

Table 75: Variable 330 mm (13”) Reel dimensions – Reference ANSI/EIA-481 (all dimensions in mm)

TAPE SIZE W	REEL SIZE Ø A	Ø N	W_1	W_2 MAX.	W_3
12.00 ± 0.30	330.0 ± 2.0 (13”)	178 ± 2.0 (7”)	12.4 + 2.0 - 0.0	18.4	13.9

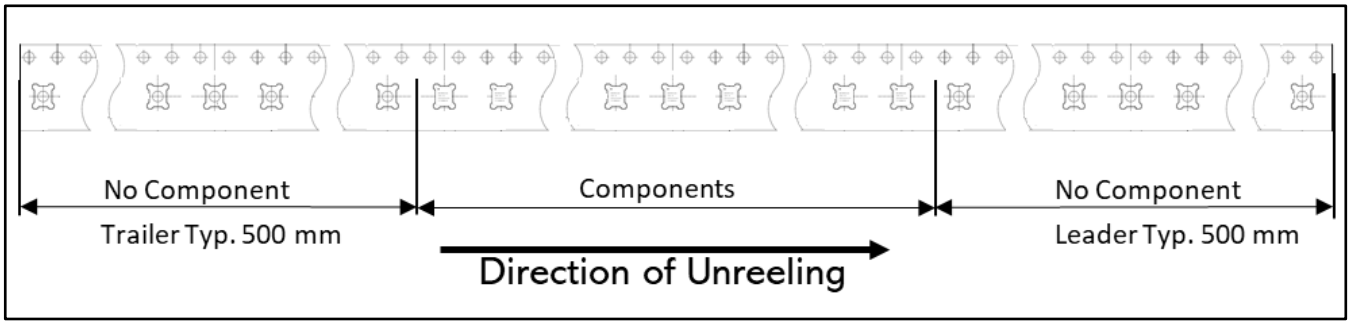


Figure 50: BOS0614 Leader/trailer and orientation on 12 mm tape.

10 Known issues

10.1 Wake-Up from SLEEP Mode

Problem Description

Once the device wakes-up from SLEEP mode by a communication on I²C/I3C bus while sensing is enabled on at least one channel (see section 6.8), it may return to SLEEP mode unexpectedly.

This issue occurs because a false ZPS event could be detected when the device wakes up from SLEEP by a communication on I²C/I3C bus, which could make the device returning into SLEEP unexpectedly.

Workaround

After waking the IC using a communication on I²C/I3C bus, the following commands should be done:

1. Wait 50 µs for the BOS0614 to reach IDLE mode.
2. Set bit OE to 0x1
3. Set bit OE to 0x0

Status

This issue applies to all devices.

10.2 Device Reset

Problem Description

After a Device Reset (bit RST set to 0x1), the device may unintentionally go back into SLEEP.

This issue occurs because a false ZPS event could be detected even though the device is not in SLEEP mode, which could make the device go into SLEEP mode.

Workaround

The Device Reset procedure should be as follow:

1. Set bit RST to 0x1 to start the software reset.
2. Wait 50 µs for the BOS0614 to reach IDLE mode
3. Set bit OE to 0x1
4. Set bit OE to 0x0

Status

This issue applies to all devices.

10.3 Calibration

Problem Description

When a sense calibration request is made (by setting SENSECONFIG.CAL to 0x1) without sensing enabled on any channel (SENSECONFIG [3:0] bits set to 0x0), the calibration can lead to incorrect results. In this situation, if a second calibration request is made, it may get stuck and the device become unusable. The calibration may be unstuck with the following sequence:

1. Set SENSECONFIG.CAL bit to 0x0.
2. Set SENSECONFIG.CH0 bit to 0x1 (or any other channel).

Workaround

To avoid the calibration issue, the sensing configuration sequence must be done as follow:

1. Set SENSECONFIG [3:0] bits to 0x1 for calibration purpose.
2. Run sensing calibration by setting bit SENSECONFIG.CAL to 0x1.
3. Wait the calibration to finish by polling SENSECONFIG.CAL. The calibration duration is approximately set by bits CONFIG.SHORT [1:0].
4. Configure the sensing conditions using registers 0x06 to 0x16.
5. Enable sensing on the desired channel using SENSECONFIG [3:0] bits.

Status

This issue applies to all devices.

11 Ordering Information

Table 76: Ordering information

	ORDERING PART NUMBER (1)	PACKAGE (2)	PACKING FORMAT	STANDARD QUANTITY (3)	MSL PEAK TEMP. (4)	DEVICE MARKING
1	BOS0614CWT	WLCSP 30B 2.1mm × 2.5mm	Cut Tape (T)	Min: 20 Max: 4000	Level 1 260 °C Unlimited	0614
2	BOS0614CWR	WLCSP 30B 2.1mm × 2.5mm	Tape & Reel (R)	5000 / Reel	Level 1 260 °C Unlimited	0614

NOTE

(1) Ordering Part Number where last letter indicates packing format.
(2) All parts are RoHS compliant.
(3) Contact sales@boreas.ca to order.
(4) MSL: Moisture Sensitivity Levels, IPC/JEDEC J-STD-020.

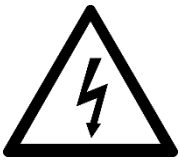
12 Document History

Table 77: Document Changes

ISSUE	DATE	DOCUMENT NUMBER	CHANGES
4	April 2022	BT005EDS01.01	Product Datasheet Added Typical Performance Characteristics (section 5.5) Clarified the WFS Command Interpreter description (section 6.10) WFS Command names changed (section 6.10) Device package branding changed (section 9.1)
3	January 2022	BT005DDS01.01	Preliminary Datasheet Changed C_{HV2} from optional to recommended (section 7.2) Added details to SLEEP mode (section 6.2.5) Added details to Device Reset procedure (section 6.2.6) Added details to Input Trigger section (section 6.2.10) Added typical sensing configuration (section 6.8.1) Register SENSERAWx removed (section 6.9) Device package branding (section 9.1) Added Known Issues section (section 10)

13 Notice and Warning

Warning High Voltage



For safety, this integrated circuit must be used by qualified and skilled personnel familiar with all applicable safety standards.

ESD Caution

This integrated circuit is ESD (Electrostatic Discharge) sensitive. Therefore, proper ESD precautions and procedures are recommended for handling and installation to avoid damage.

Boréas Technologies Datasheet Status:

Advance Information Datasheet:	Design Data
Preliminary Information Datasheet:	Prototype information
Final Datasheet:	Production information