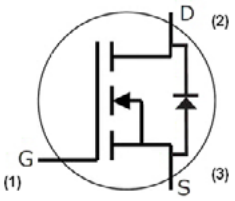
C3M0025065D

Silicon Carbide Power MOSFET
C3M™ MOSFET Technology
N-Channel Enhancement Mode

Halogen-Free

RoHS compliant



Features

- 3rd Generation SiC MOSFET technology
- High blocking voltage with low on-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

Part Number	Package	Marking
C3M0025065D	TO 247-3	C3M0025065D

Typical Applications

- EV chargers
- UPS
- Solar inverters
- Industrial SMPS
- DC/DC converters

Benefits

- Higher system efficiency
- Reduced cooling requirements
- Increased power density
- Increased system switching frequency
- Easy to parallel and simple to drive
- Enable new hard switching PFC topologies (Totem-Pole)

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			650	V	T_C = 25°C	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS\,op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			97	A	V_{GS} = 15 V, T_C = 25 °C, T_J ≤175 °C	Fig. 19 Note 2
				70		V_{GS} = 15 V, T_C = 100 °C, T_J ≤175 °C	
Pulsed Drain Current	I_{DM}			251		t_{Pmax} limited by T_{jmax} V_{GS} = 15V, T_C = 25 °C	Fig. 22
Power Dissipation	P_D			326	W	T_C = 25 °C, T_J = 175 °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-40 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	
Mounting Torque	M_D			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

Electrical Characteristics (T_C = 25℃ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	650	—	—	V	V_{GS} = 0 V, I_D = 100 µA	
Gate-Source Recommended Turn-On Voltage	$V_{GS(on)}$	—	15	—	V	Static	Fig. 29
Gate-Source Recommended Turn-Off Voltage	$V_{GS(off)}$	—	-4	—	V	Static	Fig. 29
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.3	3.6	V	V_{DS} = V_{GS}, I_D = 9.22 mA	Fig. 11
		—	1.9	—	V	V_{DS} = V_{GS}, I_D = 9.22 mA, T_J = 175°C	Fig. 11
Zero Gate Voltage Drain Current	I_{DSS}	—	1	50	µA	V_{DS} = 650 V, V_{GS} = 0 V	
Gate-Source Leakage Current	I_{GSS}	—	10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
Drain-Source On-State Resistance	$R_{DS(on)}$	—	25	34	mΩ	V_{GS} = 15 V, I_D = 33.5 A	Fig. 4, 5, 6
		—	33	—	mΩ	V_{GS} = 15 V, I_D = 33.5 A, T_J = 175°C	Fig. 4, 5, 6
Transconductance	g_{fs}	—	25	—	S	V_{GS} = 20 V, I_{DS} = 33.5 A	Fig. 7
			24		S	V_{GS} = 20 V, I_{DS} = 33.5 A, T_J = 175°C	Fig. 7
Input Capacitance	C_{iss}	—	2980	—	pF	V_{GS} = 0 V, V_{DS} = 0 V to 600 V f = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
Output Capacitance	C_{oss}	—	178	—	pF	V_{GS} = 0 V, V_{DS} = 0 V to 600 V f = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
Reverse Transfer Capacitance	C_{rss}	—	12	—	pF	V_{GS} = 0 V, V_{DS} = 0 V to 600 V f = 1 Mhz V_{AC} = 25 mV	Fig. 17, 18
Effective Output Capacitance (Energy Related)[1]	$C_{o(er)}$	—	236	—	pF	V_{GS} = 0 V, V_{DS} = 0 V to 400 V	
Effective Output Capacitance (Time Related)[2]	$C_{o(tr)}$	—	340	—	pF	V_{GS} = 0 V, V_{DS} = 0 V to 400 V	
C_{oss} Stored Energy	E_{oss}	—	37	—	µJ	V_{DS} = 600 V, f = 1 Mhz	Fig. 16
Turn-On Switching Energy (Body Diode)	E_{on}	—	578	—	µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 33.5 A, $R_{G(ext)}$ = 2.5 Ω, L=59 µH, T_J = 175°C FWD = Internal Body Diode of MOSFET	Fig. 25
Turn-Off Switching Energy (Body Diode)	E_{off}	—	214	—	µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 33.5 A, $R_{G(ext)}$ = 2.5 Ω, L=59 µH, T_J = 175°C FWD = Internal Body Diode of MOSFET	Fig. 25
Turn-On Switching Energy (External Diode)	E_{on}	—	392	—	µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 33.5 A, $R_{G(ext)}$ = 2.5 Ω, L=59 µH, T_J = 175°C FWD = External SiC DIODE	Fig. 25
Turn-Off Switching Energy (External Diode)	E_{off}	—	238	—	µJ	V_{DS} = 400 V, V_{GS} = -4 V/15 V, I_D = 33.5 A, $R_{G(ext)}$ = 2.5 Ω, L=59 µH, T_J = 175°C FWD = External SiC DIODE	Fig. 25
Turn-On Delay Time	$t_{d(on)}$	—	14	—	ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 33.5 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 26
Rise Time	t_r	—	60	—	ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 33.5 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 26
Turn-Off Delay Time	$t_{d(off)}$	—	27	—	ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 33.5 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 26
Fall Time	t_f	—	12	—	ns	V_{DD} = 400 V, V_{GS} = -4 V/15 V I_D = 33.5 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 26
Internal Gate Resistance	$R_{G(int)}$	—	1.3	—	Ω	f = 1 MHz, V_{AC} = 25 mV	
Gate to Source Charge	Q_{gs}	—	29	—	nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 33.5 A Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	Q_{gd}	—	37	—	nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 33.5 A Per IEC60747-8-4 pg 21	Fig. 12
Total Gate Charge	Q_g	—	108	—	nC	V_{DS} = 400 V, V_{GS} = -4 V/15 V I_D = 33.5 A Per IEC60747-8-4 pg 21	Fig. 12

Note:
[1] $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 V to 400 V
[2] $C_{o(tr)}$, a lumped capacitance that gives same stored energy as C_{oss} while V_{DS} is rising from 0 V to 400 V

Reverse Diode Characteristics (T_C = 25°C unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Notes
Diode Forward Voltage	V_{SD}	5.0	—	V	V_{GS} = -4 V, I_{SD} = 16.8 A, T_J = 25°C	Fig. 8, 9, 10
		4.5	—		V_{GS} = -4 V, I_{SD} = 16.8 A, T_J = 175°C	
Continuous Diode Forward Current	I_S	—	52	A	V_{GS} = -4 V, T_C = 25°C	
Diode Pulse Current	I_{SM}	—	251		V_{GS} = -4 V, pulse width t_P limited by $T_{j\,max}$	
Reverse Recovery Time	t_{rr}	33	—	ns	V_{GS} = -4 V, I_{SD} = 33.5 A, V_R = 400 V di_F/dt = 745 A/µs, T_J = 175°C	
Reverse Recovery Charge	Q_{rr}	309	—	nC		
Peak Reverse Recovery Current	I_{RRM}	17	—	A		
Reverse Recovery Time	t_{rr}	51	—	ns	V_{GS} = -4 V, I_{SD} = 33.5 A, V_R = 400 V di_F/dt = 685 A/µs, T_J = 175°C	
Reverse Recovery Charge	Q_{rr}	261	—	nC		
Peak Reverse Recovery Current	I_{RRM}	12	—	A		

Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Test Conditions	Note
Thermal Resistance from Junction to Case	$R_{\theta JC}$	0.46	°C/W		Fig. 21
Thermal Resistance From Junction to Ambient	$R_{\theta JA}$	40			

Typical Performance

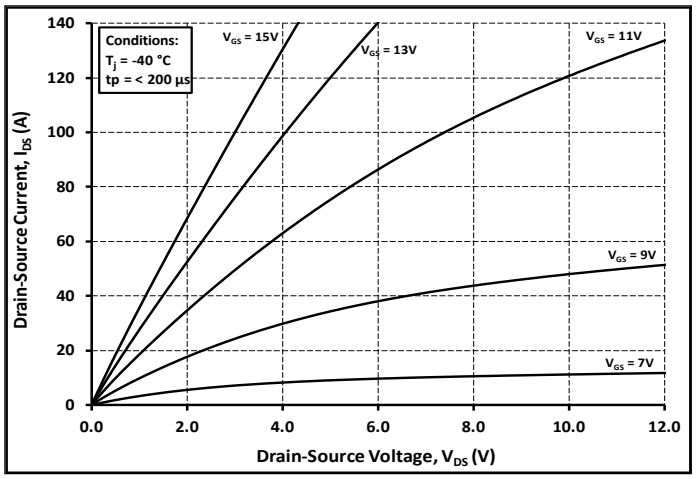


Figure 1. Output Characteristics T_J = -40°C

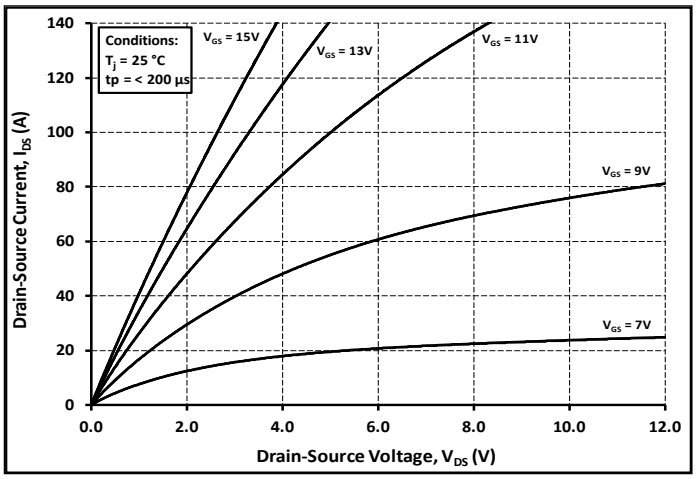


Figure 2. Output Characteristics T_J = 25°C

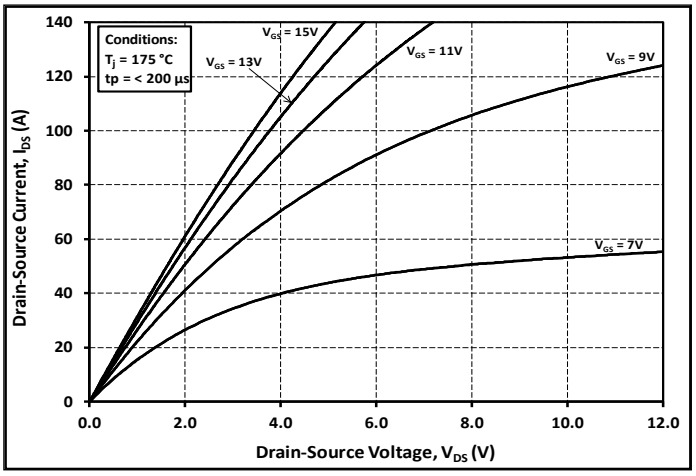


Figure 3. Output Characteristics T_J = 175°C

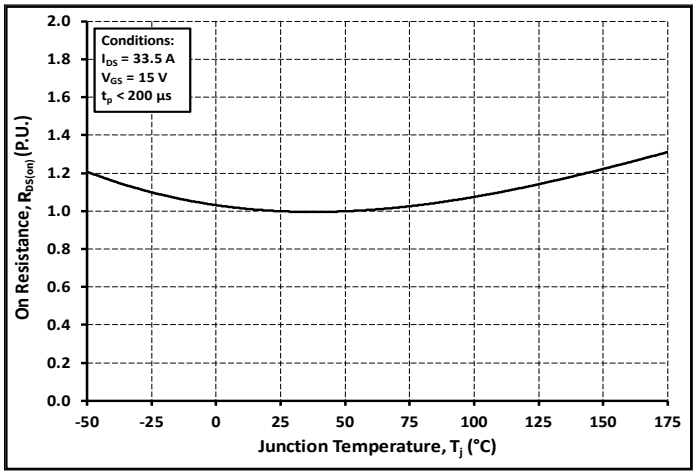


Figure 4. Normalized On-Resistance vs. Temperature

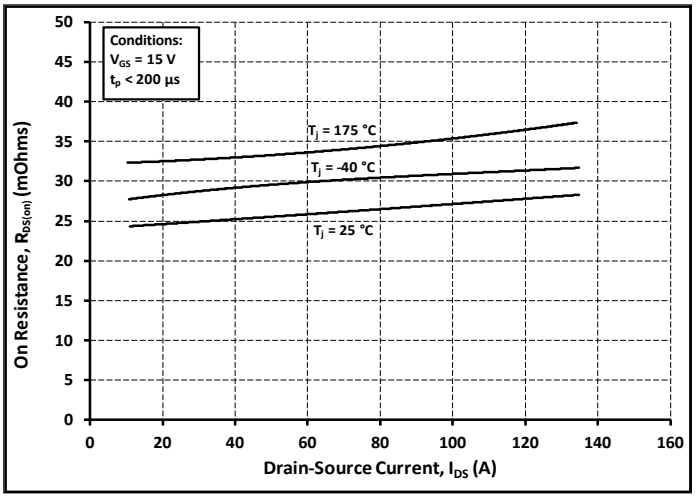


Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

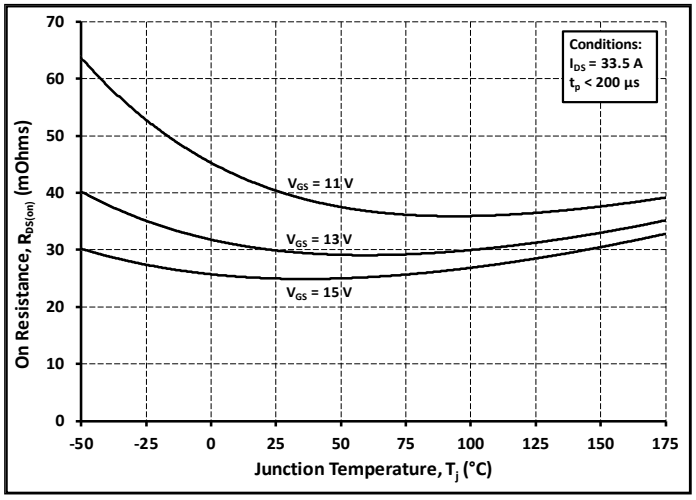


Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

Typical Performance

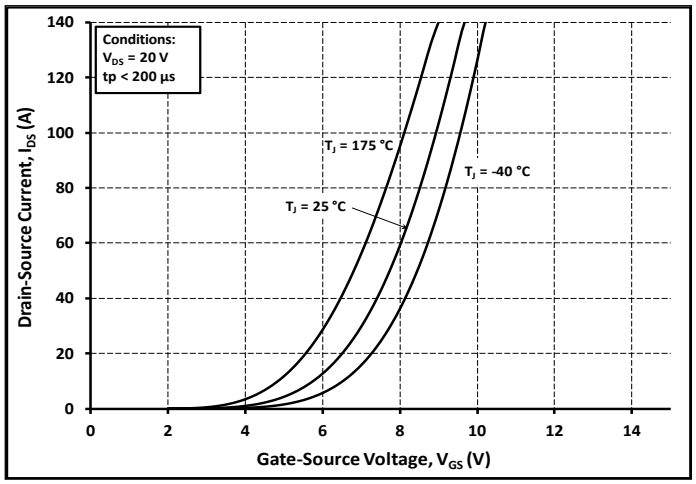


Figure 7. Transfer Characteristic for Various Junction Temperatures

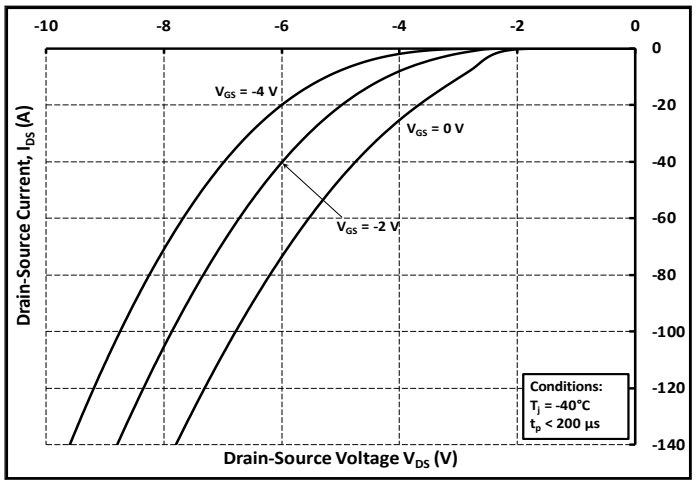


Figure 8. Body Diode Characteristic at -40°C

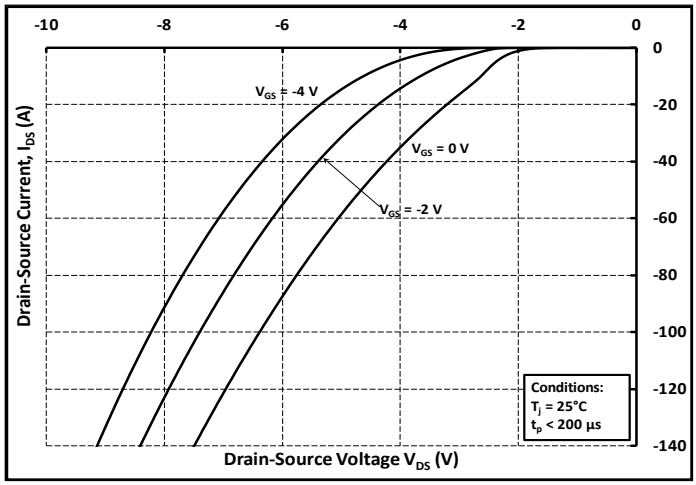


Figure 9. Body Diode Characteristic at 25°C

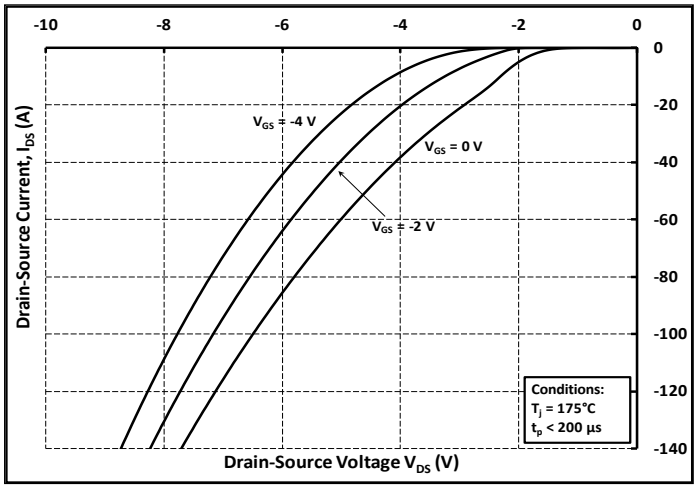


Figure 10. Body Diode Characteristic at 175°C

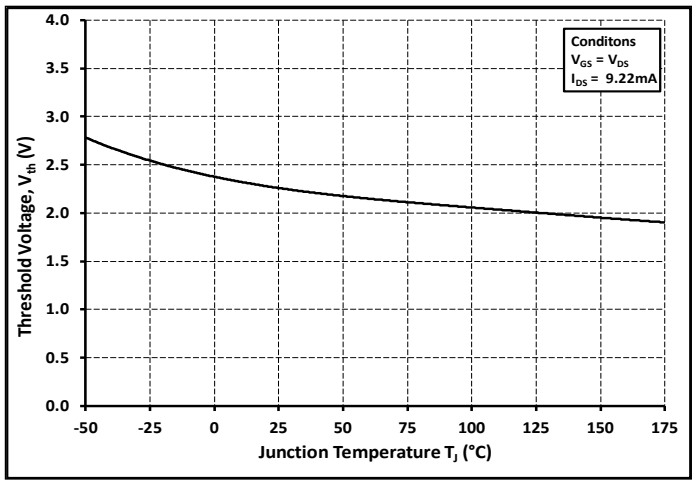


Figure 11. Threshold Voltage vs. Temperature

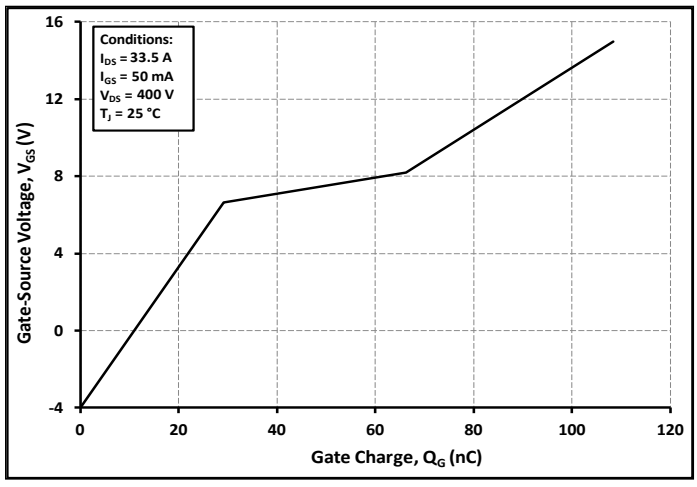


Figure 12. Gate Charge Characteristics

Typical Performance

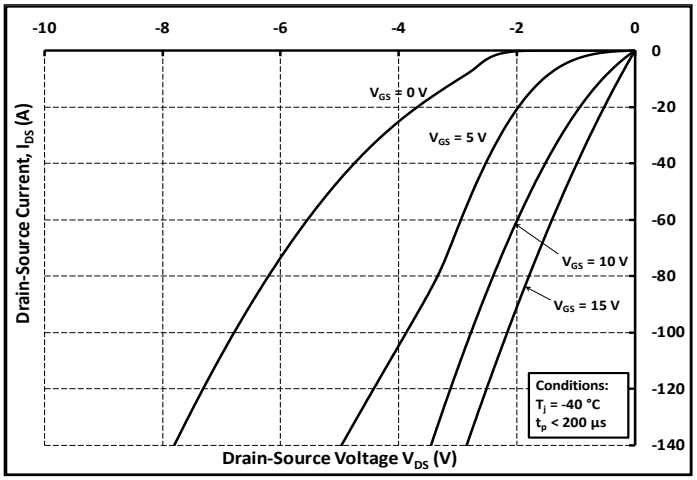


Figure 13. 3rd Quadrant Characteristic at -40°C

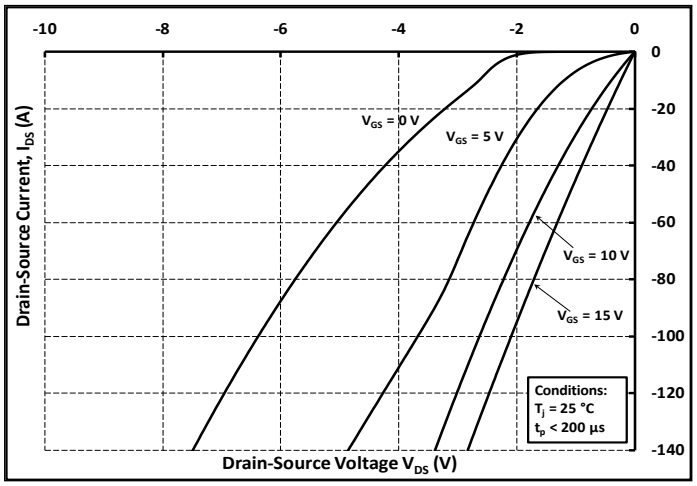


Figure 14. 3rd Quadrant Characteristic at 25°C

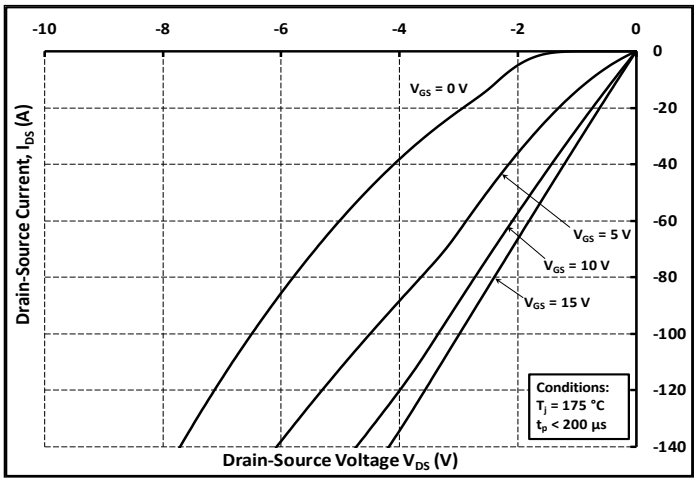


Figure 15. 3rd Quadrant Characteristic at 175°C

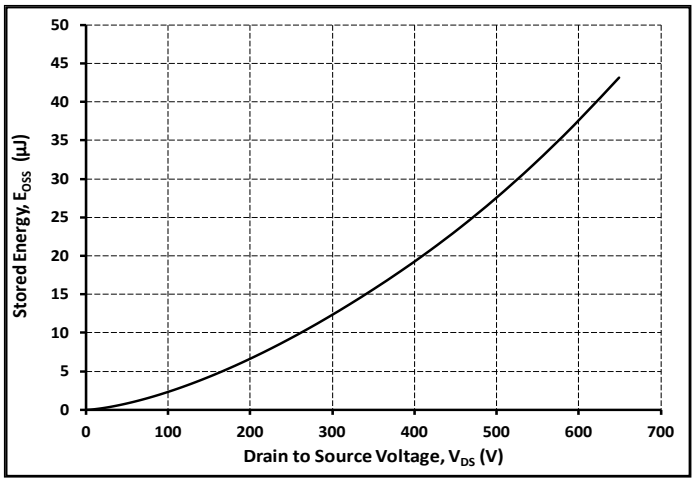


Figure 16. Output Capacitor Stored Energy

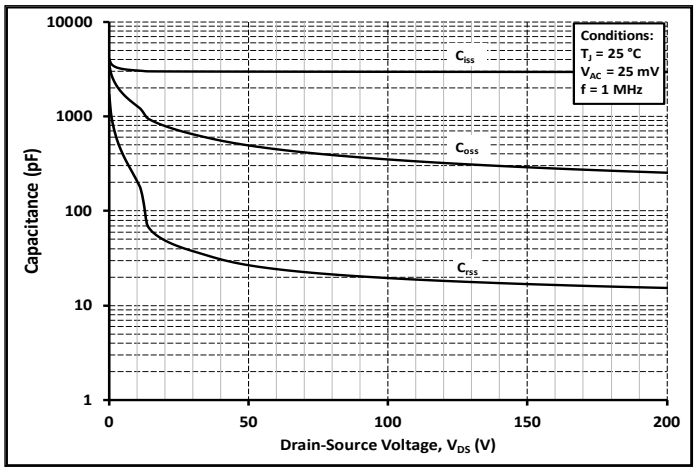


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200 V)

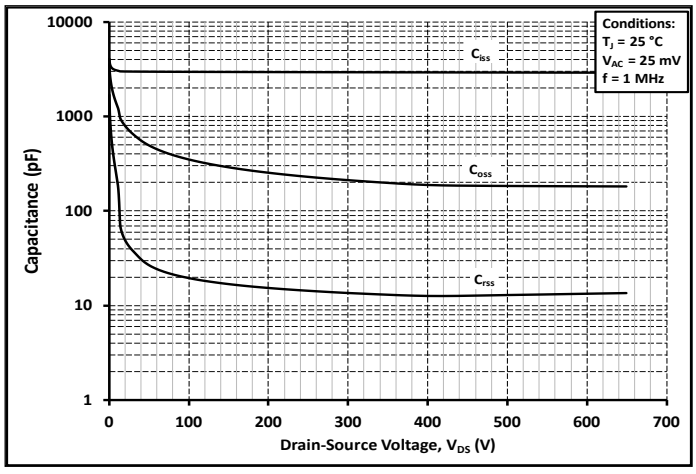


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 650 V)

Typical Performance

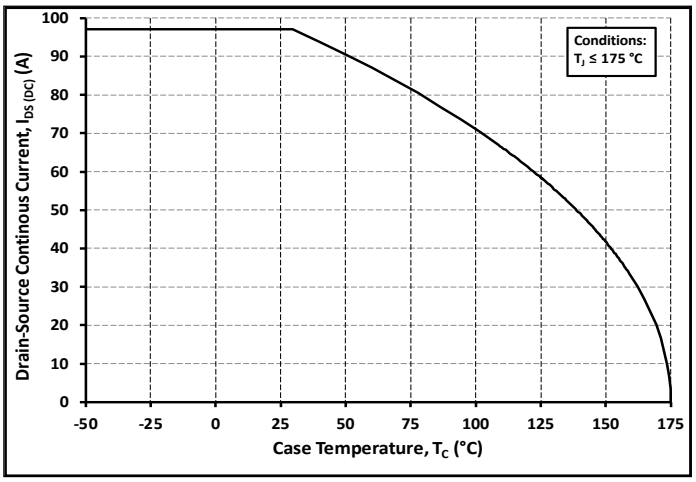


Figure 19. Continuous Drain Current Derating vs. Case Temperature

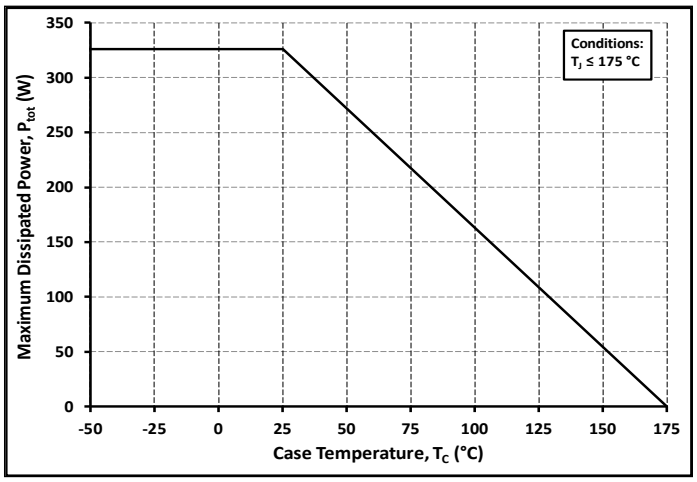


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

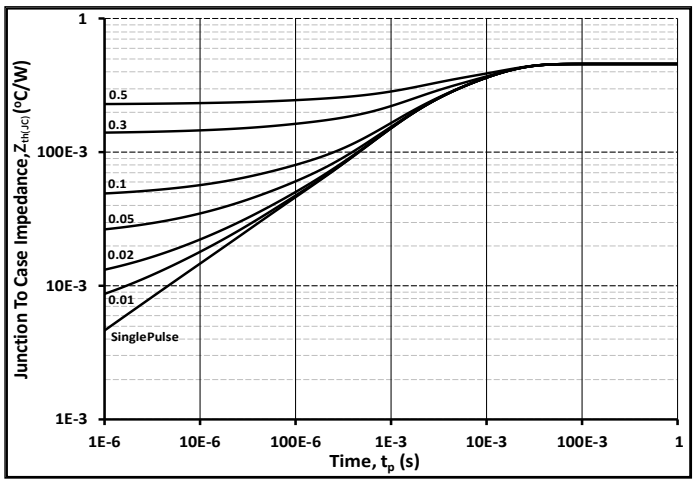


Figure 21. Transient Thermal Impedance (Junction - Case)

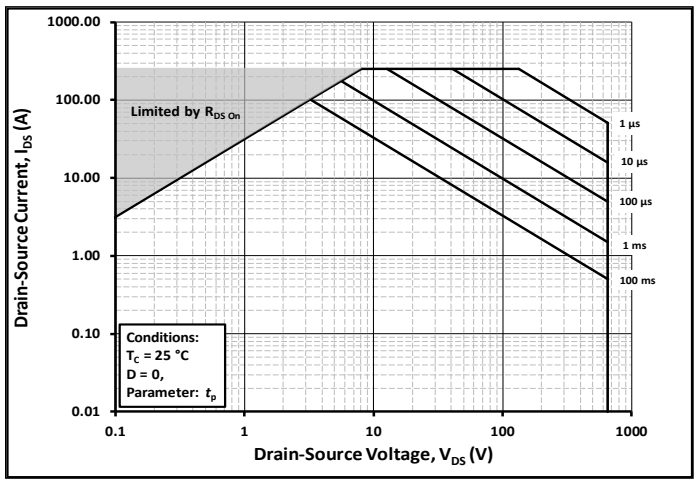


Figure 22. Safe Operating Area

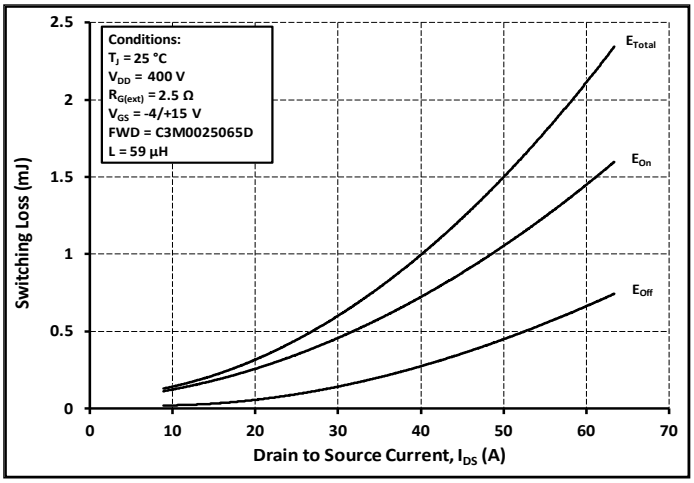


Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 400 V)

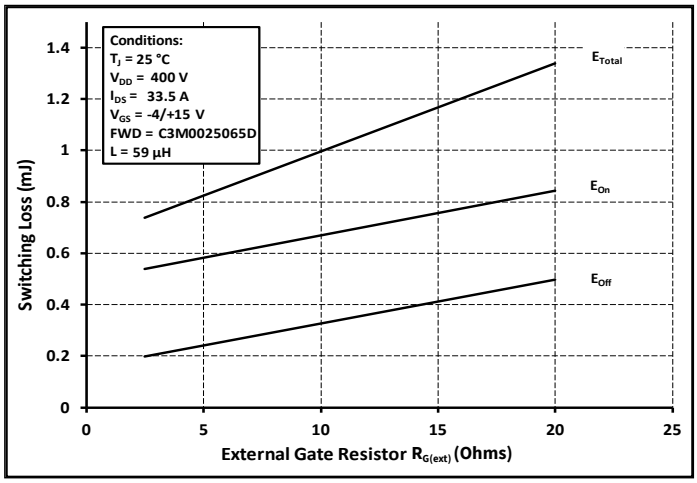


Figure 24. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

Typical Performance

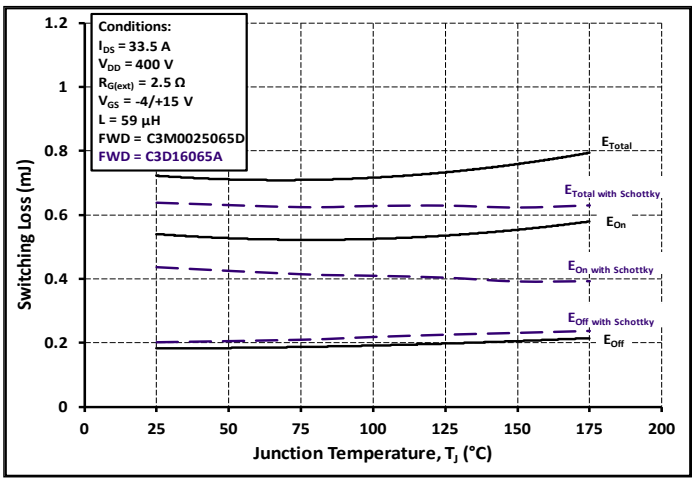


Figure 25. Clamped Inductive Switching Energy vs. Temperature

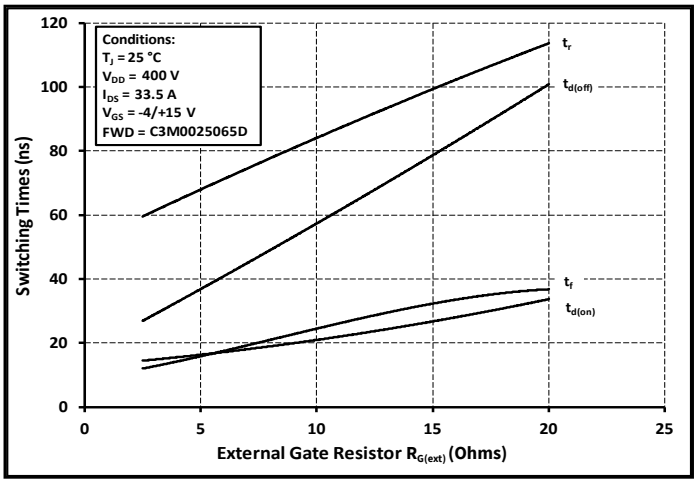


Figure 26. Switching Times vs. $R_{G(ext)}$

Test Circuit Schematic

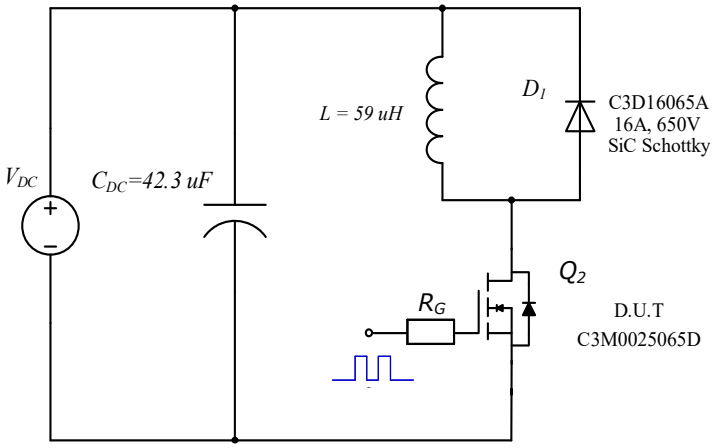


Figure 27. Clamped Inductive Switching Waveform Test Circuit

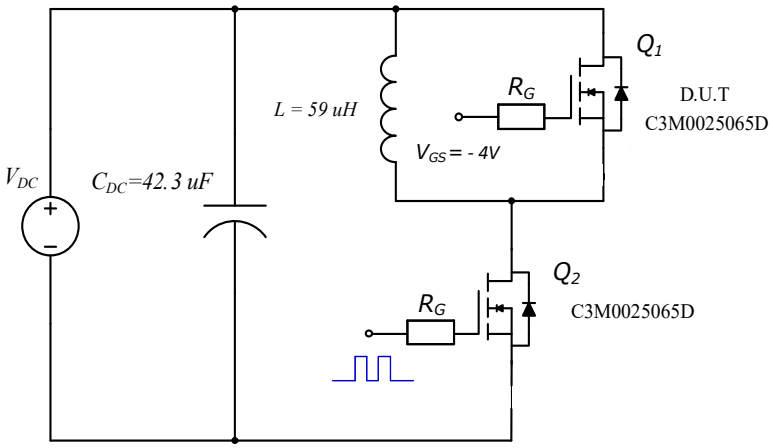
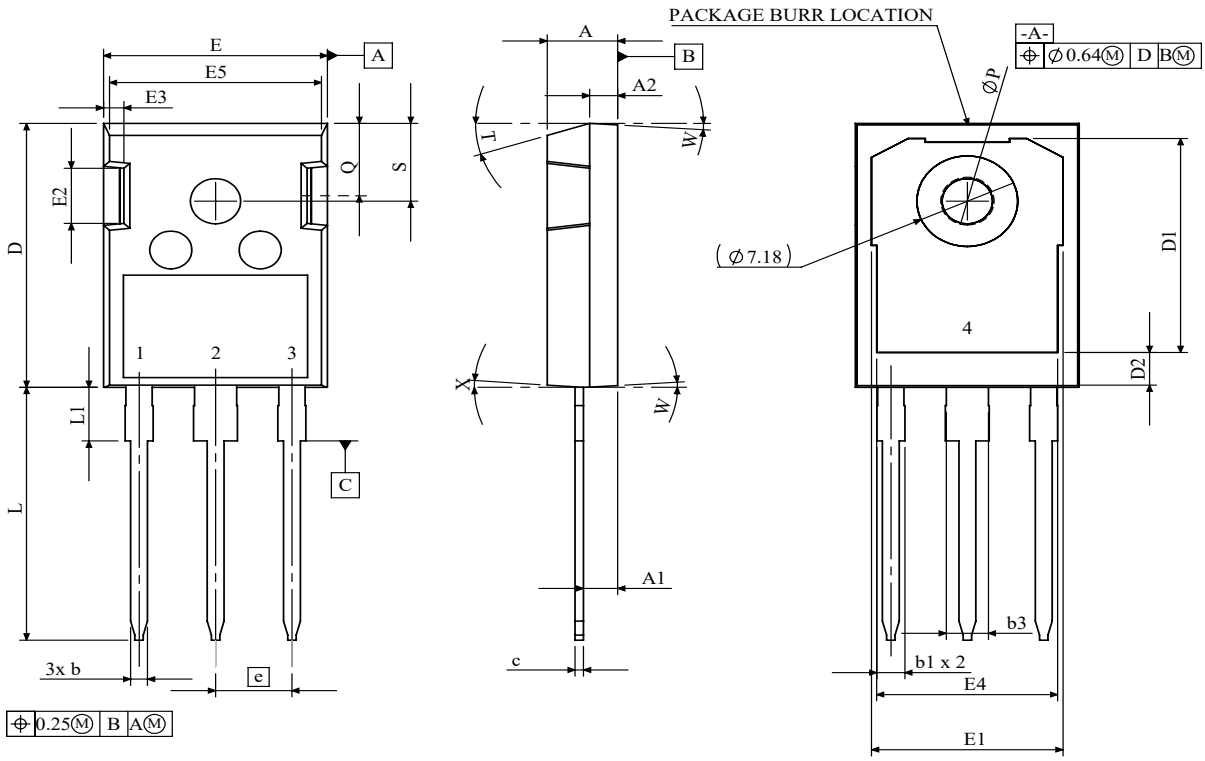


Figure 28. Body Diode Recovery Test Circuit

Package Dimensions – TO-247-4L



SYMBOL	MIN (mm)	MAX (mm)
A	4.83	5.21
A1	2.27	2.52
A2	1.91	2.16
b	1.07	1.33
b1	1.91	2.41
b3	2.87	3.38
c	0.55	0.74
D	20.75	21.05
D1	16	17.4
D2	2.86	3.26
E	15.75	16.13
E1	13.5	14.55
E2	3.68	5.1
E3	1	1.9
E4	12.38	13.43
E5	14.65	15.05
e	5.44 BSC	
L	19.73	20.48
L1	3.97	4.69
ØP	3.18	4.06
Q	5.42	5.96
S	5.85	6.49
T	17.5° REF.	
W	3.5° REF.	
X	4° REF.	

1	GATE
2	DRAIN
3	SOURCE
4	DRAIN

NOTES:
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. BURR OR MOLD FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

Wolfspeed

TITLE: PACKAGE OUTLINE DRAWING: TO-247-3L(MOSFET)

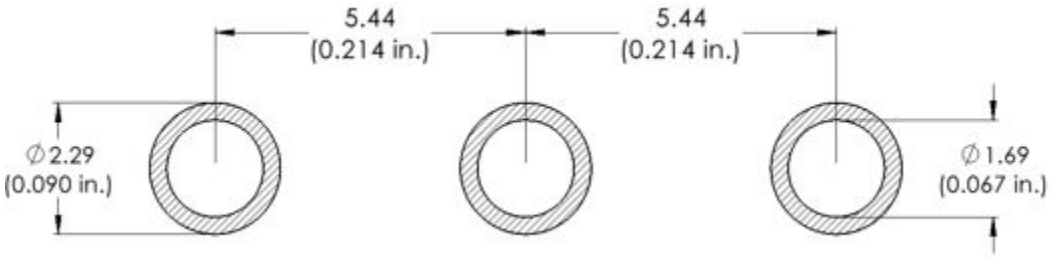
Date: 3/4/24

REVISION NO. 02

A4

PRD 05964 SCALE:1:1 SHEET 1 OF 1

Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
1	December-2020	N/A
2	November-2023	Not Released
3	December-2023	Updated Wolfspeed branding, package drawing, package image, and solder pad layout, added Revision History Table, Revised Table 1 Layout
4	September - 2024	Legal Disclaimer, POD, Diode Pulse Current Symbol

Related Links

- SPICE Models: http://wolfspeed.com/power/tools-and-support
- SiC MOSFET Isolated Gate Driver Reference Design: http://wolfspeed.com/power/tools-and-support
- SiC MOSFET Evaluation Board: http://wolfspeed.com/power/tools-and-support

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