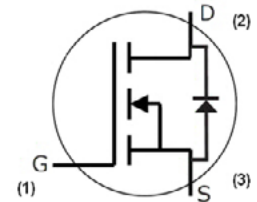


# C3M0032120D

## Silicon Carbide Power MOSFET C3M™ MOSFET Technology N-Channel Enhancement Mode

### Features

- 3rd generation SiC MOSFET technology
- High blocking voltage with low On-resistance
- High speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ( $Q_{rr}$ )
- Halogen free, RoHS compliant



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Part Number	Package	Marking
C3M0032120D	TO 247-3	C3M0032120D

### Typical Applications

- Solar inverters
- EV motor drive
- High voltage DC/DC converters
- Switched mode power supplies

### Benefits

- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

### Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	$V_{DS}$			1200	V	$T_c = 25^\circ\text{C}$	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS op}$		-4/15			Static	Note 1
DC Continuous Drain Current	$I_D$			63	A	$V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Fig. 19
				48		$V_{GS} = 15\text{ V}, T_c = 100^\circ\text{C}, T_J \leq 175^\circ\text{C}$	Note 2
Pulsed Drain Current	$I_{DM}$			120		$t_{Pmax}$ limited by $T_{Jmax}$ $V_{GS} = 15\text{ V}, T_c = 25^\circ\text{C}$	Fig. 22
Power Dissipation	$P_D$			283	W	$T_c = 25^\circ\text{C}, T_J = 175^\circ\text{C}$	Fig. 20
Operating Junction and Storage Temperature	$T_J, T_{stg}$			-40 to +175	$^\circ\text{C}$		
Solder Temperature	$T_L$			260		According to JEDEC J-STD-020	
Mounting Torque	$M_D$			1 8.8	Nm lbf-in	M3 or 6-32 screw	

Note (1): Recommended turn-on gate voltage is 15V with  $\pm 5\%$  regulation tolerance, see Application Note PRD-04814 for additional details

Note (2): Verified by design


**Electrical Characteristics** ( $T_c = 25^\circ\text{C}$  unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	Note
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1200	—	—	V	$V_{GS} = 0\text{ V}, I_D = 100\text{ }\mu\text{A}$	Fig. 11
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.5	3.6		$V_{DS} = V_{GS}, I_D = 11.5\text{ mA}$	
		—	2.0	—		$V_{DS} = V_{GS}, I_D = 11.5\text{ mA}, T_J = 175^\circ\text{C}$	
Zero Gate Voltage Drain Current	$I_{DSS}$	—	1	50	$\mu\text{A}$	$V_{DS} = 1200\text{ V}, V_{GS} = 0\text{ V}$	
Gate-Source Leakage Current	$I_{GSS}$	—	10	250	nA	$V_{GS} = 15\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	23	32	43	m $\Omega$	$V_{GS} = 15\text{ V}, I_D = 40\text{ A}$	Fig. 4, 5, 6
		—	57.6	—		$V_{GS} = 15\text{ V}, I_D = 40\text{ A}, T_J = 175^\circ\text{C}$	
Transconductance	$g_{fs}$	—	27	—	S	$V_{DS} = 20\text{ V}, I_{DS} = 40\text{ A}$	Fig. 7
			22			$V_{DS} = 20\text{ V}, I_{DS} = 40\text{ A}, T_J = 175^\circ\text{C}$	
Input Capacitance	$C_{iss}$	—	3357	—	pF	$V_{GS} = 0\text{ V},$ $V_{DS} = 1000\text{ V}$ $f = 100\text{ kHz}$ $V_{AC} = 25\text{ mV}$	Fig. 17, 18
Output Capacitance	$C_{oss}$	—	129	—			
Reverse Transfer Capacitance	$C_{rss}$	—	8	—			
$C_{oss}$ Stored Energy	$E_{oss}$	—	76	—	$\mu\text{J}$		Fig. 16
Turn-On Switching Energy (SiC Diode FWD)	$E_{on}$	—	1.94	—	mJ	$V_{DS} = 800\text{ V}, V_{GS} = -4/+15\text{ V}, I_D = 40\text{ A},$ $R_{G(ext)} = 5\text{ }\Omega, L = 157\text{ }\mu\text{H}, T_J = 175^\circ\text{C}$	Fig. 26
Turn Off Switching Energy (SiC Diode FWD)	$E_{off}$	—	0.79	—			
Turn-On Switching Energy (Body Diode FWD)	$E_{on}$	—	3.10	—			
Turn Off Switching Energy (Body Diode FWD)	$E_{off}$	—	0.72	—			
Turn-On Delay Time	$t_{d(on)}$	—	107	—	ns	$V_{DS} = 800\text{ V}, V_{GS} = -4/15\text{ V}$ $R_{G(ext)} = 5\text{ }\Omega, I_D = 40\text{ A}, L = 157$ Timing relative to $V_{DS}$ , Inductive load	Fig. 27
Rise Time	$t_r$	—	22	—			
Turn-Off Delay Time	$t_{d(off)}$	—	39	—			
Fall Time	$t_f$	—	19	—			
Internal Gate Resistance	$R_{G(int)}$	—	1.7	—	$\Omega$	$f = 1\text{ MHz}, V_{AC} = 25\text{ mV}$	
Gate to Source Charge	$Q_{gs}$	—	35	—	nC	$V_{DS} = 800\text{ V}, V_{GS} = -4\text{ V}/15\text{ V}$ $I_D = 40\text{ A}$ Per IEC60747-8-4 pg 21	Fig. 12
Gate to Drain Charge	$Q_{gd}$	—	40	—			
Total Gate Charge	$Q_g$	—	114	—			

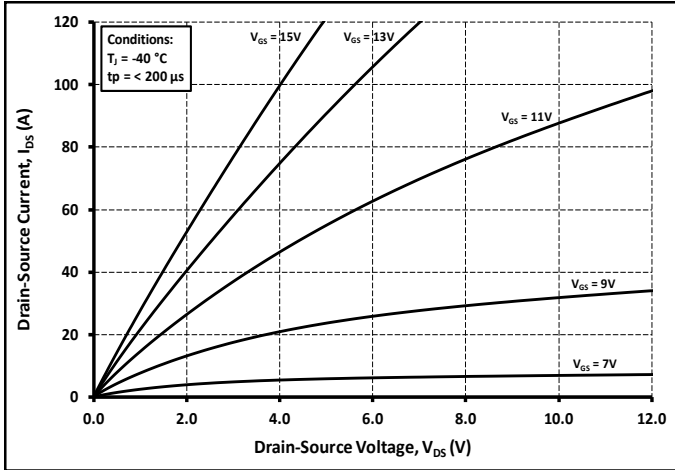
Reverse Diode Characteristics (T<sub>c</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Typ.	Max.	Unit	Test Conditions	Note
Diode Forward Voltage	V <sub>SD</sub>	4.6	—	V	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 20 A, T <sub>J</sub> = 25°C	Fig. 8, 9, 10
		4.2	—		V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 20 A, T <sub>J</sub> = 175°C	
Continuous Diode Forward Current	I <sub>S</sub>	—	62	A	V <sub>GS</sub> = -4 V, T <sub>c</sub> = 25°C	
Diode Pulse Current	I <sub>SM</sub>	—	120		V <sub>GS</sub> = -4 V, T <sub>c</sub> = 25°C, pulse width limited by T <sub>jmax</sub>	
Reverse Recover Time	t <sub>rr</sub>	69	—	nS	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 40 A, V <sub>R</sub> = 800 V di <sub>F</sub> /dt = 1500 A/μs, T <sub>J</sub> = 175°C	
Reverse Recovery Charge	Q <sub>rr</sub>	848	—	nC		
Peak Reverse Recovery Current	I <sub>rrm</sub>	19	—	A		

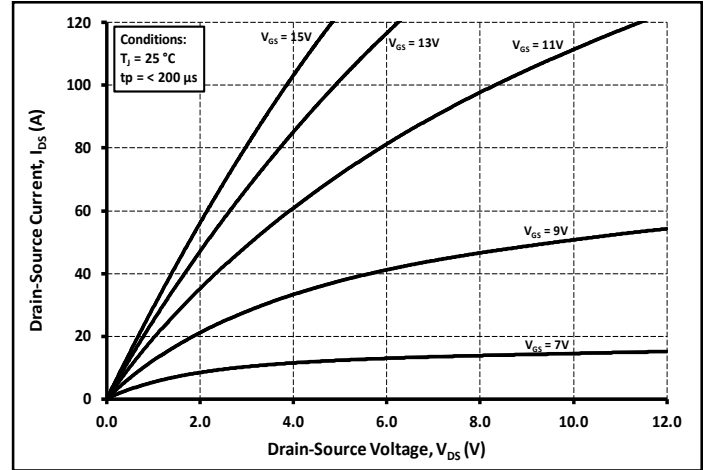
Thermal Characteristics

Parameter	Symbol	Typ.	Unit	Note
Thermal Resistance from Junction to Case	R <sub>θJC</sub>	0.45	°C/W	Fig. 21
Thermal Resistance from Junction to Ambient	R <sub>θJA</sub>	40		

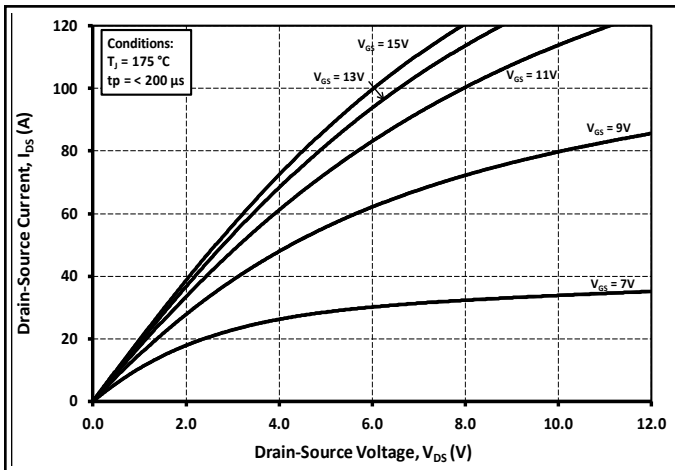
## Typical Performance



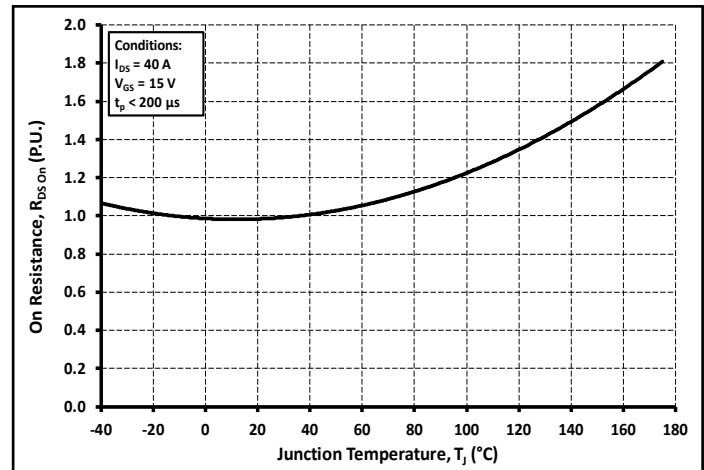
**Figure 1.** Output Characteristics  $T_j = -40^\circ\text{C}$



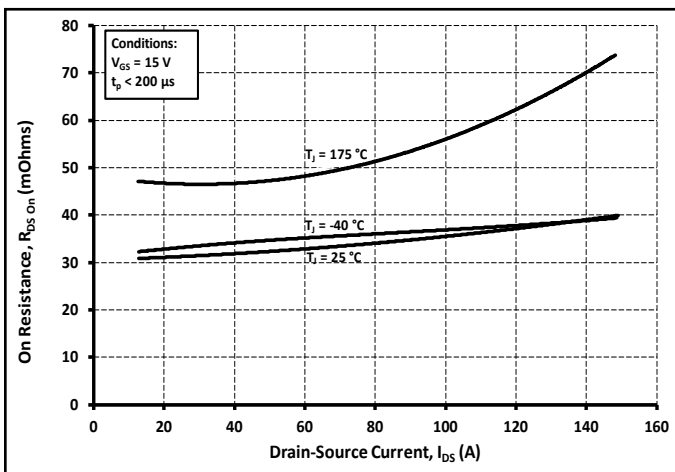
**Figure 2.** Output Characteristics  $T_j = 25^\circ\text{C}$



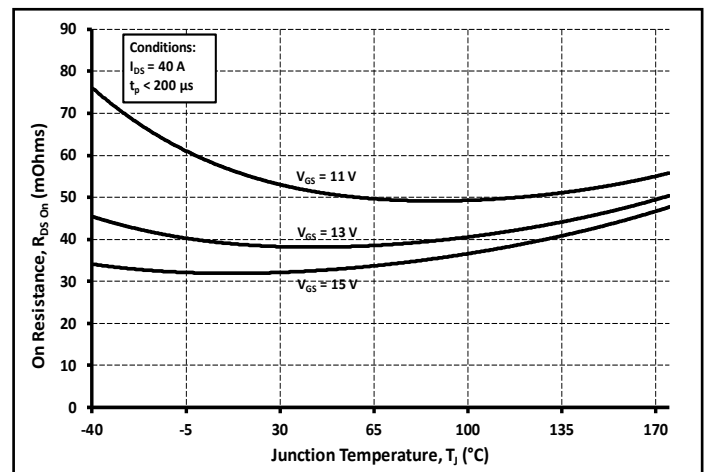
**Figure 3.** Output Characteristics  $T_j = 175^\circ\text{C}$



**Figure 4.** Normalized On-Resistance vs. Temperature

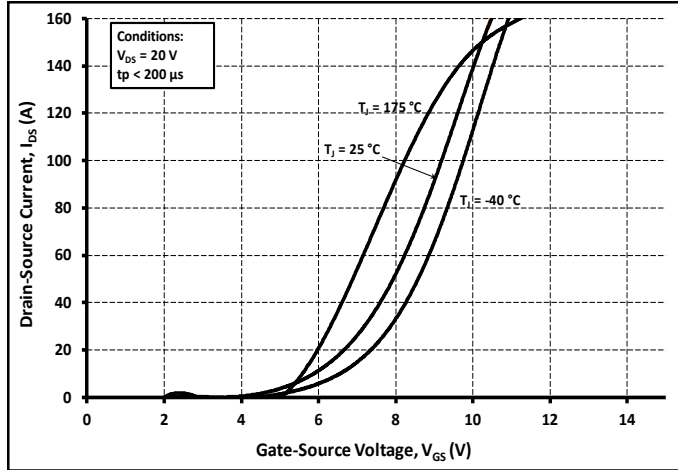


**Figure 5.** On-Resistance vs. Drain Current  
For Various Temperatures

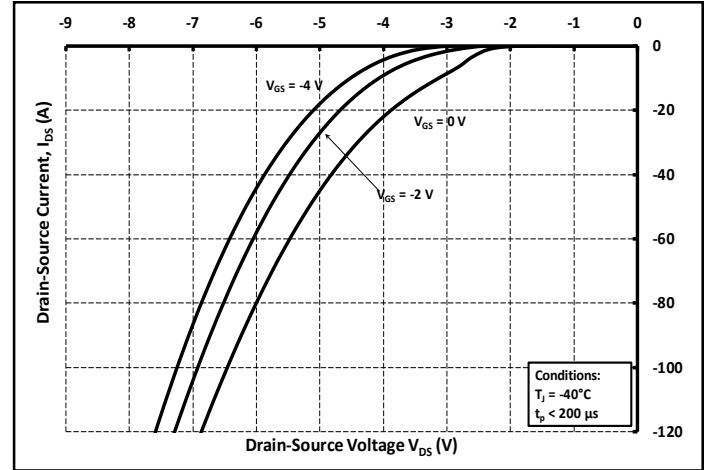


**Figure 6.** On-Resistance vs. Temperature  
For Various Gate Voltage

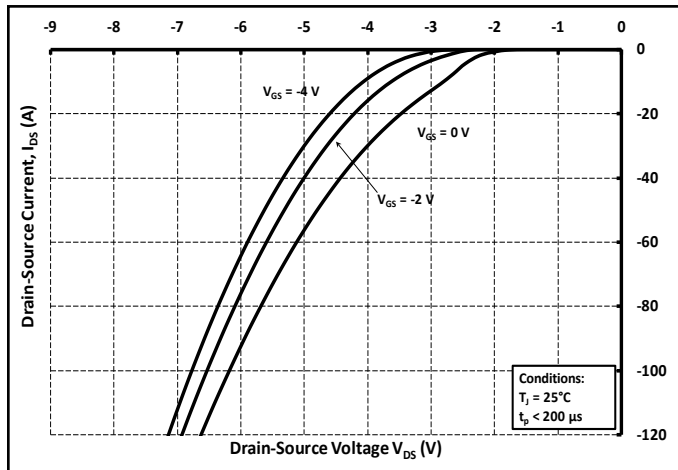
## Typical Performance



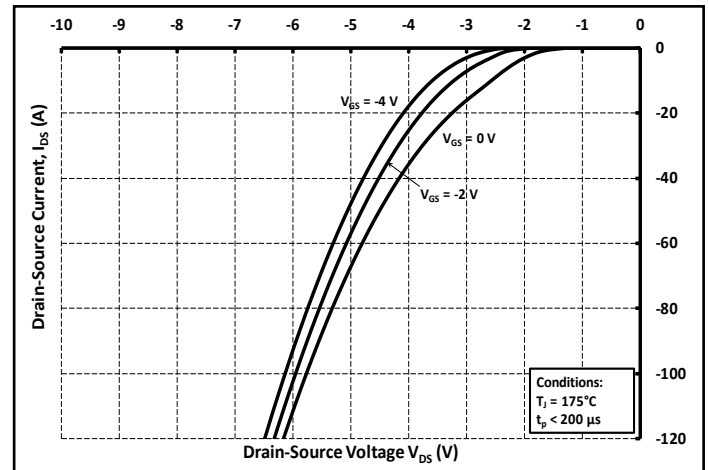
**Figure 7.** Transfer Characteristic for Various Junction Temperatures



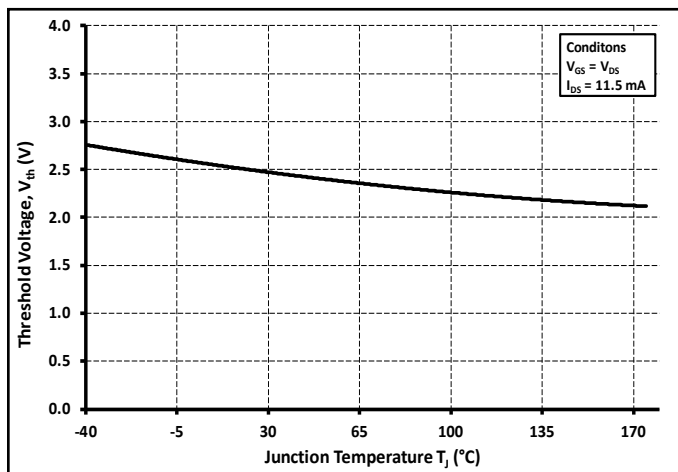
**Figure 8.** Body Diode Characteristic at  $-40^\circ\text{C}$



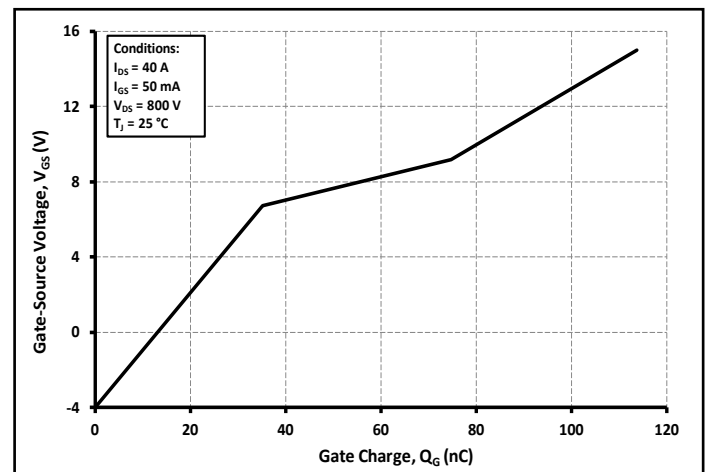
**Figure 9.** Body Diode Characteristic at  $25^\circ\text{C}$



**Figure 10.** Body Diode Characteristic at  $175^\circ\text{C}$

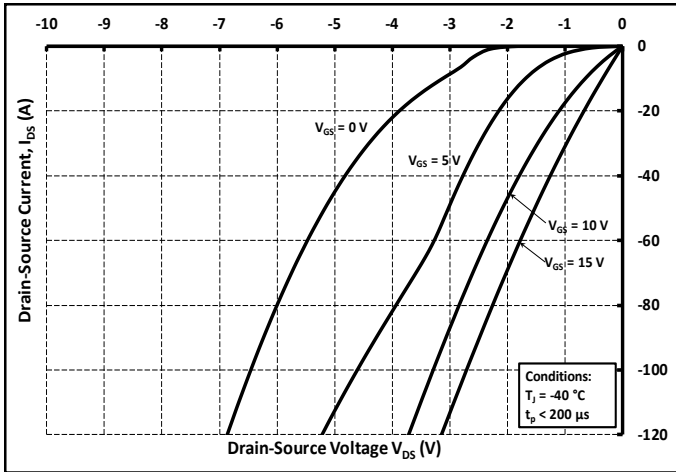


**Figure 11.** Threshold Voltage vs. Temperature

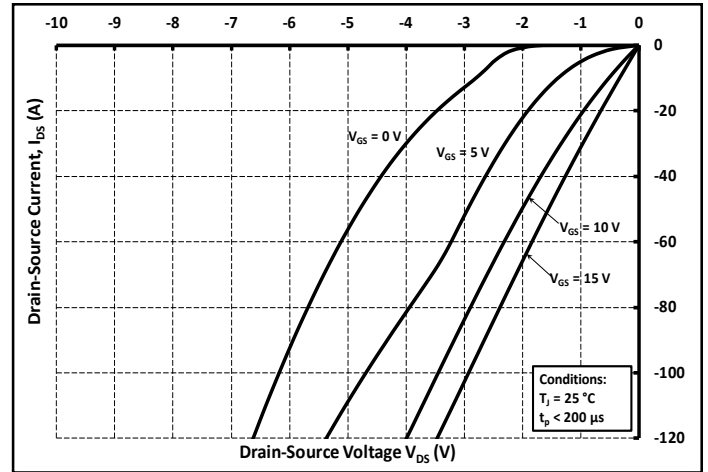


**Figure 12.** Gate Charge Characteristics

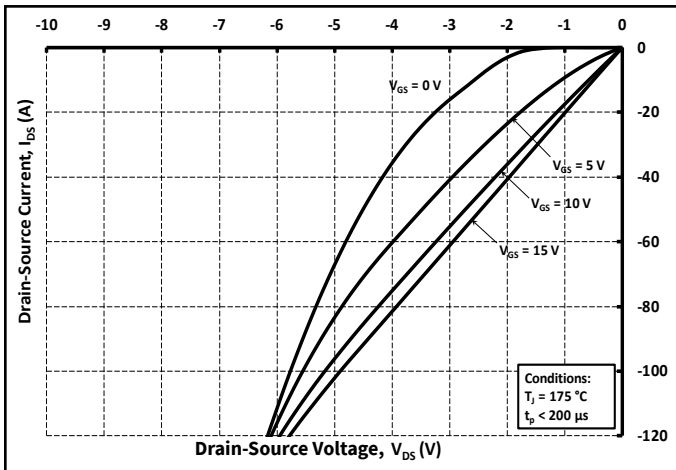
## Typical Performance



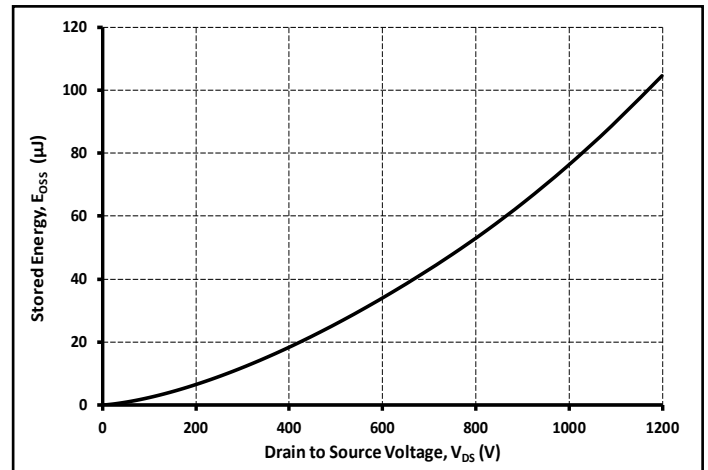
**Figure 13.** 3rd Quadrant Characteristic at  $-40^{\circ}\text{C}$



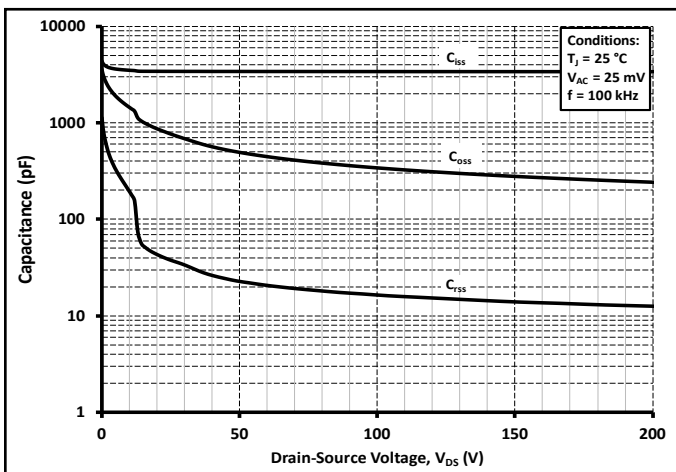
**Figure 14.** 3rd Quadrant Characteristic at  $25^{\circ}\text{C}$



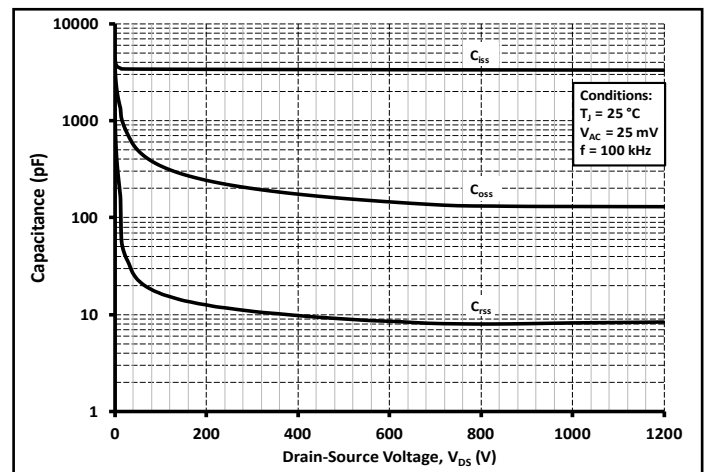
**Figure 15.** 3rd Quadrant Characteristic at  $175^{\circ}\text{C}$



**Figure 16.** Output Capacitor Stored Energy

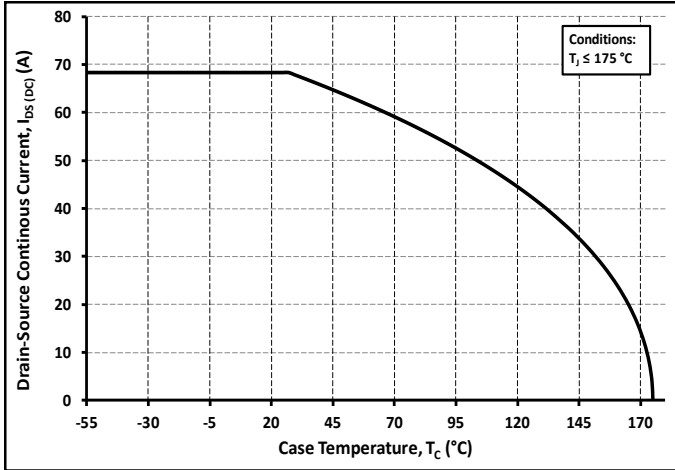


**Figure 17.** Capacitances vs. Drain-Source Voltage (0 - 200 V)

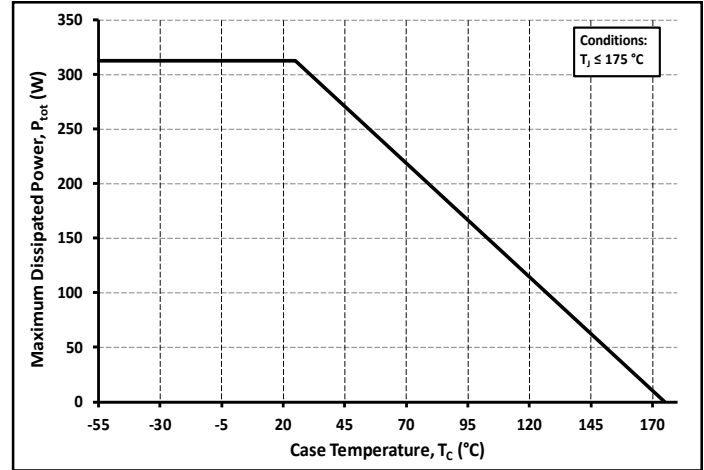


**Figure 18.** Capacitances vs. Drain-Source Voltage (0 - 1200 V)

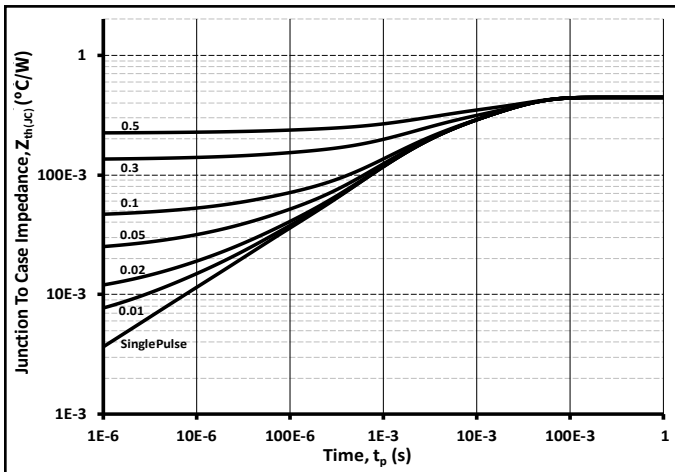
## Typical Performance



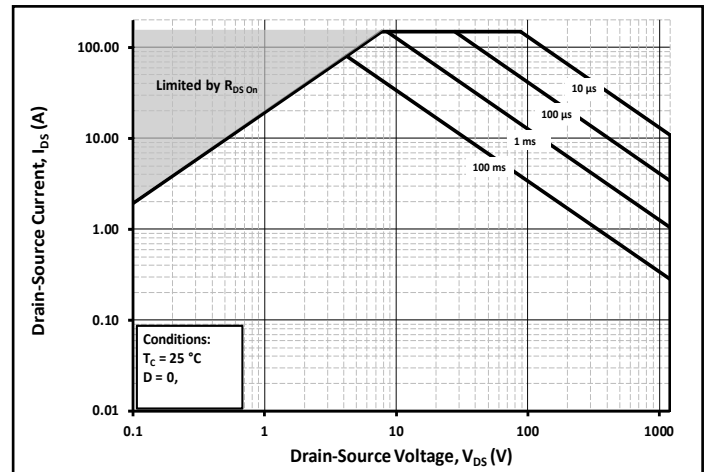
**Figure 19.** Continuous Drain Current Derating vs. Case Temperature



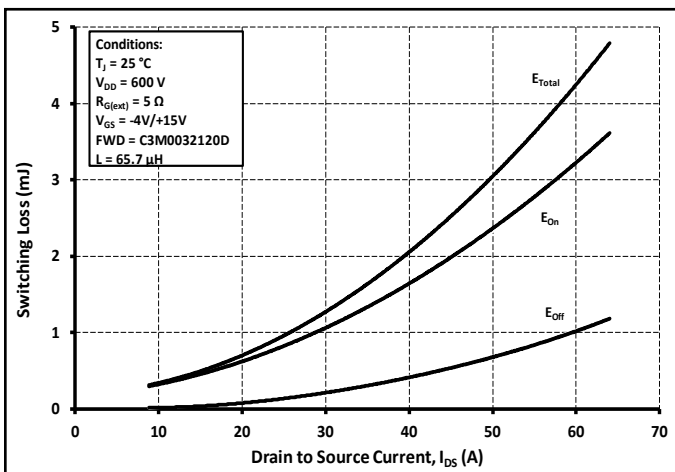
**Figure 20.** Maximum Power Dissipation Derating vs. Case Temperature



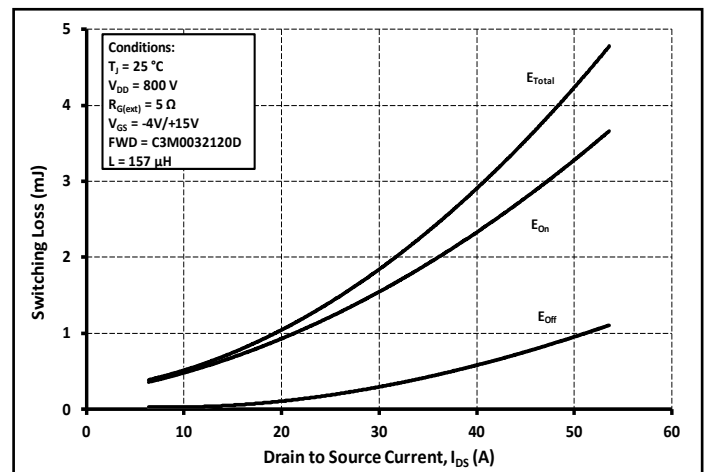
**Figure 21.** Transient Thermal Impedance (Junction - Case)



**Figure 22.** Safe Operating Area



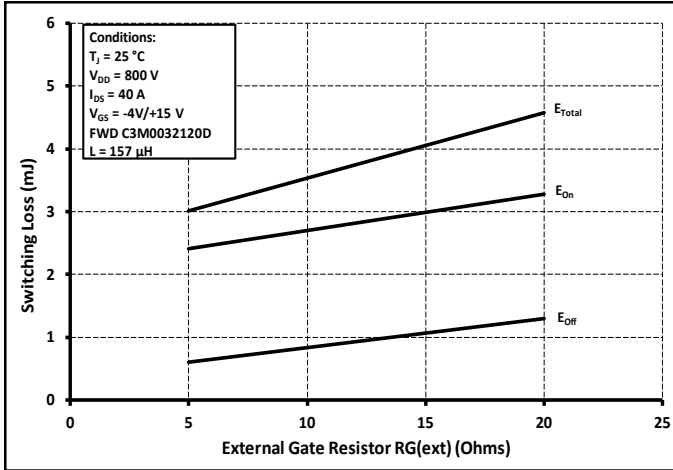
**Figure 23.** Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600\text{ V}$ )



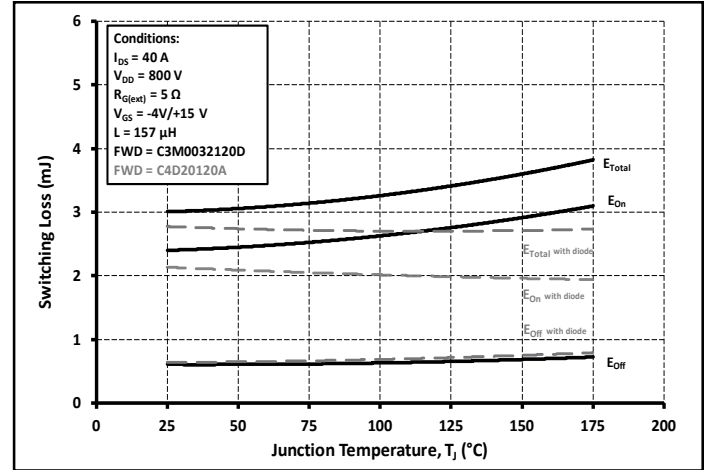
**Figure 24.** Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 800\text{ V}$ )



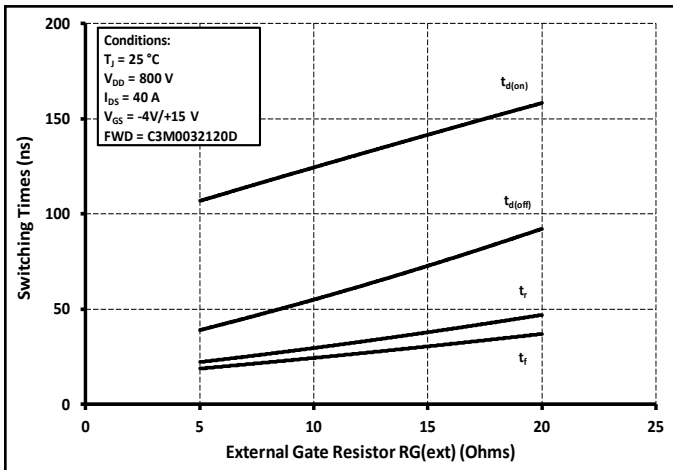
## Typical Performance



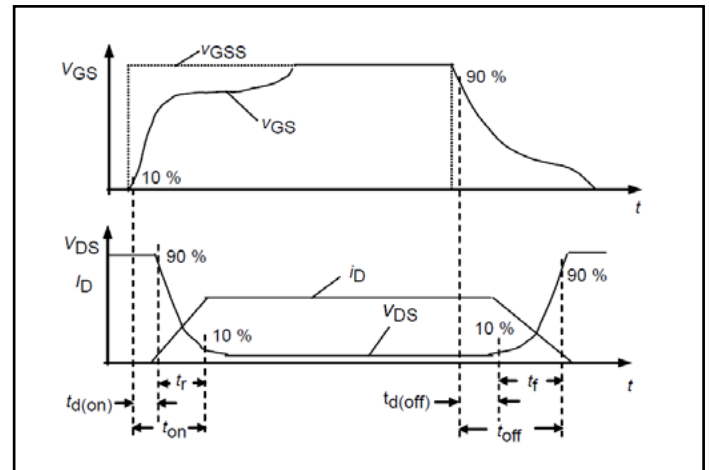
**Figure 25.** Clamped Inductive Switching Energy vs.  $R_{G(ext)}$



**Figure 26.** Clamped Inductive Switching Energy vs. Temperature



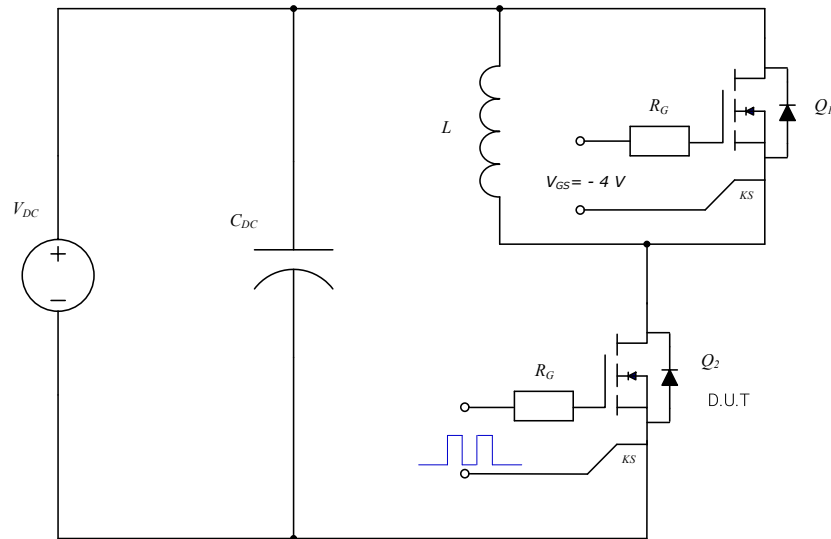
**Figure 27.** Switching Times vs.  $R_{G(ext)}$



**Figure 28.** Switching Times Definition



## Test Circuit Schematic

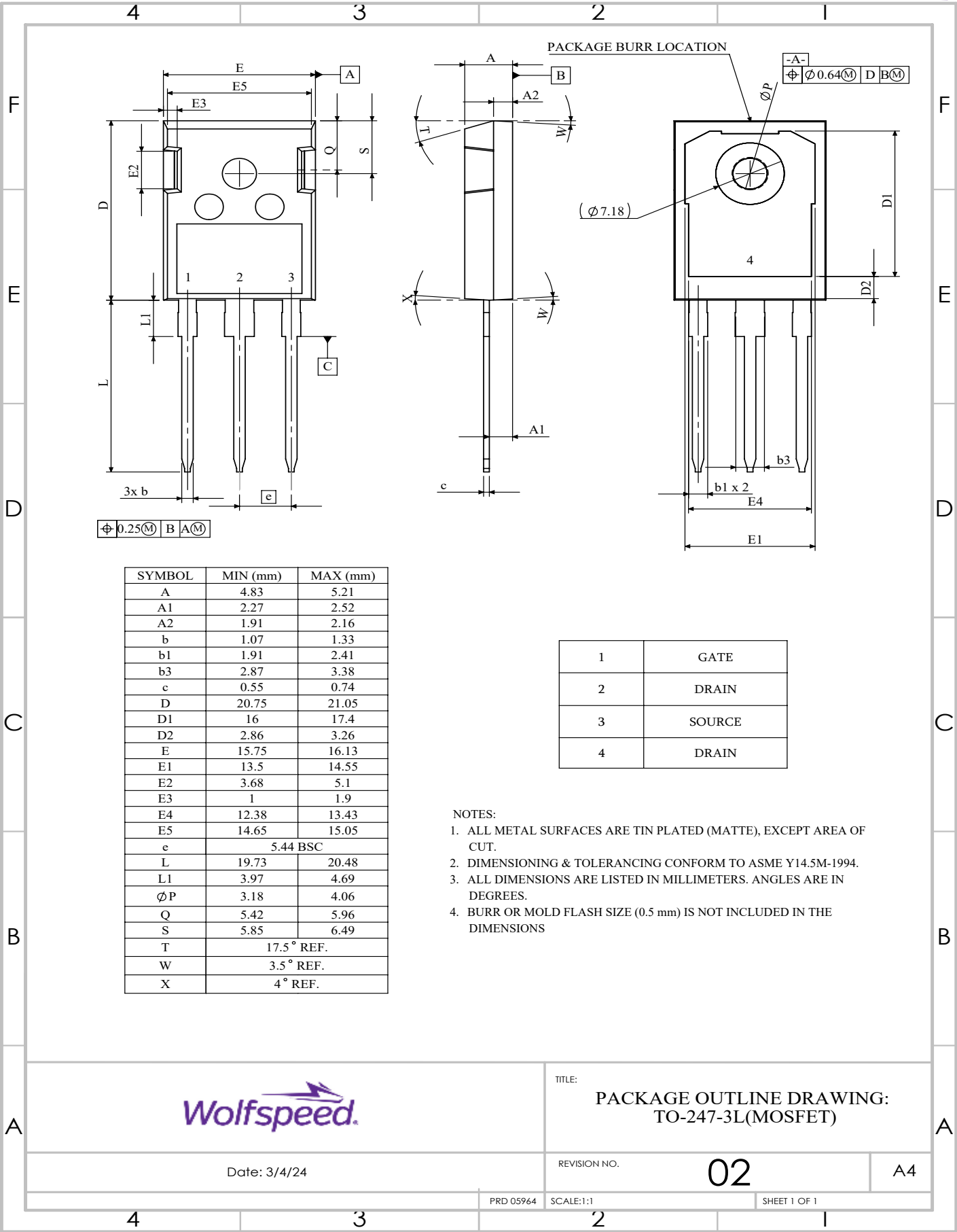


**Figure 29.** Clamped Inductive Switching Waveform Test Circuit

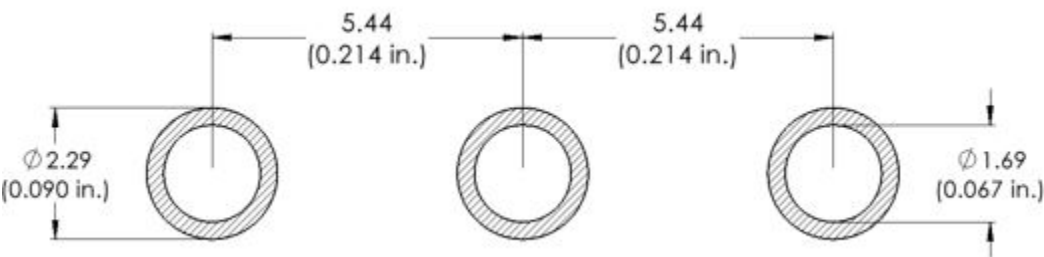
**Note:**

<sup>3</sup> Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

Package Dimensions - TO-247-4L



Recommended Solder Pad Layout



Revision History

Current Revision	Date of Release	Description of Changes
-	December-2019	N/A
1	January-2024	Updated WolfSpeed branding, package drawing, package image, and solder pad layout, added Revision History Table. Table 1 layout revised
2	September - 2024	Legal Disclaimer, POD, Diode Pulse Current Symbol

Related Links

- [SPICE Models](http://wolfspeed.com/power/tools-and-support): <http://wolfspeed.com/power/tools-and-support>
- [SiC MOSFET Isolated Gate Driver Reference Design](http://wolfspeed.com/power/tools-and-support): <http://wolfspeed.com/power/tools-and-support>
- [SiC MOSFET Evaluation Board](http://wolfspeed.com/power/tools-and-support): <http://wolfspeed.com/power/tools-and-support>



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### **Contact info:**

4600 Silicon Drive  
Durham, NC 27703 USA  
Tel: +1.919.313.5300  
[www.wolfspeed.com/power](http://www.wolfspeed.com/power)