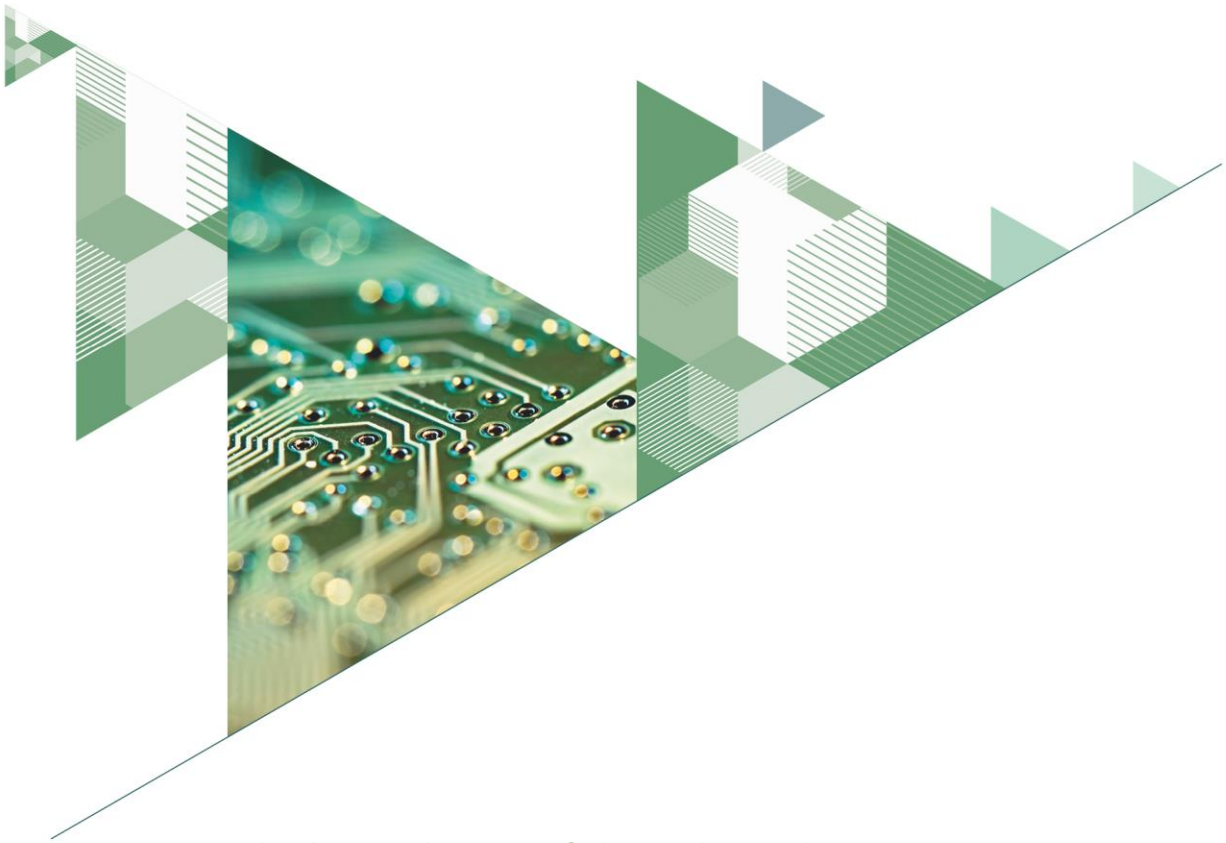


# CGD65A130SH2 DATASHEET

## H2 series 650 V / 130 mΩ GaN HEMT with ICeGaN™ Gate, Current Sense and NL$^3$ Circuit

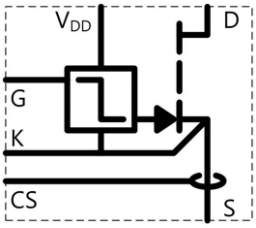
APRIL 2024

CAMBRIDGE GaN DEVICES

# H2 series 650 V / 130 mΩ GaN HEMT with ICeGaN™ Gate, Current Sense and NL$^3$ Circuit

## Key features

- 650 V – 12 A e-mode GaN power switch
- ICeGaN gate technology for high gate threshold, broad gate voltage window and excellent gate robustness
- Gate drive voltage 9 V to 20 V
- Innovative NL$^3$ circuit to boost No Load, Light Load efficiency
- Current sense function
- Integrated Miller Clamp for 0 V TurnOFF
- $R_{DS(on)}$ = 130 mΩ
- Suitable for very high switching frequency
- Small 8x8 mm$^2$ PCB footprint
- Bottom side cooled DFN package





## Description

The CGD65A130SH2 is an enhancement mode GaN-on-silicon power transistor, exploiting the unique material properties of GaN to deliver high current, high breakdown voltage and high switching frequency for a wide range of electronics applications. The CGD65A130SH2 features CGD's ICeGaN gate technology enabling compatibility with virtually all gate drivers and controller chips available. The integrated current sense function eliminates the need for a separate current sense resistor in series with the source and the associated efficiency losses. Because no separate current sense resistor connected to source is needed, the device can be directly soldered to the large copper area of the ground plane, improving the thermal performance and simplifying the thermal design. The H2 series ICeGaN features an advanced NL$^3$ Circuit that leads to near-zero device losses at no-load conditions. It comes in a DFN 8x8 SMD package to support high frequency operation while ensuring the highest thermal performance.

## Application & Topologies

PSUs, Industrial SMPS and inverters

- USB PD and fast charging
- AC adapters
- Notebook adapters, PC power
- Gaming PSUs
- LED lighting
- Class-D Audio
- TV and wireless power
- PV micro-inverters
- SMPS and converters in single-switch and half-bridge topologies with hard- or soft-switching
- DC/DC converters
- Quasi-resonant flyback and Active Clamp flyback
- Totem pole and single-switch PFC
- LLC and high frequency converters
- Class-E inverters

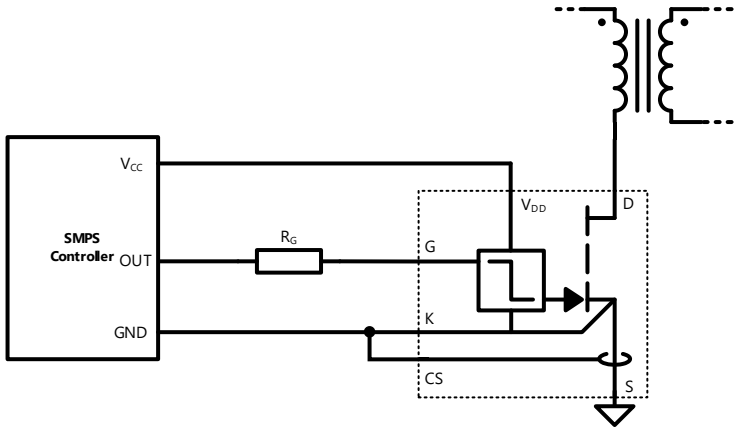
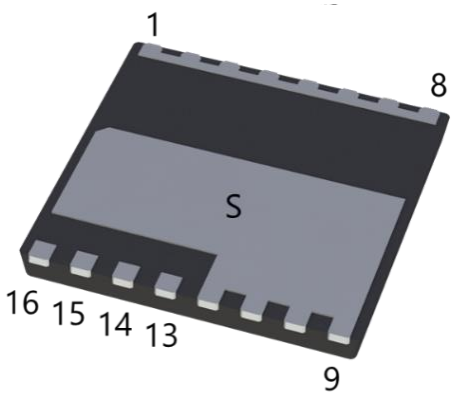



*Figure 1. Exemplary Application Circuit*




| PIN | NAME | DESCRIPTION |
|---|---|---|
| 1-8 | Drain | Power HEMT Drain. |
| 9-12 | Source | Power HEMT Source, thermal pad. |
| 13 | Kelvin Source | Kelvin Source connection (internally tied to power HEMT Source), reference potential for gate voltage. |
| 14 | Gate | Gate signal input.<br>Recommended gate-drive voltage: $V_{drive}$ ($V_{GS}$ in on-state) = 9 V to $V_{DD}$. |
| 15 | Current Sense | Current Sense output, relative to Source, non-isolated.<br>Pin must not be left floating. When not used short it to Source. |
| 16 | $V_{DD}$ | ICeGaN™ gate supply voltage (recommended at 12 V), relative to Source. |

*Figure 2. Pin Configuration and Functions*

## Absolute Maximum Ratings

$T_{case}$ = 25 °C if not listed.

| PARAMETER | | VALUE | UNIT |
|---|---|---|---|
| Operating junction temperature | $T_J$ | -55 to +150 | °C |
| Storage temperature range | $T_S$ | -55 to +150 | °C |
| Drain-to-Source voltage | $V_{DS}$ | 650 | V |
| Drain-to-Source voltage - transient [1] | $V_{DS(transient)}$ | 750 | V |
| Gate-to-Source voltage | $V_{GS}$ | -1 to +20 and $V_{GS} \leq V_{DD}$ | V |
| Gate-to-Source voltage - transient [2] | $V_{GS(transient)}$ | -1.5 to +21.5 and $V_{GS} \leq V_{DD}$ + 1.5 | V |
| Current Sense voltage | $V_{CS}$ | -1.5 to 1.5 | V |
| ICeGaN gate supply voltage | $V_{DD}$ | 0 to +20 | V |
| Continuous drain current | $I_{D(continuous)}$ | 12 | A |
| Continuous drain current ($T_{case}$ = 100 °C) | $I_{D(continuous)}$ | 7.5 | A |

The recommended range of operation for $V_{drive}$ ($V_{GS}$ in on-state) and $V_{DD}$ is 9 V to 20 V, enabling simple integration with a large variety of control chips and gate drivers.
Recommended maximum operating case temperature: $T_{case}$ = 125 °C.

[1] Non-repetitive pulsed conditions, < 1 ms.

[2] Non-repetitive pulsed conditions, < 1 ms.

## Electrical Characteristics

Values at $T_J$ = 25 °C, $V_{DD}$ = 12 V if not listed. To turn the device on the recommended gate voltage range is $V_{GS}$ = 9 V to $V_{DD}$. To turn the device off set $V_{GS}$ = 0 V. An integrated Miller Clamp eliminates the need for negative gate voltages.

### STATIC CHARACTERISTICS

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Drain-to-Source Blocking voltage | $BV_{DS}$ | $V_{GS}$ = 0 V, $I_{DSS}$ = 8.5 µA | 650 | | | V |
| Drain-to-Source on resistance | $R_{DS(on)}$ | $V_{GS}$ = 12 V, $I_D$ = 0.9 A | | 130 | 182 | mΩ |
| Drain-to-Source on resistance | $R_{DS(on)}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 12 V, $I_D$ = 0.9 A | | 350 | | mΩ |
| Source-to-Drain voltage | $V_{SD(on)}$ | $V_{GS}$ = 0 V, $I_D$ = 0.9 A | | 2.0 | 3.7 | V |
| Gate-to-Source threshold | $V_{GS(th)}$ | $V_{DS}$ = 0.1 V, $I_D$ = 4.2 mA | 2.2 | 2.9 | 4.2 | V |
| Gate-to-Source threshold | $V_{GS(th)}$ | $T_J$ = 150 °C<br>$V_{DS}$ = 0.1 V, $I_D$ = 4.2 mA | | 2.6 | | V |
| Gate-to-Source current | $I_{GS}$ | $V_{GS}$ = 12 V, $V_{DS}$= 0 V | | 2.6 | 3.7 | mA |
| Gate-to-Source current | $I_{GS}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 12 V, $V_{DS}$= 0 V | | 2.0 | | mA |
| $V_{DD}$ current ($V_{GS}$ in on-state) | $I_{VDD}$ | $V_{GS}$ = 12 V, $V_{DS}$= 0 V | | 0.8 | 1.4 | mA |
| $V_{DD}$ current ($V_{GS}$ in on-state) | $I_{VDD}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 12 V, $V_{DS}$= 0 V | | 0.4 | | mA |
| $V_{DD}$ current ($V_{GS}$ in off-state) | $I_{VDD}$ | $V_{GS}$ = 0 V, $V_{DS}$= 0 V | | 70 | 150 | µA |
| $V_{DD}$ current ($V_{GS}$ in off-state) | $I_{VDD}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 0 V, $V_{DS}$= 0 V | | 35 | | µA |
| $V_{DD}$ start-up current ($V_{GS}$ in off-state) | $I_{VDD\_start}$ | $V_{GS}$ = 0 V, $V_{DS}$= 0 V | | 250 | | µA |
| Drain-to-Source leakage current | $I_{DSS}$ | $V_{GS}$ = 0 V, $V_{DS}$ = 650 V | | 0.2 | 8.5 | µA |
| Drain-to-Source leakage current | $I_{DSS}$ | $T_J$ = 150 °C<br>$V_{GS}$ = 0 V, $V_{DS}$ = 650 V | | 12 | | µA |

The H2 series ICeGaN features an advanced NL$^3$ (No Load, Light Load) Circuit that leads to near-zero device losses at no-load conditions through very low $V_{DD}$ current while $V_{GS}$ is in off-state.

## DYNAMIC CHARACTERISTICS

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Output capacitance[3] | $C_{OSS}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V<br>f = 100 kHz | | 21 | | pF |
| Time-related effective output capacitance[4] | $C_{O(TR)}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V | | 52 | | pF |
| Energy-related effective output capacitance[5] | $C_{O(ER)}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V | | 33 | | pF |
| Output charge | $Q_{OSS}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V | | 21 | | nC |
| Output capacitance stored energy | $E_{OSS}$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V | | 2.7 | | µJ |
| Total gate charge[6] | $Q_G$ | $V_{DS}$ = 400 V, $V_{GS}$ = 0…12 V<br>$I_D$ = 4.2 A, $I_G$=20 mA | | 1.9 | | nC |
| Reverse recovery charge | $Q_{RR}$ | | | 0 | | nC |
| Turn-on delay time | $t_{d(on)}$ | See Figure 18 and Figure 19 | | 6 | | ns |
| Turn-off delay time | $t_{d(off)}$ | See Figure 18 and Figure 19 | | 16 | | ns |
| $V_{DS}$ rise time | $t_r$ | See Figure 18 and Figure 19 | | 4.5 | | ns |
| $V_{DS}$ fall time | $t_f$ | See Figure 18 and Figure 19 | | 4.5 | | ns |

## CURRENT SENSING

Please refer to the application note CG-AN2206: Current Sensing with ICeGaN. Please contact CGD for advice on the use of the current sense function.

## ESD RATING

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| ESD withstand rating | HBM | Human Body Model<br>(per JEDEC JS-001-2017) | 2000 | | | V |

[3] Evaluated using small-signal measurements.

[4] $C_{O(TR)}$ is the value of fixed capacitance that takes the same amount of charging time as $C_{OSS}$ when $V_{DS}$ changes from 0 V to a given $V_{DS}$, assuming a constant-current charging process.

[5] $C_{O(ER)}$ is the value of fixed capacitance that stores the same amount of energy as $C_{OSS}$ when $V_{DS}$ changes from 0 V to a given $V_{DS}$.

[6] Turn-on gate charge value is listed. Turn-off gate charge value is lower, because ICeGaN gate discharges the gate internally.

## Thermal Characteristics

Typical values unless otherwise specified.

| PARAMETER | | CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| Thermal resistance, junction to case | $R_{th(JC)}$ | | 1.6 | °C/W |
| Maximum reflow soldering temperature | $T_{reflow}$ | MSL 3 | 260 | °C |

## Figures

Figures at $T_J$ = 25 °C, $V_{DD}$ = 12 V if not specified.

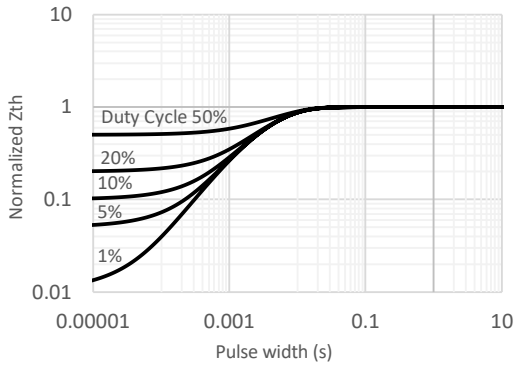



*Figure 3. Normalized thermal transient impedance ($Z_{th,JC}$) as a function of pulse width.*

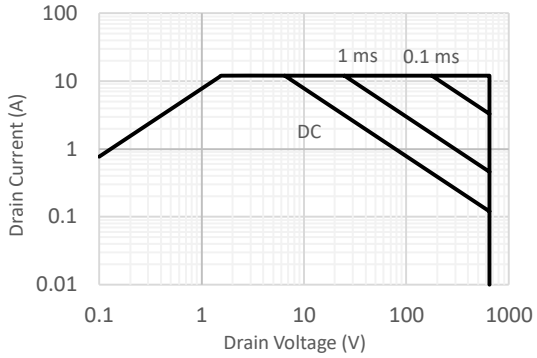



*Figure 4. Safe Operating Area (SOA) based on thermal impedance $Z_{th,JC}$ at $T_{CASE}$ = 25 °C.*

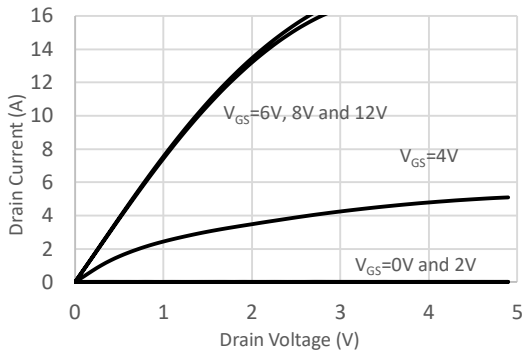



*Figure 5. Forward output characteristics at $T_J$ = 25 °C.*

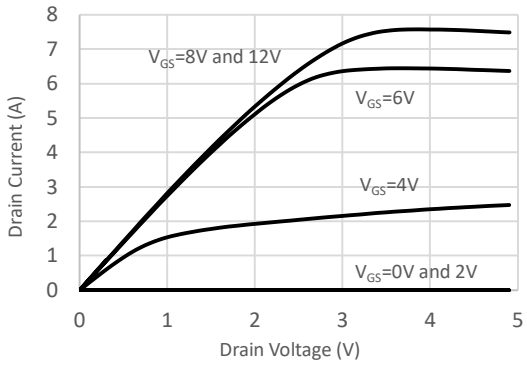



*Figure 6. Forward output characteristic at $T_J$ = 150 °C.*

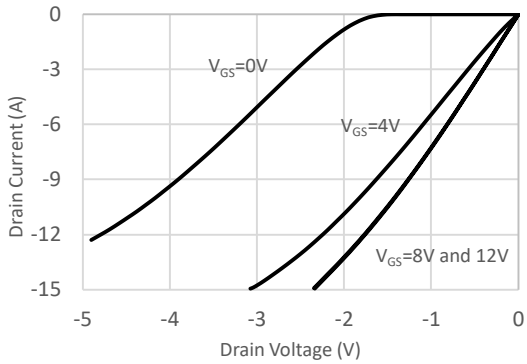



*Figure 7. Reverse output characteristics at $T_J$ = 25 °C.*

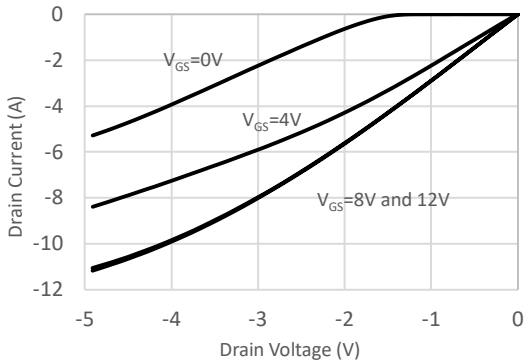



*Figure 8. Reverse output characteristics at $T_J$ = 150 °C.*

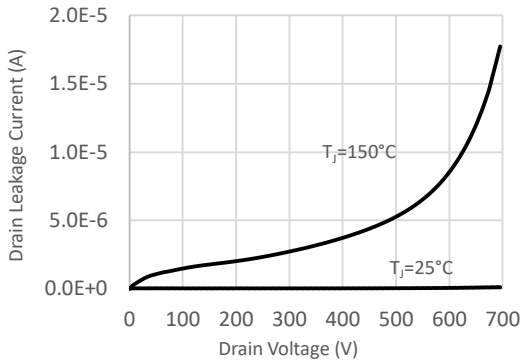



*Figure 9. Drain leakage current characteristics at $T_J$ = 25 °C and $T_J$ = 150 °C.*

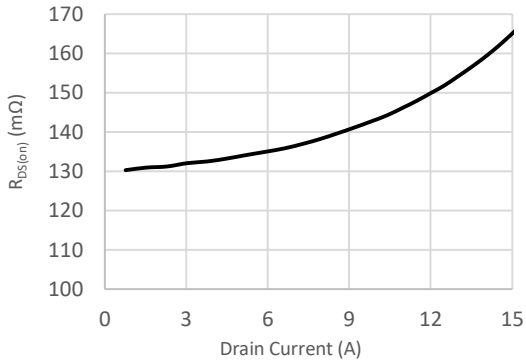



*Figure 10. On-state resistance as a function of drain current at $T_J$ = 25 °C.*

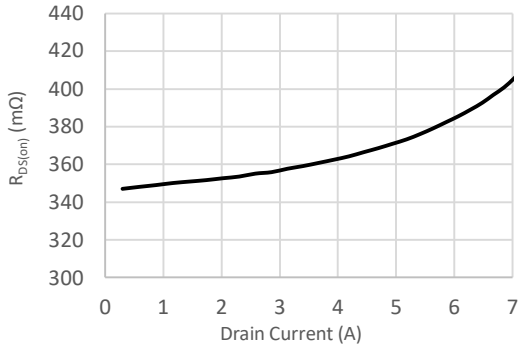



*Figure 11. On-state resistance as a function of drain current at $T_J$ = 150 °C.*

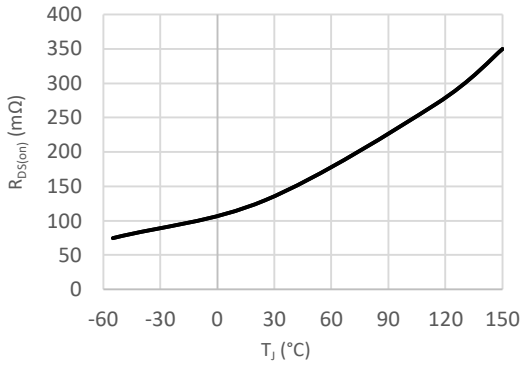



*Figure 12. On-state resistance as a function of junction temperature at $V_{GS}$ = 12 V and $I_D$ = 0.9 A.*

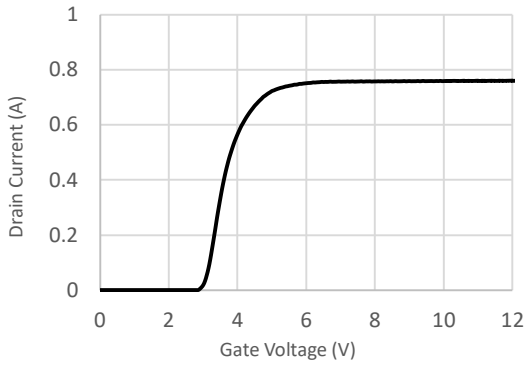



*Figure 13. Transfer characteristics at $V_{DS}$ = 0.1 V, $T_J$ = 25 °C.*

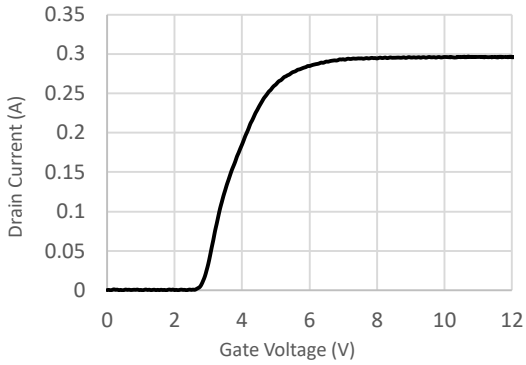



*Figure 14. Transfer characteristics at $V_{DS}$ = 0.1 V, $T_J$ = 150 °C.*

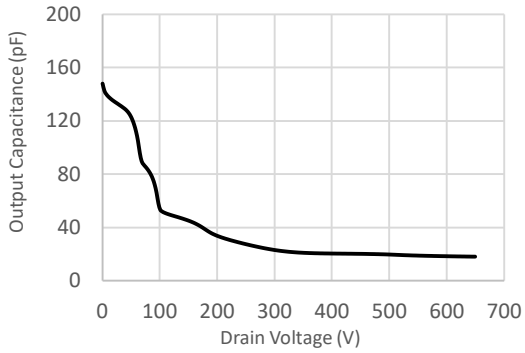



*Figure 15. Typical output capacitance $C_{OSS}$ vs. $V_{DS}$ at 100 kHz, $T_J$ = 25 °C.*

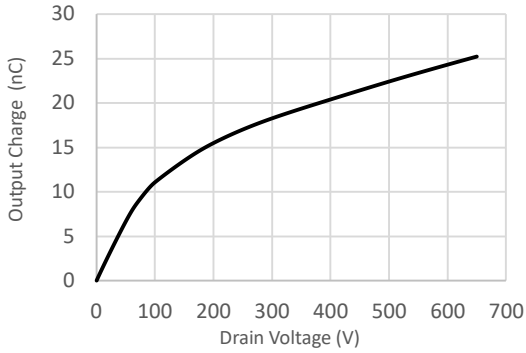



*Figure 16. Typical output charge $Q_{OSS}$ vs. $V_{DS}$ at 100 kHz, $T_J$ = 25 °C.*

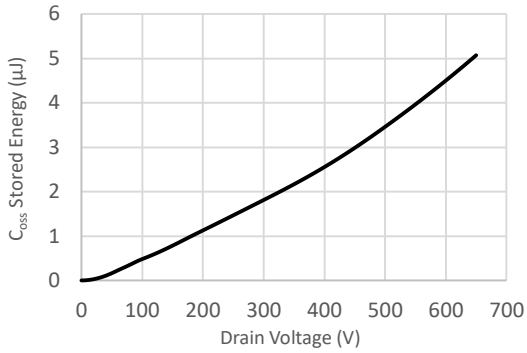



*Figure 17. Typical $C_{OSS}$ stored energy $E_{OSS}$ vs. $V_{DS}$ at $T_J$ = 25 °C.*

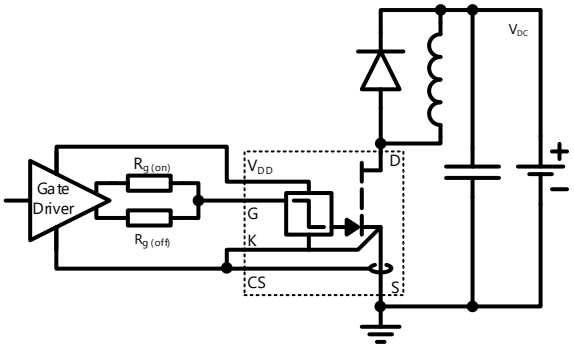



*Figure 18. Inductive switching circuit. $I_D$ = 6 A, $R_{g(on)}$ = 15 Ω, $R_{g(off)}$ = 2 Ω, $V_{DD}$ = 12 V, $V_{DC}$ = 400 V, L = 125 µH, diode = IDH04G65C5.*

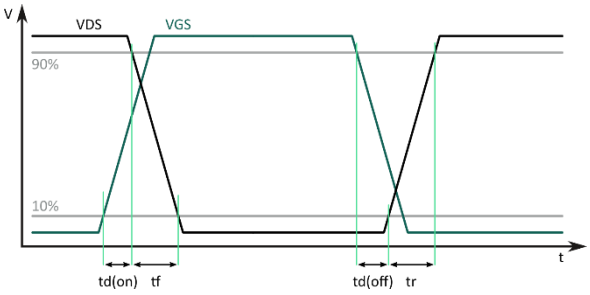



*Figure 19. Switching waveform timing definitions.*

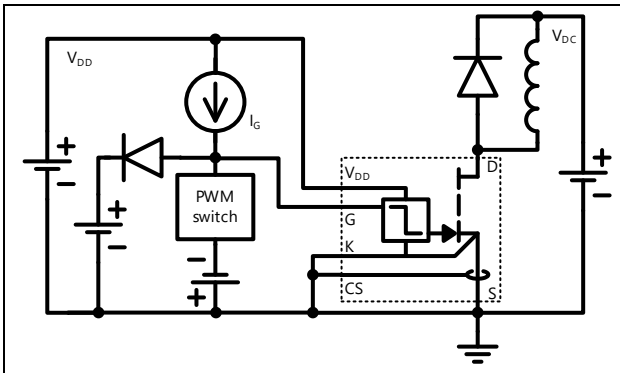



*Figure 20. $Q_G$ gate charge characterization circuit. $I_G$=20 mA, $V_{DC}$ = 400 V, $V_{DD}$=12V, L = 125 µH, freewheeling diode = IDH04G65C5.*

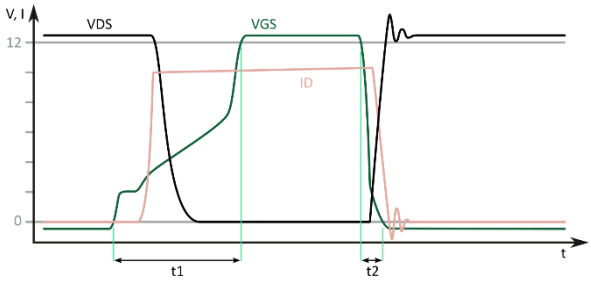
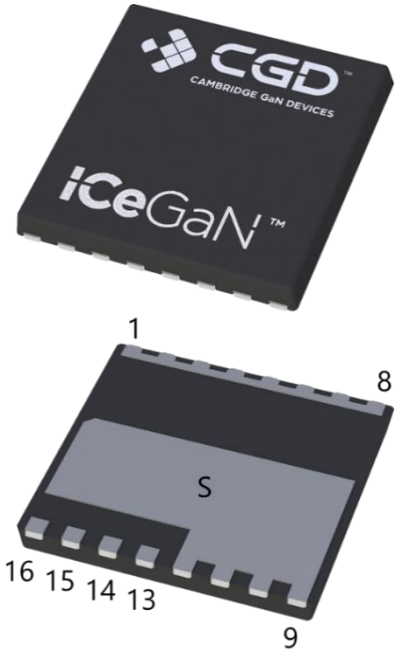


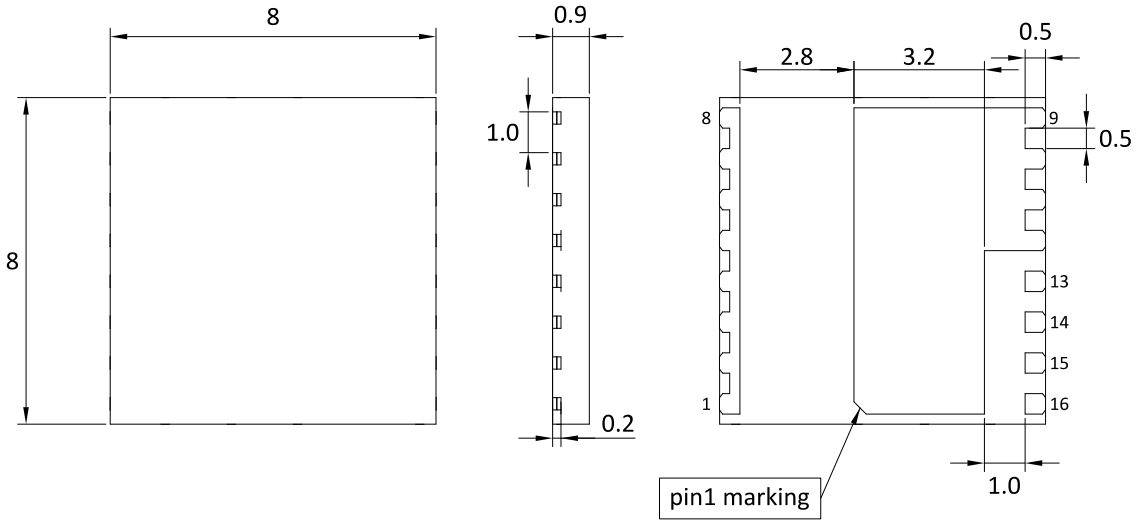

*Figure 21. $Q_G$ gate charge characterisation waveform at $I_G$ = 20 mA and $V_{DD}$ = 12 V. Time intervals t1 and t2 indicate the integration boundaries to calculate $Q_G$ from $I_G$ at turn-on and turn-off. Turn-off gate charge is lower than turn-on gate charge.*

## Packaging

DFN 8x8 mm.

| PIN NUMBER | NAME |
|---|---|
| 1-8 | Drain |
| 9-12 | Source |
| 13 | Kelvin Source |
| 14 | Gate |
| 15 | Current Sense |
| 16 | $V_{DD}$ |

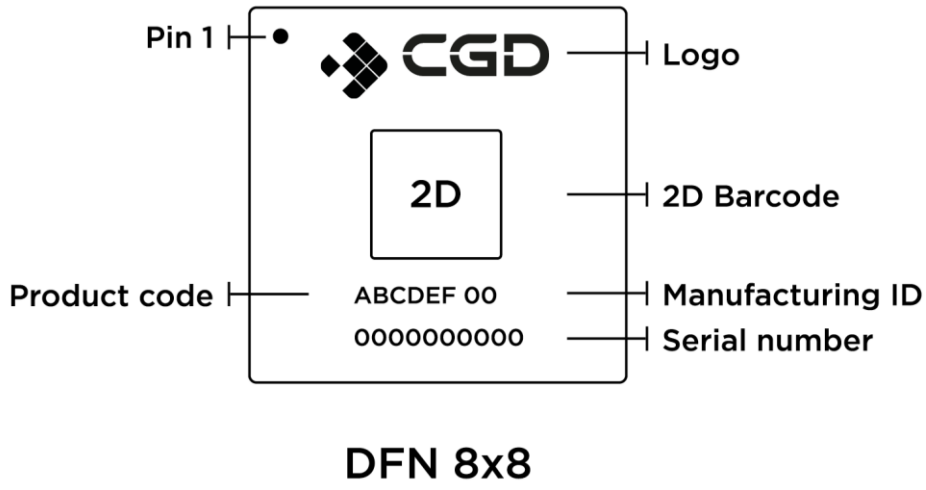



top view bottom view

Like any unwanted electronic device, CGD components should be recycled or otherwise disposed of in accordance with local laws and regulations.

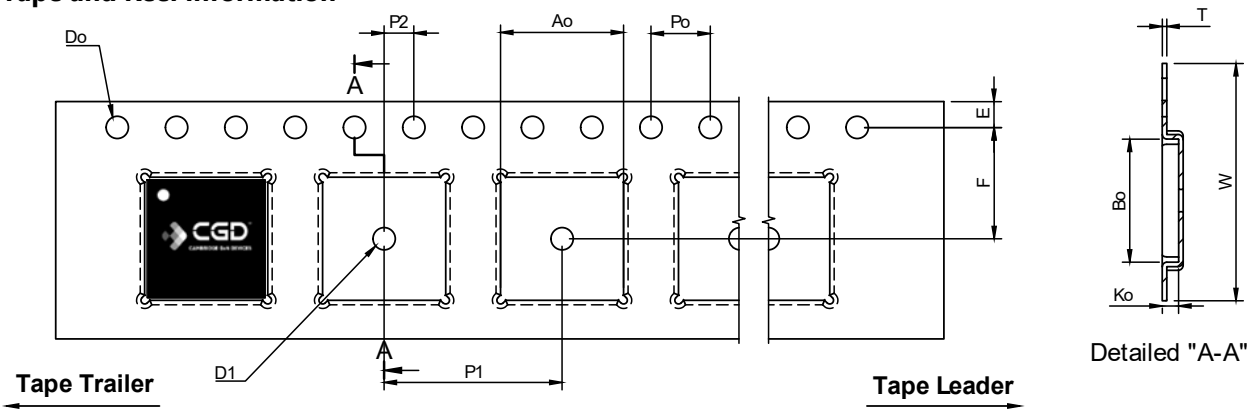
**Package Marking:**



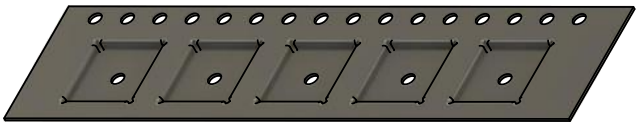

DFN 8x8

| PRODUCT CODE | PART NUMBER |
|---|---|
| 65U1SY | CGD65A130SH2 |

## Tape and Reel Information

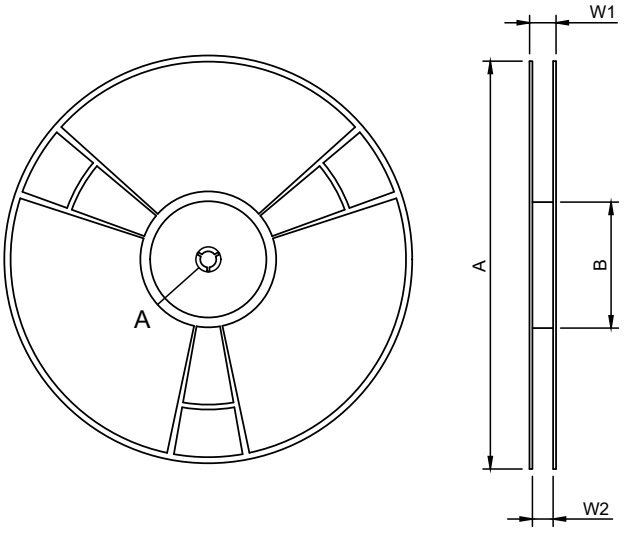



Tape Trailer - a minimum length of 160mm empty cavities sealed with cover tape.
Tape Leader - a minimum length of 400mm empty cavities sealed with cover tape.



Isometric View

| Dimensions (mm) | | |
|---|---|---|
| | Nominal | Tolerance |
| Ao | 8.30 | ± 0.10 |
| Bo | 8.30 | ± 0.10 |
| Ko | 1.25 | ± 0.05 |
| E | 1.75 | ± 0.10 |
| F | 7.50 | ± 0.10 |
| Po | 4.00 | ± 0.10 |
| P1 | 12.00 | ± 0.10 |
| P2 | 2.00 | ± 0.10 |
| W | 16.00 | ± 0.3 |
| T | 0.30 | ± 0.05 |
| Do | Ø1.50 | + 0.1 / - 0.0 |
| D1 | Ø1.50 | + 0.2 / - 0.0 |




| 13" Reel Dimensions (mm) | | |
|---|---|---|
| | Min | Max |
| W1 | | 22.2 |
| W2 | 16.6 | 17.1 |
| A | 328.0 | 332.0 |
| B | 100.0 | 104.0 |
| C | 20.2 | |
| D | 1.5 | 2.5 |
| E | 12.8 | 13.5 |

## Ordering Information

| ORDERING CODE | PACKAGE TYPE | FORM | QUANTITY |
|---|---|---|---|
| CGD65A130SH2-T13 | DFN 8x8 mm | Tape-and-Reel (13”) | 3500 |

**Version History**

This version is 2.0

| VERSION | DESCRIPTION | DATE | BY |
|---|---|---|---|
| 1.0 | Initial Release | July 2023 | JZ, MA |
| 2.0 | Added $I_D$ ($T_{case}$= 100°C) in Absolute Maximum Ratings table, added $C_{O(TR)}$, $C_{O(ER)}$, $E_{OSS}$ specifications and updated values of $t_{d(off)}$, $t_r$ and $t_f$, in Dynamic Characteristics table, added Figure 11, updated the range of Figures 15, 16, 17, added package marking and ordering information. | April 2024 | NG |

*Dare to innovate differently*

CGD™
CAMBRIDGE GaN DEVICES

Cambridge GaN Devices Limited
Jeffreys Building, Suite 8
Cowley Road
Cambridge
CB4 0DS
United Kingdom