CMX90A705 5.5W Ka-Band GaN Power Amplifier

Description

The CMX90A705 is a packaged two-stage Ka-band GaN linear power amplifier delivering 37.4 dBm (5.5 W) of saturated power with 16.5 dB of small signal gain. It can be used as both driver stage and final stage PA in a commercial satellite communication terminal.

RF ports are nominally matched to 50 Ω for ease of use, with integrated DC blocking capacitors at RF input and output. The PCB will incorporate drain and gate feed decoupling capacitors suitable for modulated signals e.g. QPSK.

The active device is fabricated using state-of-the-art 0.15 µm gate length GaN-on-SiC process and packaged in a small form factor, 4 x 4 mm thermally enhanced plastic air-cavity QFN.

4x4mm AQFN-12 Package

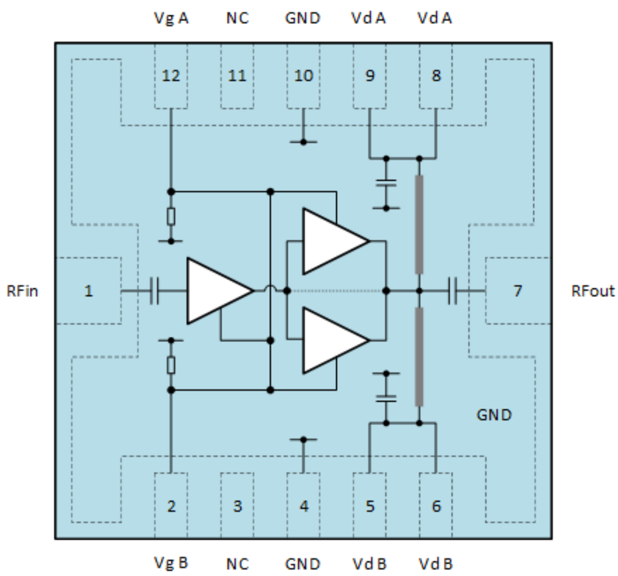
Product Features

- Frequency range 27.5 – 31 GHz
- Saturated output power 37.4 dBm
- Small signal gain 16.5 dB
- RF ports matched to 50 Ω and DC blocked
- ACPR better than -28 dBc @ 30 dBm avg.
- Power added efficiency 22 % @ Psat
- Dual-side biasing
- DC bias 100mA @ +27.5 V

Applications

- High-volume commercial satcom terminals
- Telecommunications
- Residential satellite internet
- Commercial VSAT

Block Diagram



Ordering Information

Part Number	Description
CMX90A705A6-R701	7” Reel with 100 pieces
CMX90A705A6-R705	7” Reel with 500 pieces
EV90A705	Evaluation Board

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+30 dBm
Device Voltage (Vd)	+28 V
Power Dissipation (Pdiss)	18.8 W (Tc = 85 °C)
Junction Temperature (Tjmax)	225 °C (MTTF >1 x 10^6 hours)
Storage Temperature	-40 to +125 °C
ESD Sensitivity	HBM 250V (Class 1A); CDM 750V (Class C2b)
MSL Level	MSL3

Exceeding the maximum ratings may result in damage or reduced device reliability.

Thermal Characteristics

Parameter	Rating
Thermal Resistance (Rjc)	7.4°C/W (Tc = 70˚C)

Thermal resistance is junction-to-case, where case refers to the exposed die pad on the backside which is in contact with the board.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Frequency Range	27.5		31	GHz
Case Temperature (Tc)	-40		+85	°C
Device Voltage (Vd)	22	27.5	28	V
Gate Voltage (Vg)	-5	-1.89	-1.5	V
Power down Voltage (Vg)		-3		V

The device is tested under certain conditions, but performance is not guaranteed over the full range of recommended operating conditions.

ESD Caution

CMX90A705 incorporates ESD protection circuitry however ESD precautions are strongly recommended for handling and assembly. Ensure that devices are protected from ESD in antistatic bags or carriers when being transported. Personal grounding is to be worn at all times when handling these devices.

RoHS Compliance

All devices supplied by CML Microcircuits are compliant with RoHS directive (2011/65/EU), containing less than the permitted levels of hazardous substances.

Electrical Specification

Results taken on the EV90A705 EVB, where board losses have been de-embedded using TRL calibration.

Vd = 27.5 V, Idq = 100 mA, Ta = +25 °C and Zo = 50 Ω (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Units
Frequency		27.5		31	GHz
Small Signal Gain	27.5 GHz 29 GHz 31 GHz		16 17 14		dB
Reverse Isolation	27.5 GHz to 31 GHz		-43		dB
Psat	27.5 GHz 29 GHz 31 GHz		36.7 37.9 37.7		dBm
PAE	At saturated Pout, 29 GHz		22		%
OIP3	Average. Pout = 26 dBm/tone. At 29 GHz. Tone Spacing = 100 MHz		42		dBm
ACPR	Pout = 30 dBm, at 29 GHz 16-APSK, RC filter = 0.25 Symbol Rate = 100 Ms/s		-32.5		dBc
Input Return Loss	27.5 GHz to 31 GHz		-10		dB
Output Return Loss	27.5 GHz to 31 GHz		-9		dB
Gate Voltage (Vg)	Idq = 100 mA, No RF Input		-1.89		V
Standby Current (Id)	Vg = -5 V, No RF Input		162		uA
Drain Current (Id)	At Psat, 29 GHz		860		mA
Gate Current (Ig)	Idq = 100 mA, Vd = 27.5 V		-200		uA
Turn-On Time	RFin = TBC dBm		TBD		ns
Turn-Off Time	RFin = TBC dBm		TBD		ns

Pin Assignments

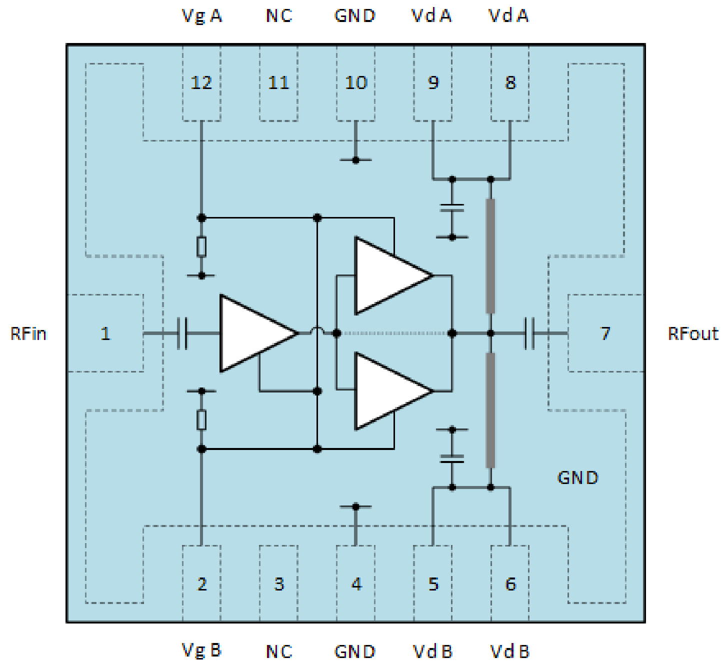


Figure 1 - Top View

Table 1 - Pin Assignments

Pin	Name	Description
1	RFin	RF input, nominally 50 Ω with integrated DC-blocking capacitor.
2	Vg B	Gate voltage (South)
3	NC	No connection
4	GND	DC and RF Ground
5, 6	Vd B	Drain voltage (South)
7	RFout	RF output, nominally 50 Ω with integrated DC-blocking capacitor.
8, 9	Vd A	Drain voltage (North)
10	GND	DC and RF Ground
11	NC	No connection
12	Vg A	Gate voltage (North)
Die pad	GND	DC and RF ground. Exposed die pad must be connected to GND.

Notes

The bottom exposed die pad must be connected to the ground plane on the board for electrical and thermal reasons, so a good connection is critical. Attention should be paid to the solder paste design to ensure that there isn't too much solder on the ground area thus causing the device to float and resulting in poor placement of part. See later section with recommended land pattern.

Vg and Vd connections can be made to either the North or South sides of the package. Vg and Vd connections to both sides are not required. Decoupling components should be provided on both sides, refer to the evaluation board details in the application information section (Figure 42, Table 2 and Figure 44).

Typical Performance

The following plots show typical performance characteristics of CMX90A705 measured on the evaluation board (Part Number EV90A705). Board losses have been de-embedded from the measurement results using TRL calibration.

Test conditions unless otherwise noted

Vd = 27.5 V, Idq = 100 mA, Tc = 25 ˚C and Zo = 50 Ω.

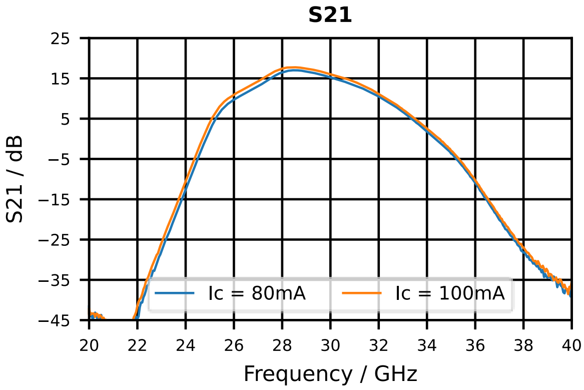


Figure 2 - Small Signal Gain, S21

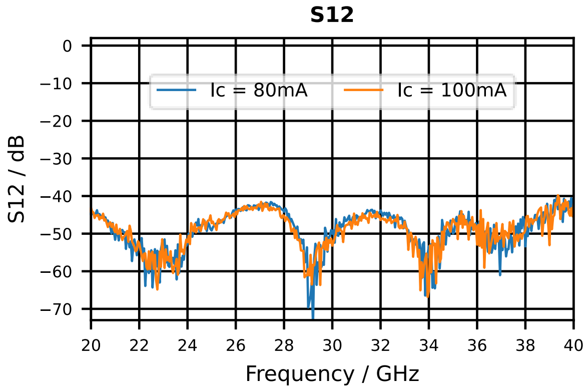


Figure 3 - Reverse Isolation, S12

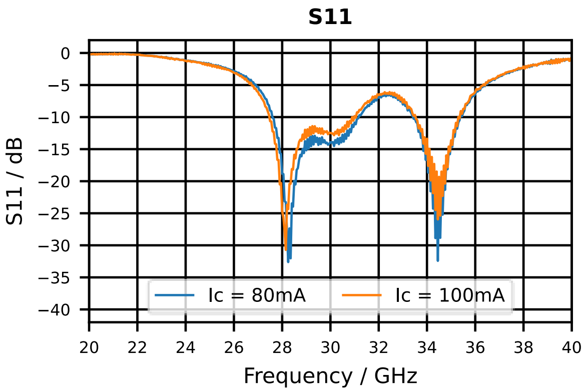


Figure 4 - Input Return Loss, S11

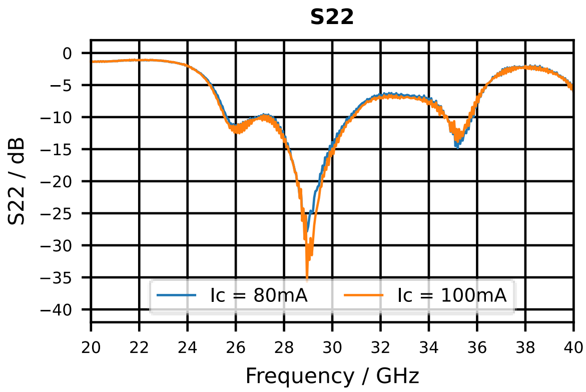


Figure 5 - Output Return Loss, S22

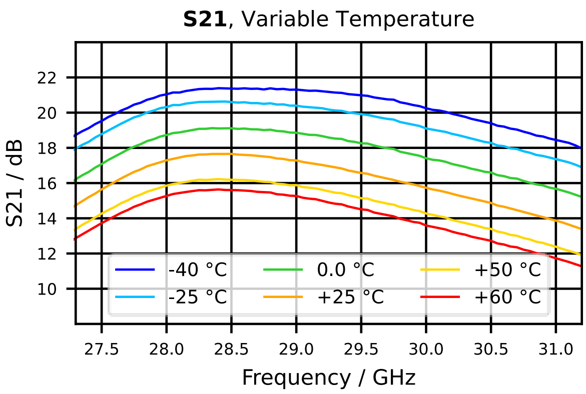


Figure 6 - Small Signal Gain

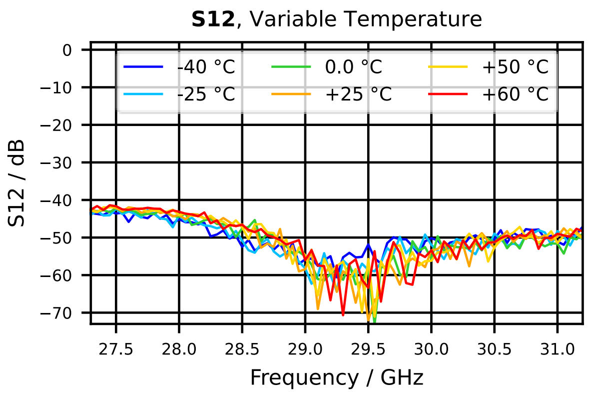


Figure 7 - Reverse Isolation

Test conditions unless otherwise noted

Vd = 27.5 V, Idq = 100 mA, Tc = 25 ˚C and Zo = 50 Ω. Pulse width = 100 µs and duty cycle = 10%.

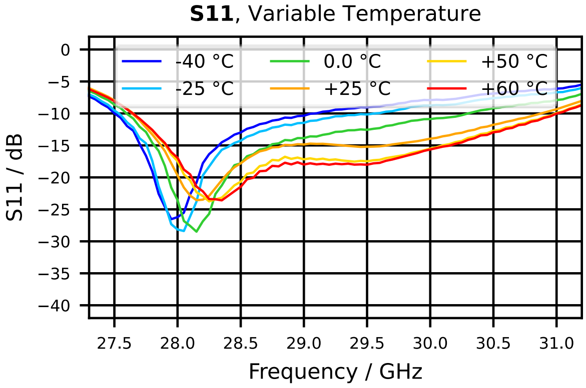


Figure 8 - Input Return Loss

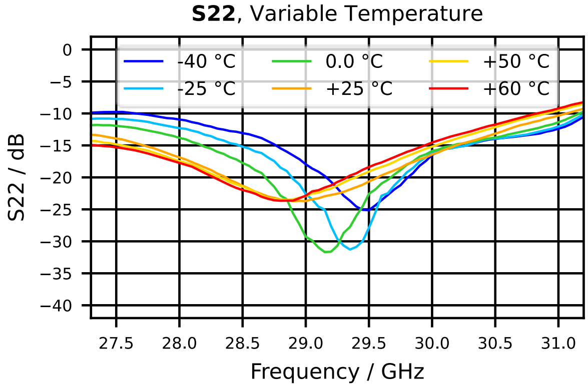


Figure 9 - Output Return Loss

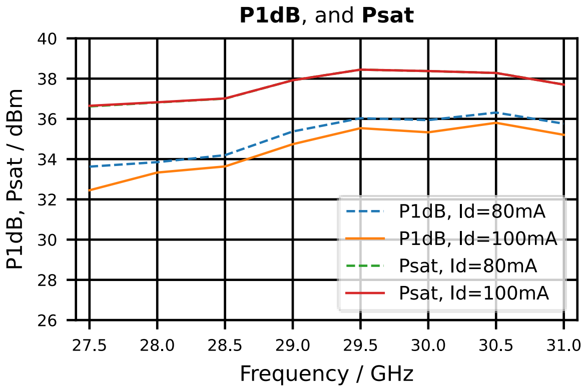


Figure 10 - P1dB and Saturated Power (Psat) vs Frequency and drain current

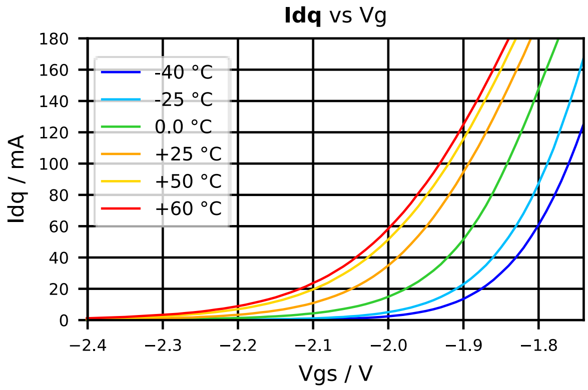


Figure 11 - Quiescent Bias drain current vs gate voltage

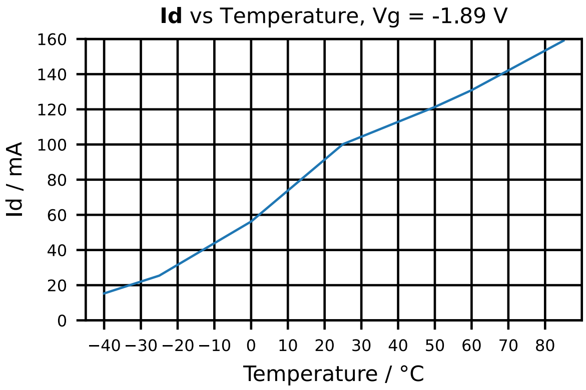


Figure 12 - Drain Current vs temperature at constant gate voltage

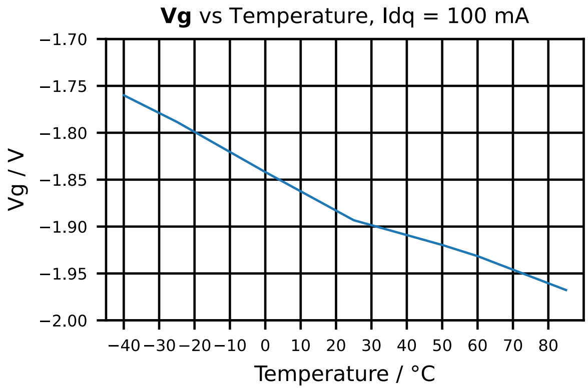


Figure 13 - Gate voltage vs temperature at constant drain current

Test conditions unless otherwise noted

Vd = 27.5 V, Idq = 100 mA, Tc = 25 ˚C and Zo = 50 Ω. Pulse width = 100 µs and duty cycle = 10%.

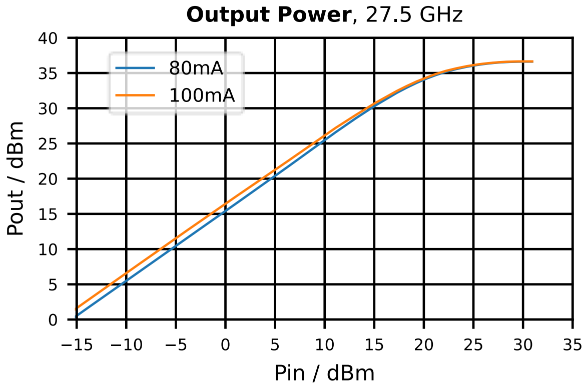


Figure 14 - Pout vs Pin and Idq at 27.5 GHz

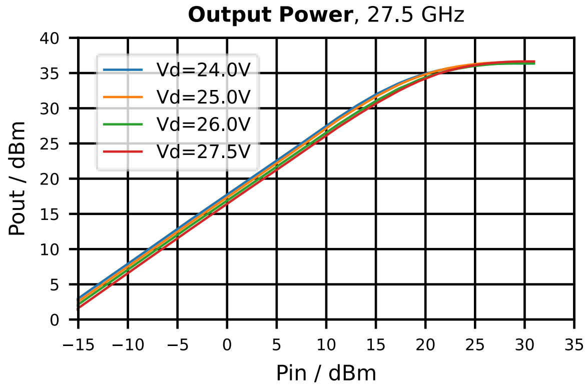


Figure 15 - Pout vs Pin and Vd at 27.5 GHz

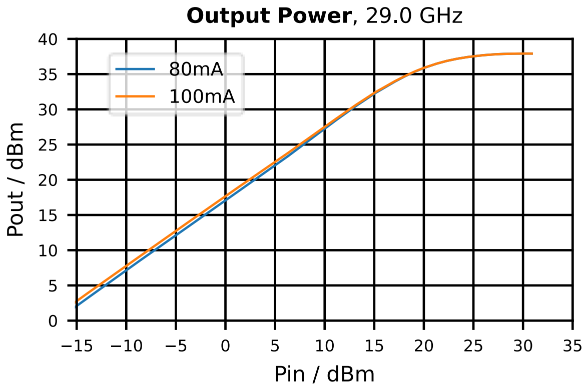


Figure 16 - Pout vs Pin and Idq at 29.0 GHz

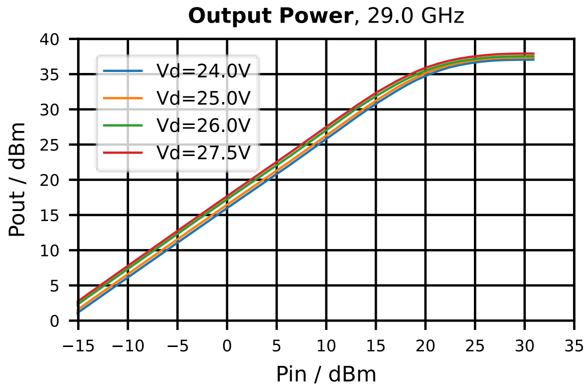


Figure 17 - Pout vs Pin and Vd at 29.0 GHz

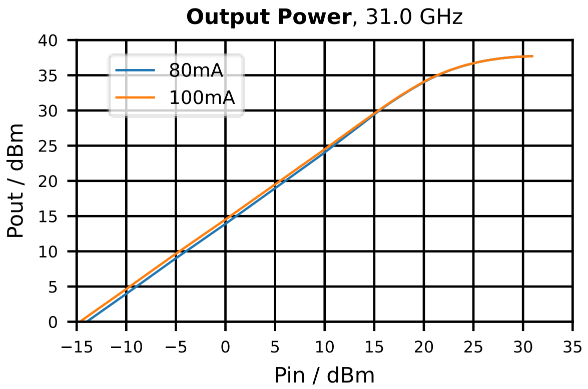


Figure 18 - Pout vs Pin and Idq at 31.0 GHz

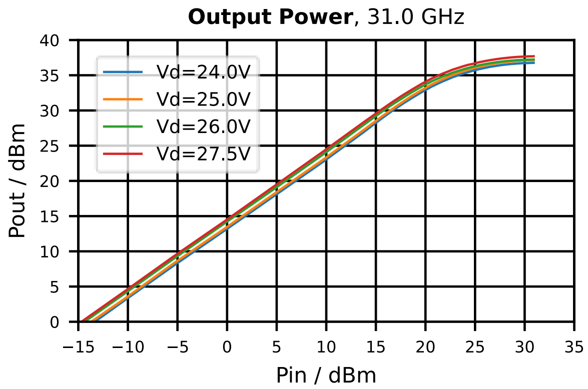


Figure 19 - Pout vs Pin and Vd at 31.0 GHz

Test conditions unless otherwise noted
Vd = 27.5 V, Idq = 100 mA, Tc = 25 ˚C and Zo = 50 Ω. Pulse width = 100 µs and duty cycle = 10%.

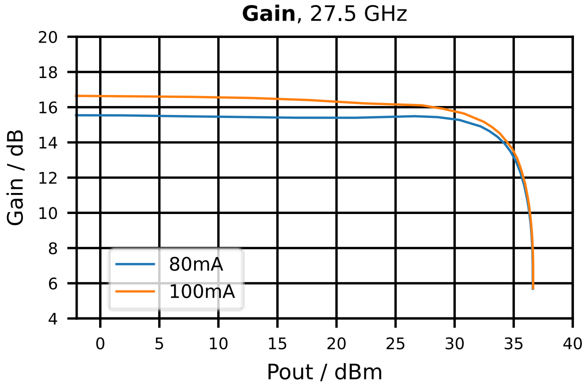


Figure 20 - Gain vs Pout and Idq at 27.5 GHz

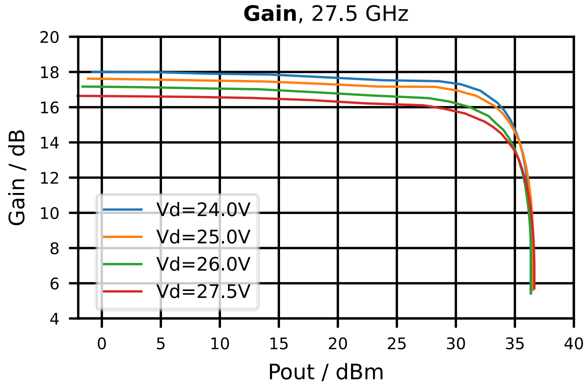


Figure 21 - Gain vs Pout and Vd at 27.5 GHz

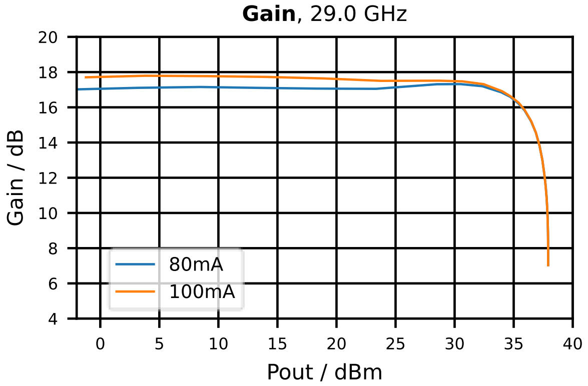


Figure 22 - Gain vs Pout and Idq at 29.0 GHz

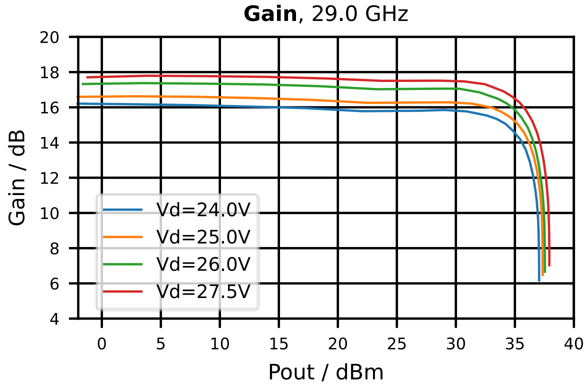


Figure 23 - Gain vs Pout and Vd at 29.0 GHz

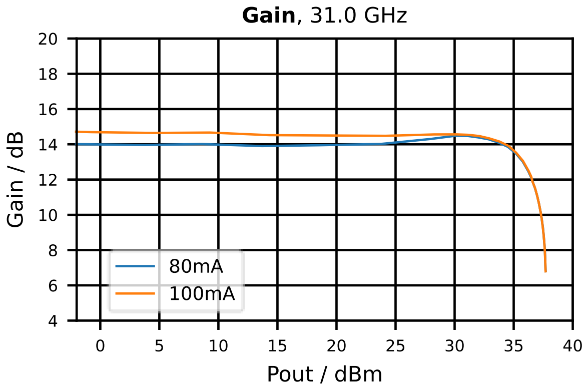


Figure 24 - Gain vs Pout and Idq at 31.0 GHz

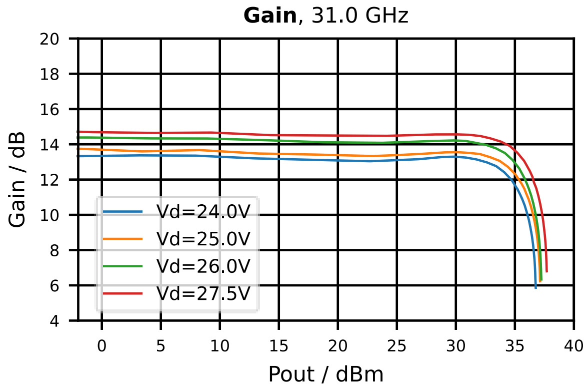


Figure 25 - Gain vs Pout and Vd at 31.0 GHz

Test conditions unless otherwise noted

Vd = 27.5 V, Idq = 100 mA, Tc = 25 ˚C and Zo = 50 Ω. Pulse width = 100 µs and duty cycle = 10%.

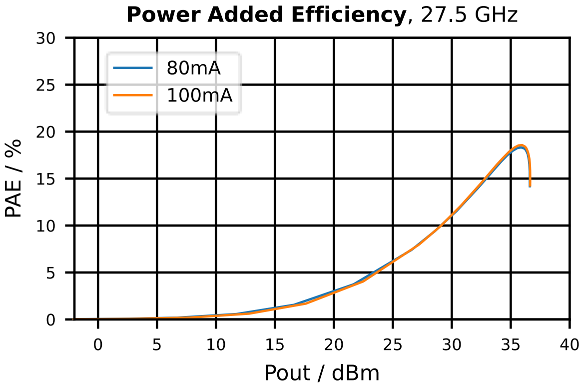


Figure 26 - PAE vs Pout and Idq at 27.5 GHz

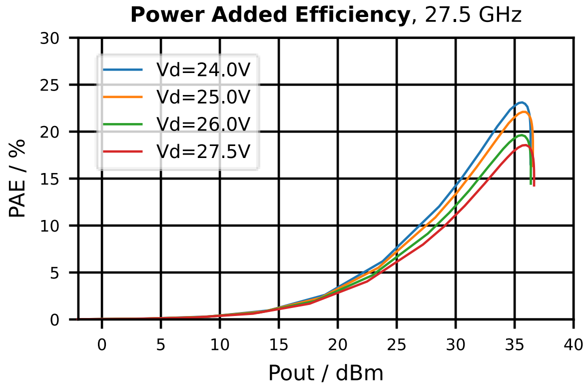


Figure 27 - PAE vs Pout and Vd at 27.5 GHz

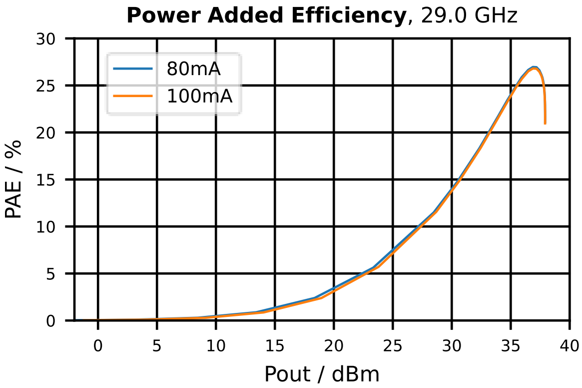


Figure 28 - PAE vs Pout and Idq at 29.0 GHz

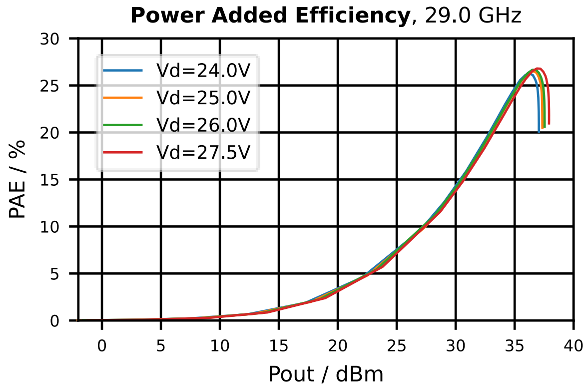


Figure 29 - PAE vs Pout and Vd at 29.0 GHz

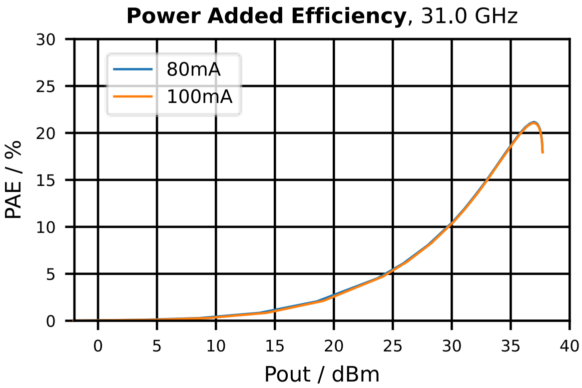


Figure 30 - PAE vs Pout and Idq at 31.0 GHz

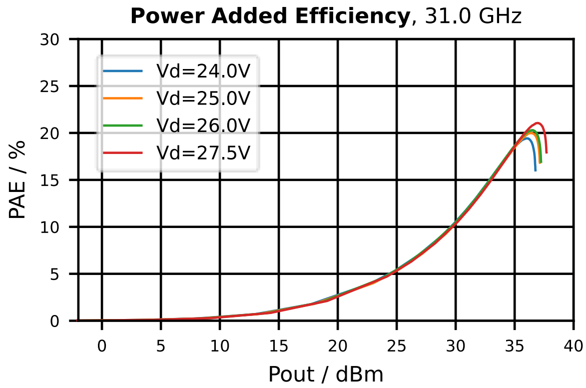


Figure 31 - PAE vs Pout and Vd at 31.0 GHz

Test conditions unless otherwise noted

Vd = 27.5 V, Idq = 100 mA, Tc = 25 ˚C and Zo = 50 Ω. Tone spacing = 100 MHz.

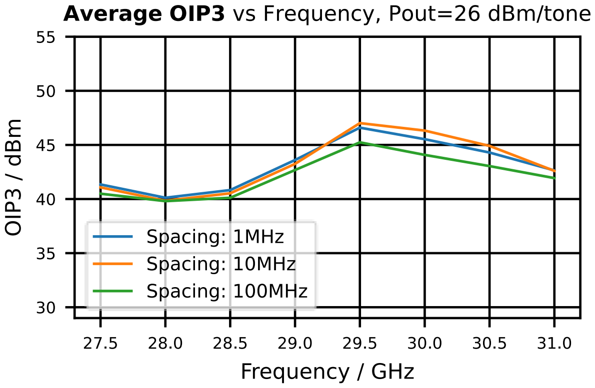


Figure 32 - Average OIP3 vs frequency and Spacing

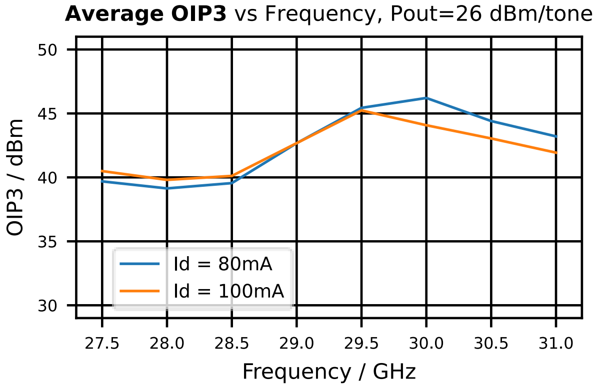


Figure 33 - Average OIP3 vs frequency and Idq Spacing = 100 MHz

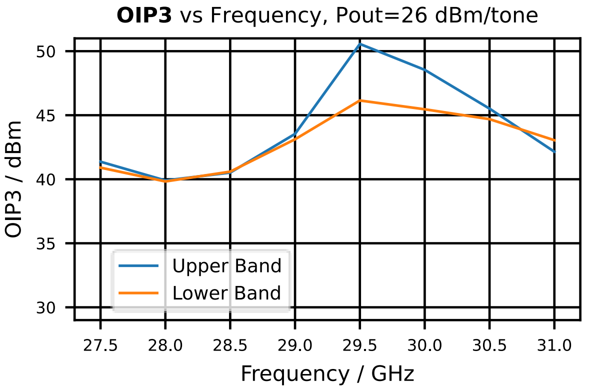


Figure 34 - OIP3 at upper and lower bands Frequency Spacing = 10 MHz

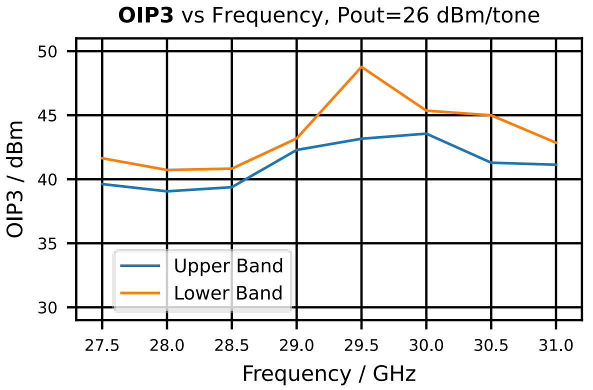


Figure 35 - OIP3 at upper and lower bands Frequency spacing = 100 MHz

Test conditions unless otherwise noted

Vd = 27.5 V, Idq = 100 mA, Tc = 25 ˚C and Zo = 50 Ω. Test signal is modulated with 16-APSK, DVB-S2-9/10, RRC = 0.25, with Symbol Rate = 100 Ms/s. PAPR = 5.53 dB

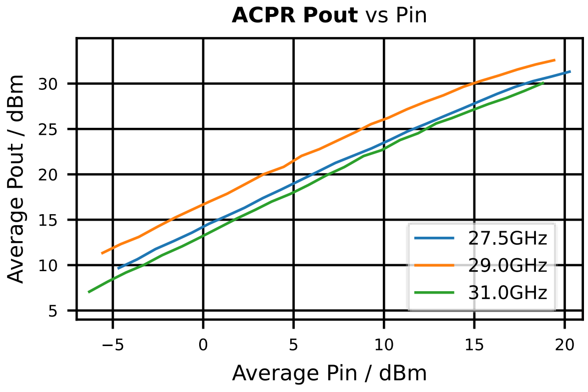


Figure 36 - ACPR average Pout vs Pin vs frequency

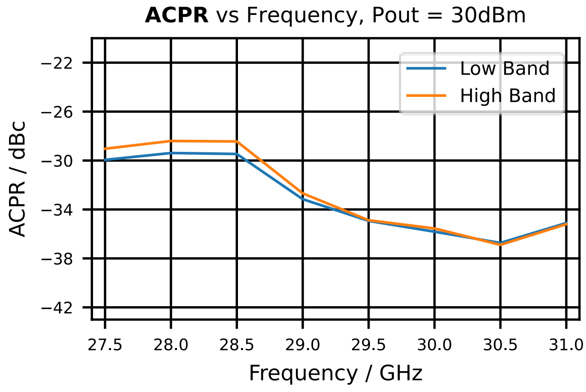


Figure 37 - ACPR of low and high bands vs frequency

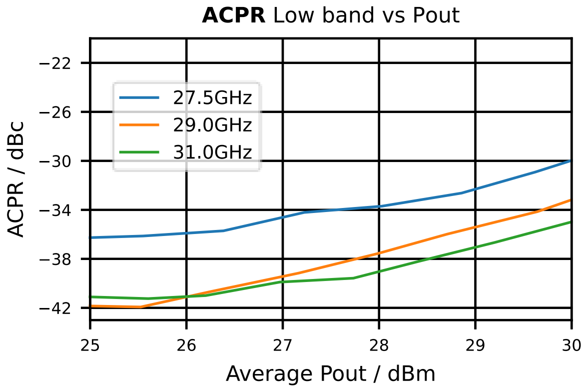


Figure 38 - ACPR at low band vs average Pout

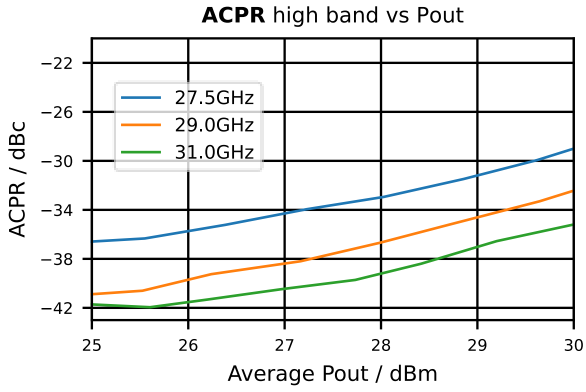


Figure 39 - ACPR at high band vs average Pout

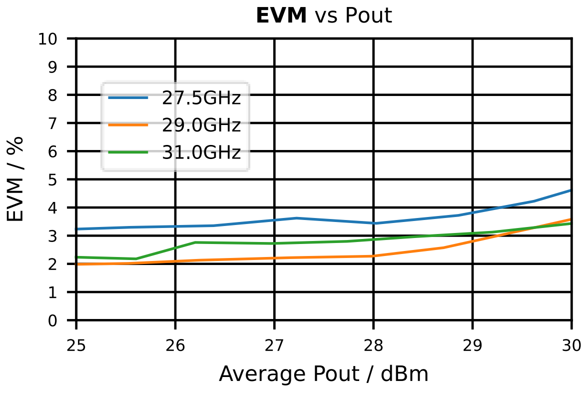


Figure 40 - EVM vs Pout and frequency

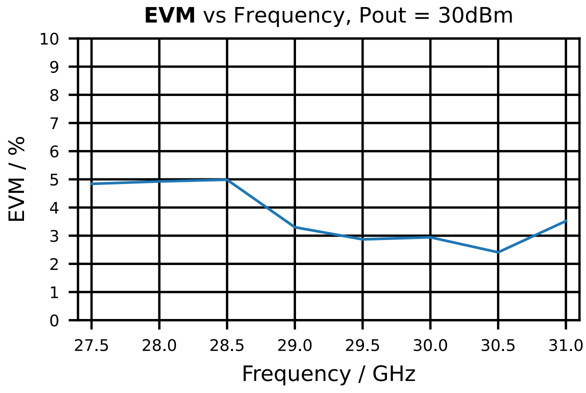


Figure 41 - EVM at average Pout = 30dBm vs frequency

Application Information

Schematic Diagram

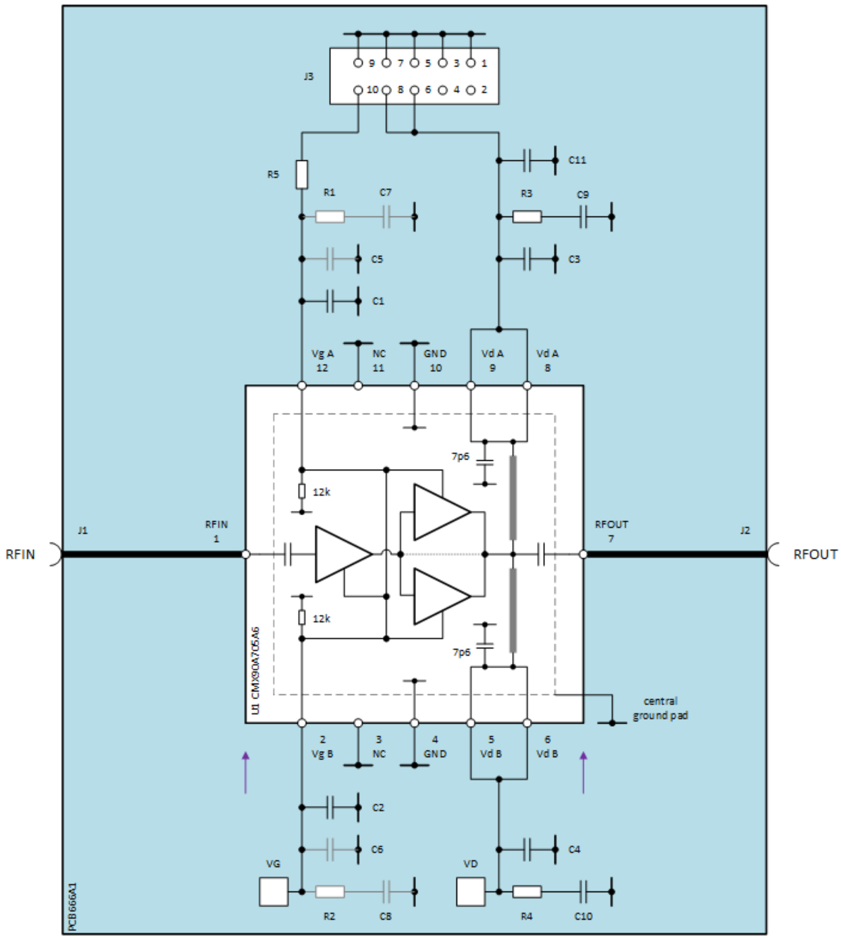


Figure 42 - EV90A705 Schematic

Bill Of Materials (BOM mod state 2)

Table 2 - Bill Of Materials

Reference Designator	Value	Size	Description
C1, C2, C3, C4	1 nF	0402	X7R, 10 %, 50 V
C5, C6	DNF	0402	X7R, 10 %, 50 V
C7, C8	DNF	0402	X7R, 10 %, 50 V
C9, C10	1 µF	0805	XR7, 10 %, 50 V
C11	22 µF	2917	Tant. 10 %, 35 V
R1, R2	DNF	0402	1 %
R3, R4	10 R	0603	1 %
R5	0 R	0402	1 %
J1, J2		2.92 mm	Frontlynk FL38J7-LS502SQA06
J3			Samtec TFM-105-02-L-DH

Notes

- DNF = Do not fit component

J3 should be used with Samtec SFSD-05 sockets. Pre-made cable assemblies can be purchased e.g. SFSD-05-28-H-10.00-SR.

PCB Layout

Careful layout of the printed circuit board (PCB) is essential for optimum RF and thermal performance. The recommended layout, including ground via pattern underneath the device, may be taken from the evaluation board (Part Number EV90A705).

The PCB is a single layer of Isola I-TERA MT40, 8 thou thickness with ½ oz copper mounted to an aluminium carrier which provides rigidity and thermal dissipation (Figure 43) and the EV90A705 PCB666A1 (Figure 44) is 26 mm x 50 mm. The CMX90A705 has integrated DC blocking capacitors on the input and output.

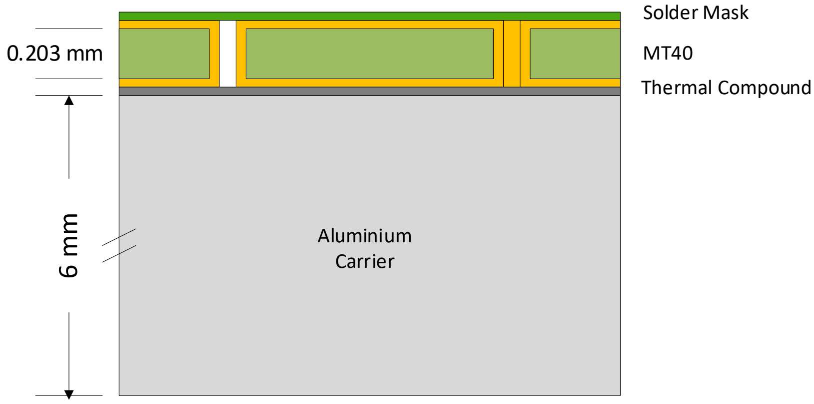


Figure 43 - EV90A705 Layer Stack

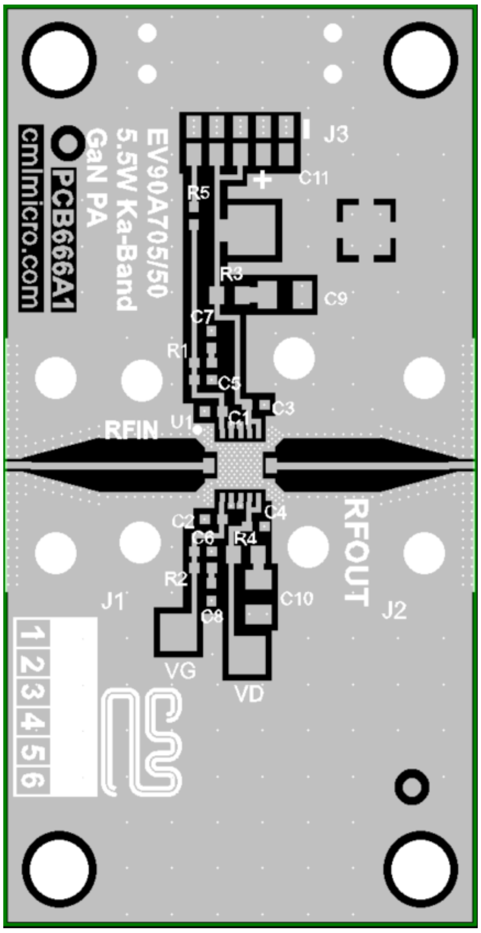


Figure 44 - EV90A705 PCB Top Layer View

Thermal Design

The primary RF/DC ground and thermal path is via the exposed ground pad on the backside of the package, which must be connected to the PCB ground plane. An array of plated through-hole vias directly underneath the die pad area is essential to conduct heat away and minimise ground inductance. EV90A705 has 94 x 0.15 mm, copper filled grounding vias connecting the top layer to the bottom layer in the central square region. 3 x 11 and 1 x 9 similar vias connect the four corner ground areas, providing further heat removal and lower inductance.

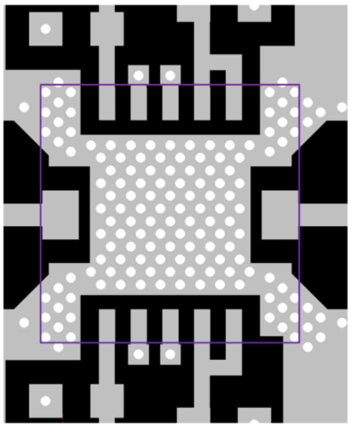


Figure 45 - EV90A705 Ground Vias

The device junction temperature (Tj) can be calculated using Tj = Tc + (Pdiss x Rjc) where Pdiss = Pdc + Pin – Pout and Tc is the case temperature on the backside of the package (central ground pad) in contact with the PCB.

The four holes in the EV90A705 corners should be used to mount the evaluation board/carrier to a heatsink using thermal compound. The heatsink and any fan should be chosen to ensure sufficient cooling under ambient conditions.

Bias Procedure

The CMX90A705 is a two-stage depletion mode GaN amplifier and therefore careful sequencing of the drain (Vd) and gate (Vg) supplies is critical and the following power-up and down sequence must be followed.

Power-up:

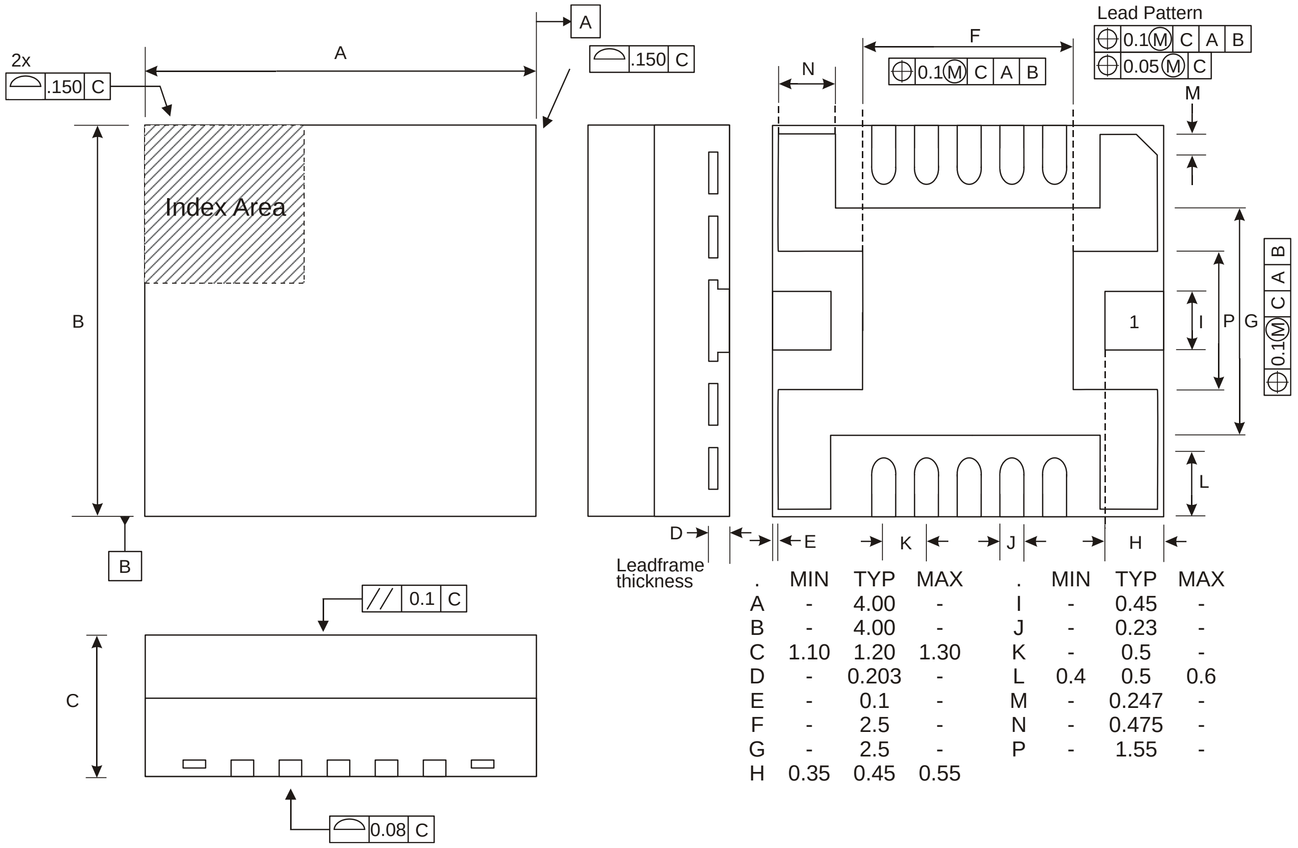
- Connect the amplifier in a suitable 50 Ω environment, with no RF input.
- Switch on the gate supply and set the gate voltage (Vg) to -5V.
- Apply the drain (Vd) voltage (typically +27.5 V).
- Increase Vg to set Id to 100 mA (Vg typically -1.89 V).
- A suitable RF input can now be applied.

Power-down:

- Turn off the applied RF input.
- Decrease the gate voltage to -5V.
- Switch off the drain supply.
- Switch off the gate supply.

Package Outline

12-lead 4x4 mm AQFN Package (A6)

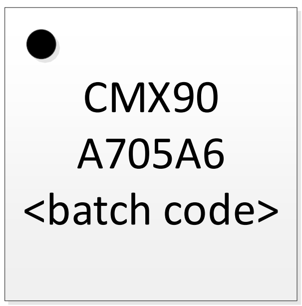


.	MIN	TYP	MAX	.	MIN	TYP	MAX
A	-	4.00	-	I	-	0.45	-
B	-	4.00	-	J	-	0.23	-
C	1.10	1.20	1.30	K	-	0.5	-
D	-	0.203	-	L	0.4	0.5	0.6
E	-	0.1	-	M	-	0.247	-
F	-	2.5	-	N	-	0.475	-
G	-	2.5	-	P	-	1.55	-
H	0.35	0.45	0.55				

Figure 46 - Package Outline

Package Marking

Pin 1 indicator (dot) and 3 rows of text for device identification.



Line 1: CMX90 SµRF series

Line 2: 6-character part code

Line 3: Batch code

Revision History

Issue	Description	Date
1.0	First Approved datasheet	24th May 2024

Contact Information

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