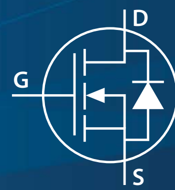
EPC2204 – Enhancement Mode Power Transistor

V_{DS} , 100 V
$R_{DS(on)}$, 6 mΩ
I_D , 29 A



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Revised November 26, 2024

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5–5.25 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: Ask a GaN Expert

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
$V_{DS(tr)}$	Drain-to-Source Voltage (Repetitive Transient)(1)	120	
I_D	Continuous (T_A = 25°C)	29	A
	Pulsed (25°C, T_{PULSE} = 10 µs)	167	
	Pulsed (125°C, T_{PULSE} = 10 µs)	134	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

(1) Pulsed repetitively, duty cycle factor (DC_{Factor}) ≤ 1%;
See Figure 13 and Reliability Report Phase 16, Section 3.2.6

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{θJC}$	Thermal Resistance, Junction-to-Case	1	°C/W
$R_{θJB}$	Thermal Resistance, Junction-to-Board	2.5	
$R_{θJA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	64	

Note 1: $R_{θJA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.25 mA	100			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 80 V		0.04	0.2	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	1.3	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.3	6.7	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.03	0.2	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 4 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 16 A		4.4	6	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.6		V

Defined by design. Not subject to production test.

Die Size: 2.5 x 1.5 mm

EPC2204 eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- DC-DC Converters
- Isolated DC-DC Converters
- Lidar
- Sync rectification for AC-DC and DC-DC
- Point of Load Converters
- USB-C
- Class-D Audio
- LED Lighting
- eMobility

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2204

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V		644	851	pF
C_{RSS}	Reverse Transfer Capacitance			2.3		
C_{OSS}	Output Capacitance			304	456	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 50 V, V_{GS} = 0 V		401		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			501		
R_G	Gate Resistance			0.4		Ω
Q_G	Total Gate Charge	V_{DS} = 50 V, V_{GS} = 5 V, I_D = 16 A		5.7	7.4	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 50 V, I_D = 16 A		1.8		
Q_{GD}	Gate-to-Drain Charge			0.8		
$Q_{G(TH)}$	Gate Charge at Threshold			1		
Q_{OSS}	Output Charge	V_{DS} = 50 V, V_{GS} = 0 V		25	38	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
All measurements were done with substrate connected to source.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C*

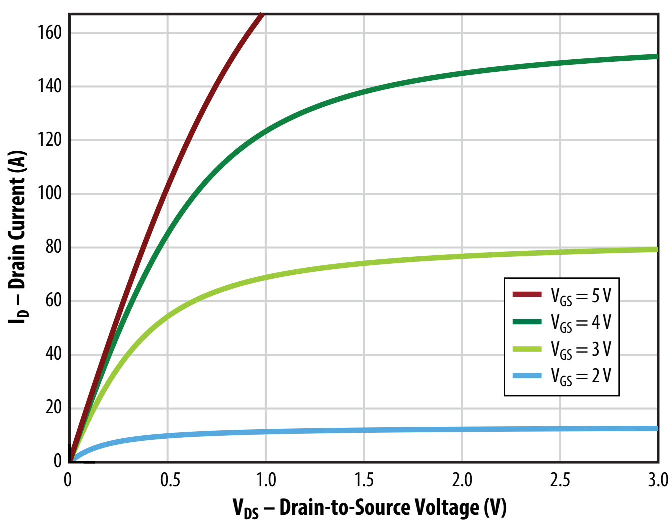


Figure 2: Typical Transfer Characteristics*

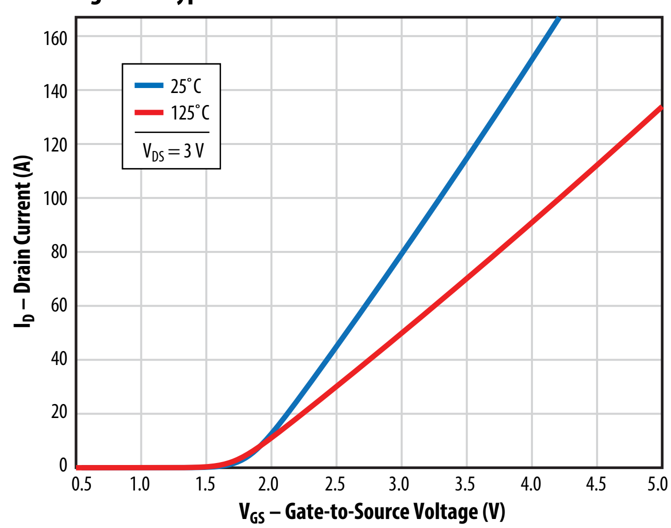


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

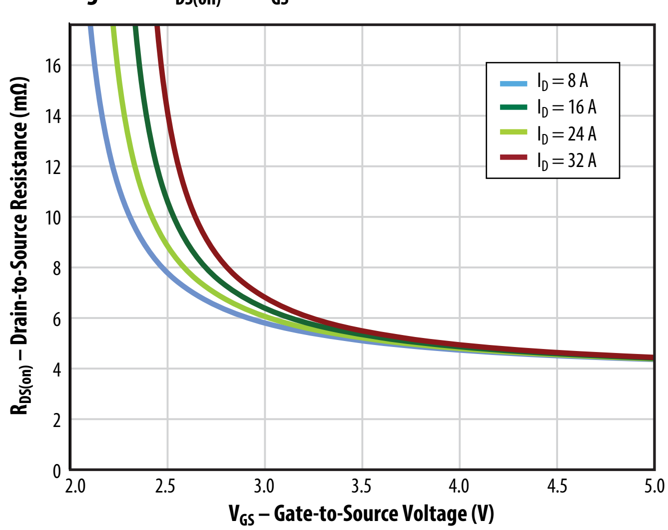
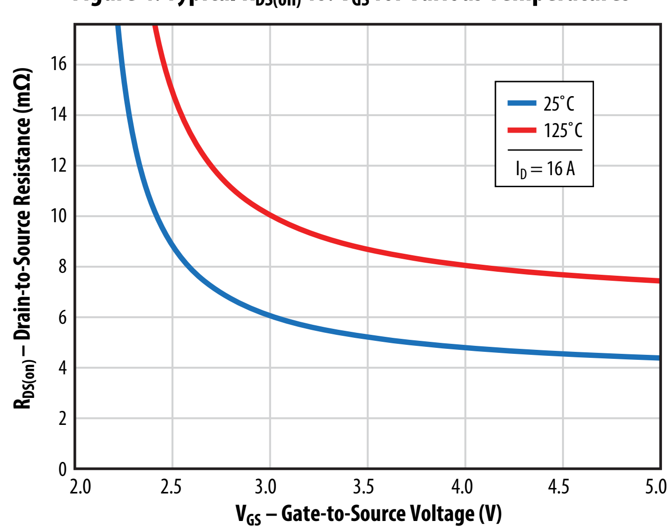


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures



* Generated based on a pulse width of 300 µs.

Figure 5a: Typical Capacitance (Linear Scale)

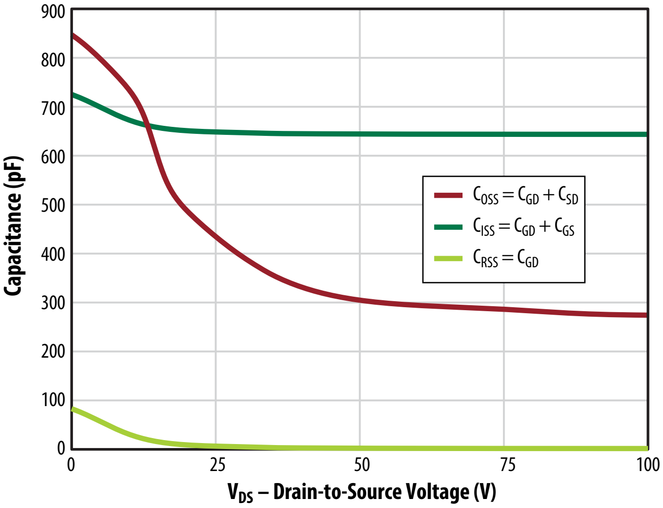


Figure 5b: Typical Capacitance (Log Scale)

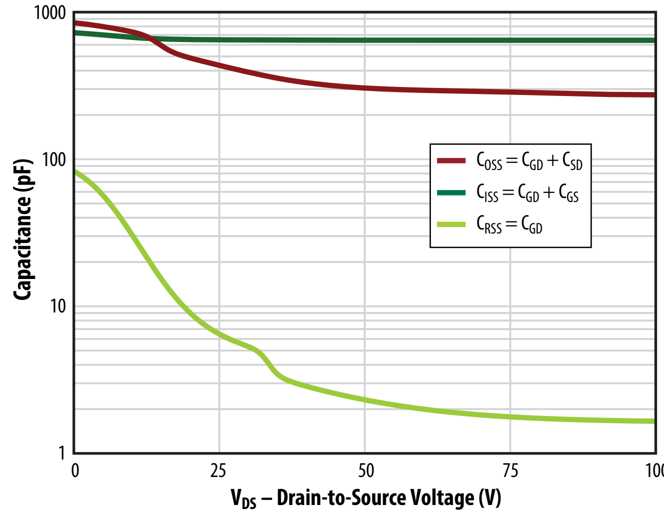


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

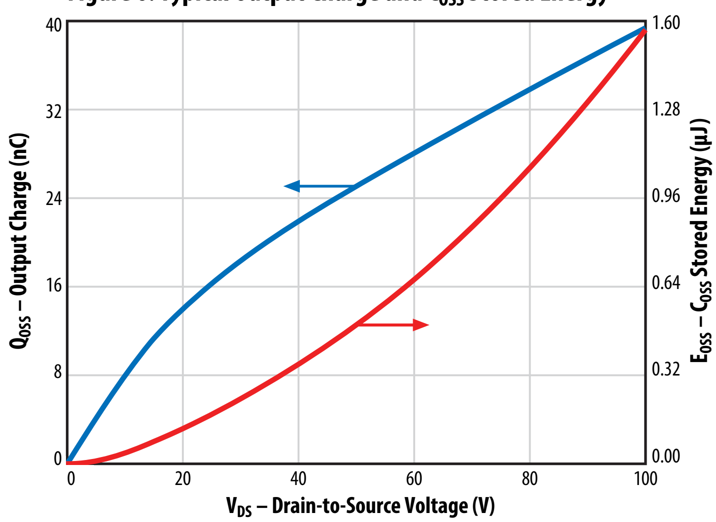


Figure 7: Typical Gate Charge

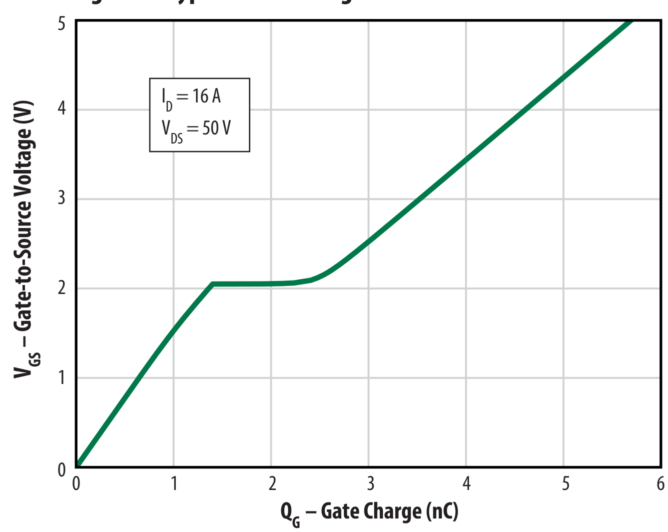
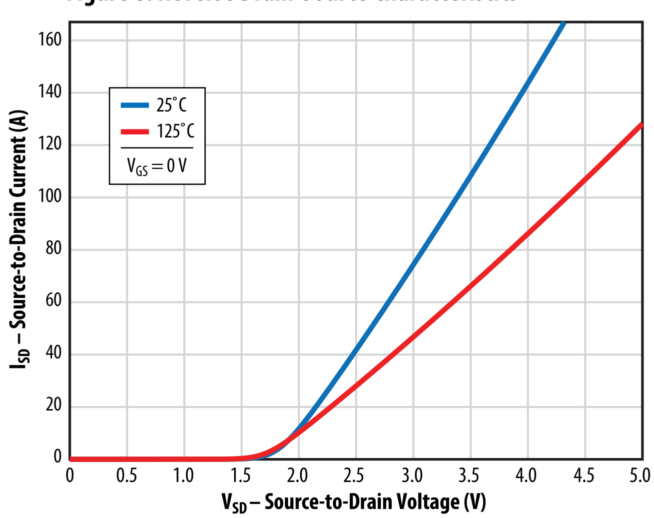


Figure 8: Reverse Drain-Source Characteristics*



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

* Generated based on a pulse width of 300 µs.

Figure 9: Normalized On-State Resistance vs. Temperature

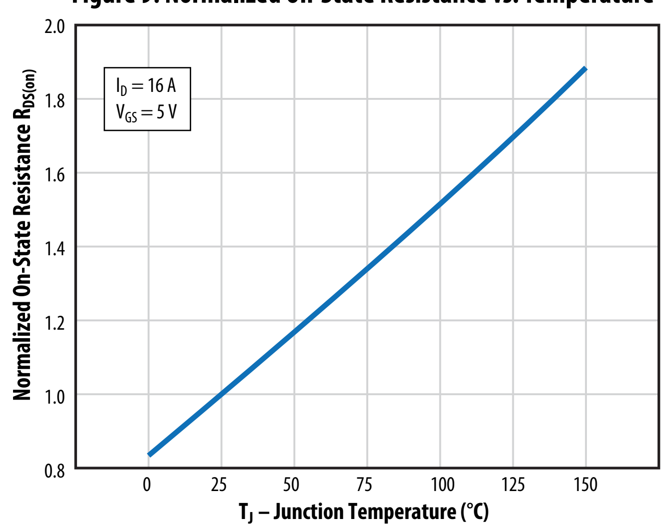


Figure 10: Normalized Threshold Voltage vs. Temperature

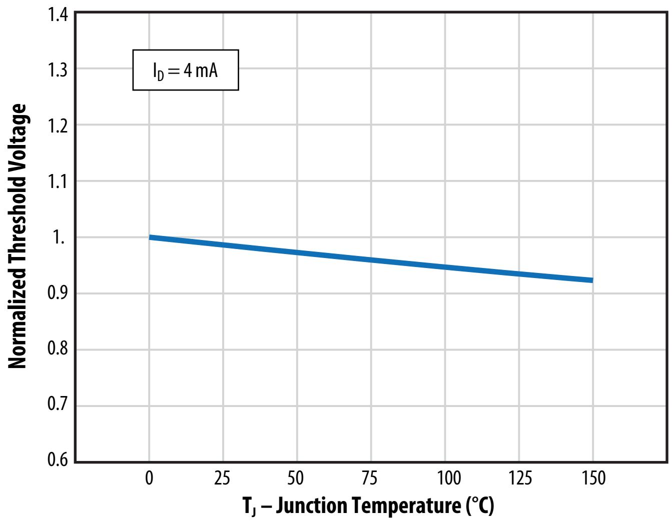
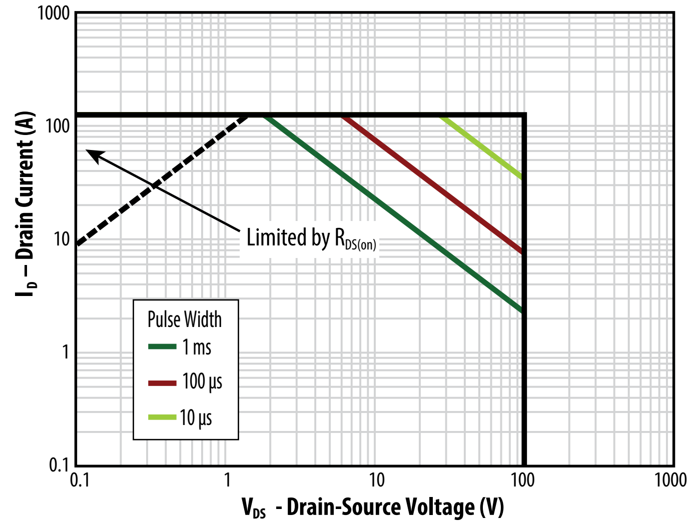


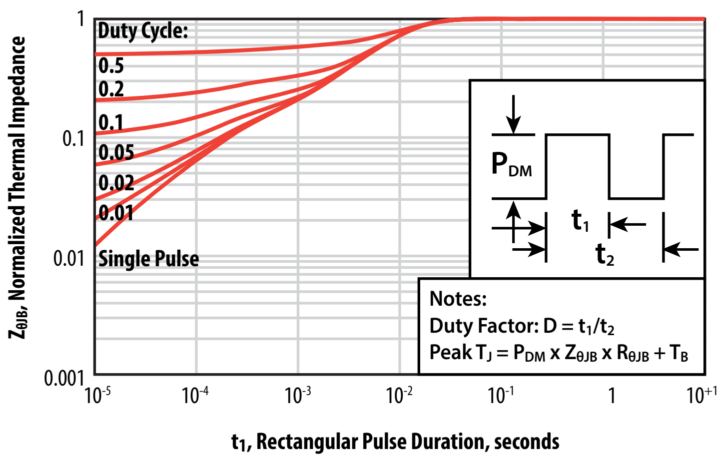
Figure 11: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

Figure 12: Transient Thermal Response Curves

Junction-to-Board



Junction-to-Case

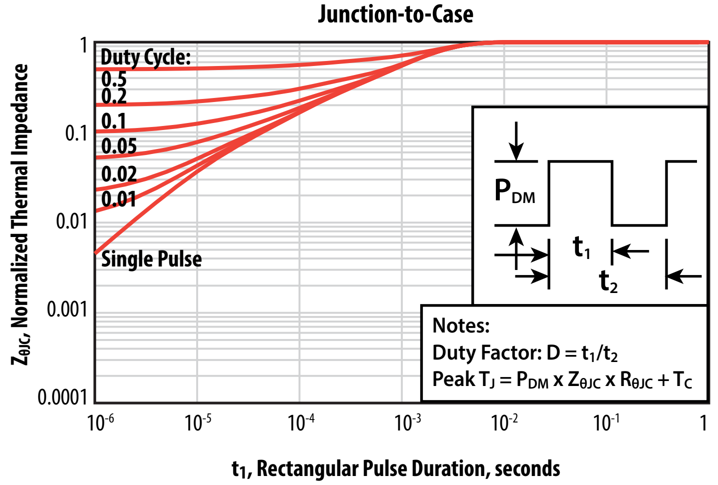
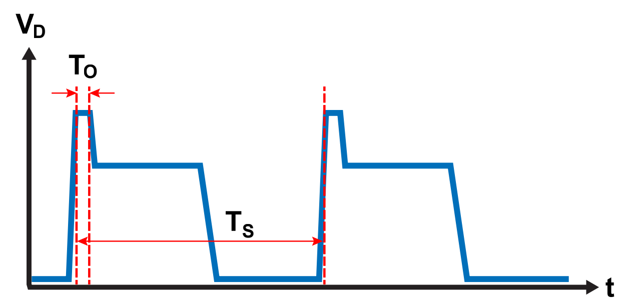


Figure 13: Duty Cycle Factor (DC_{Factor}) Illustration for Repetitive Overvoltage Specification

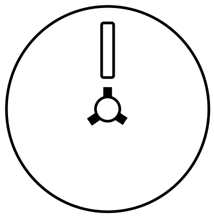


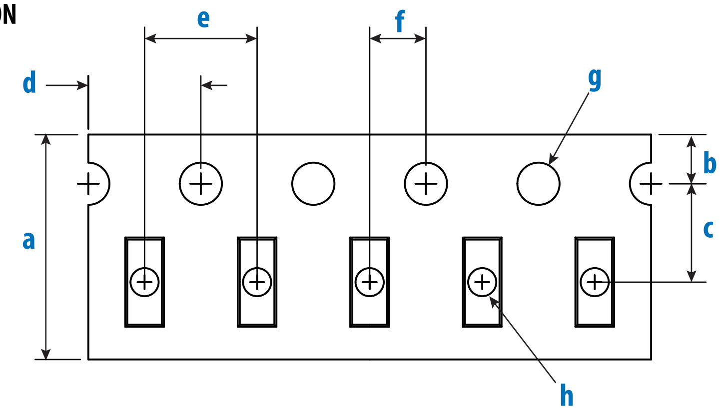
1% is the ratio between T_O (overvoltage duration) and T_S (one switching period).

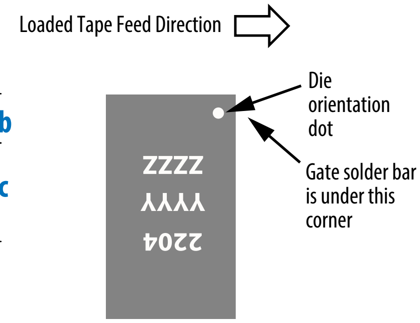
TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel

7" inch reel







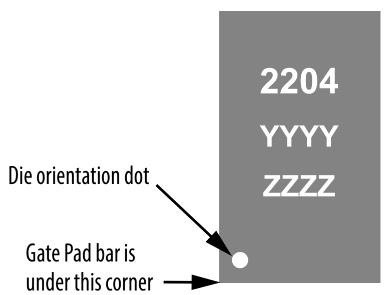
Die is placed into pocket solder bar side down (face side down)

EPC2204 (Note 1)	Dimension (mm) Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	0.50	0.45	0.55

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

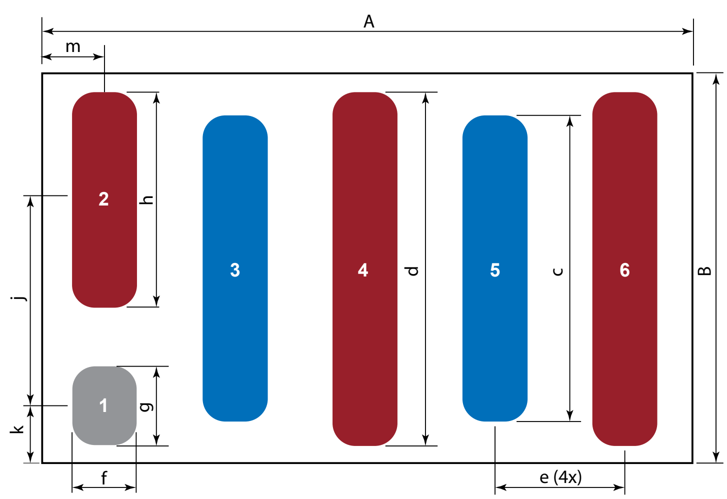
DIE MARKINGS



Part Number	Laser Markings: Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2204	2204	YYYY	ZZZZ

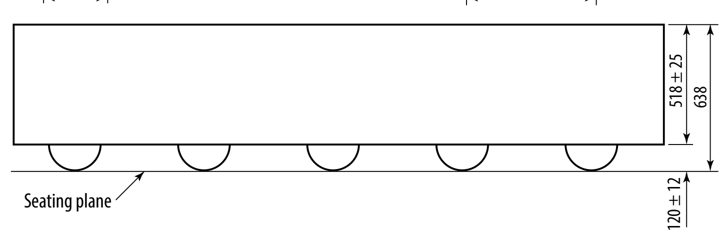
DIE OUTLINE

Solder Bump View



DIM	Micrometers MIN	Nominal	MAX
A	2470	2500	2530
B	1470	1500	1530
c	1155	1175	1195
d	1330	1350	1370
e		500	
f	230	250	270
g	280	300	320
h	805	825	845
j		787.5	
k	209	225	
m	234	250	

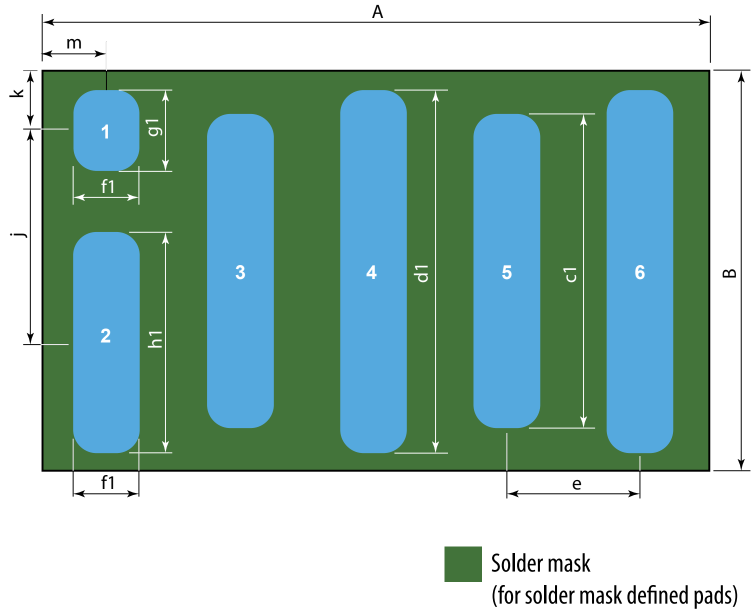
Side View



Pad 1 is Gate;
Pads 2 ,4, 6 are Source;
Pads 3, 5 are Drain

Note: Dimensions **d** and **c** are centered

RECOMMENDED LAND PATTERN
(units in µm)

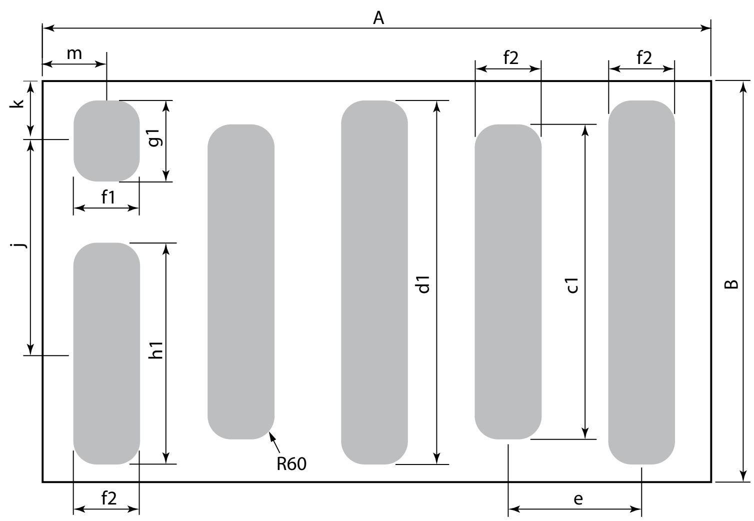


Land pattern is solder mask defined

DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
g1	280
h1	805
j	787.5
k	225
m	250

Pad 1 is Gate;
Pads 2 ,4, 6 are Source;
Pads 3, 5 are Drain

RECOMMENDED STENCIL DRAWING
(units in µm)



DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
f2	210
g1	280
h1	805
j	787.5
k	225
m	250

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

LAYOUT CONSIDERATIONS

GaN transistors generally behave like power MOSFETs, but at much higher switching speeds and power densities, therefore layout considerations are very important, and care must be taken to minimize layout parasitic inductances. The recommended design utilizes the first inner layer as a power loop return path. This return path is located directly beneath the top layer's power loop allowing for the smallest physical loop size. This method is also commonly referred to as flux cancellation. Variations of this concept can be implemented by placing the bus capacitors either next to the high side device, next to the low side device, or between the low and high side devices, but in all cases the loop is closed using the first inner layer right beneath the devices.

A similar concept is also used for the gate loop, with the return gate loop located directly under the turn ON and OFF gate resistors.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other, and a via next to the source pad closest to the gate pad is used as Kelvin connection for the gate driver return path.

The **EPC9097 Half-Bridge Development Board Using EPC2204** implements our recommended vertical inner layout.

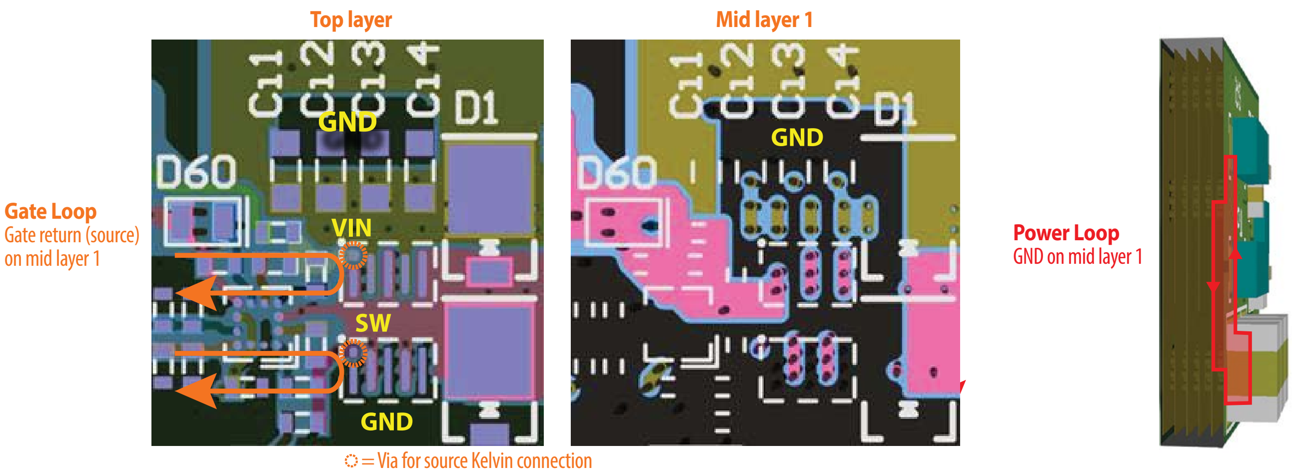


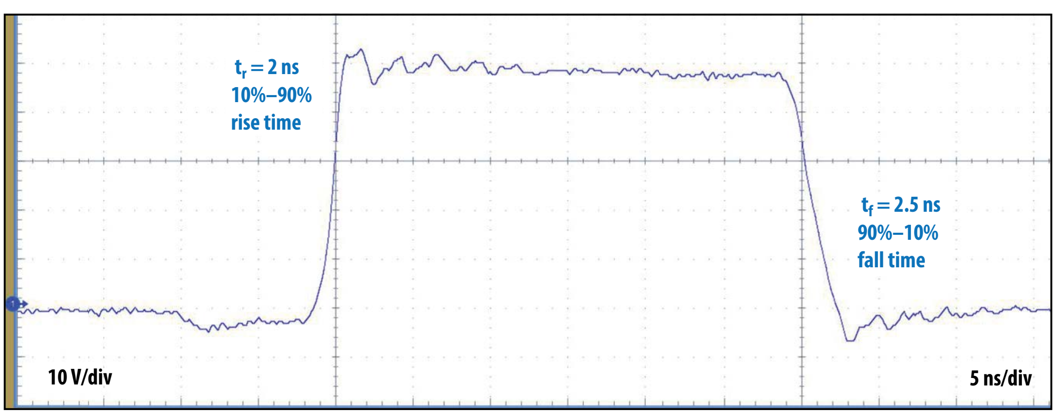
Figure 13: Inner vertical layout for power and gate loops from EPC9097

Detailed recommendations on layout can be found on EPC's website: **Optimizing PCB Layout with eGaN FETs.pdf**

TYPICAL SWITCHING BEHAVIOR

The following typical switching waveforms are captured in these conditions:

- **EPC9097 Half-Bridge Development Board Using EPC2204**
- Gate driver: uP1966E with 0.4 Ω/0.7 Ω pull-down/pull-up resistance
- External R_G(ON) = 1 Ω, R_G(OFF) = 0 Ω
- V_{IN} = 48 V, I_L = 25 A



V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 10 A, f_{sw} = 500 kHz, L = 2.2 µH

Figure 14: Typical half-bridge voltage switching waveforms

See the **EPC9097 Quick Start Guide (QSG)** for more information.

TYPICAL THERMAL CONCEPT

The EPC2204 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. ***Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.***

Recommended best practice thermal solutions are covered in detail in **How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf**.

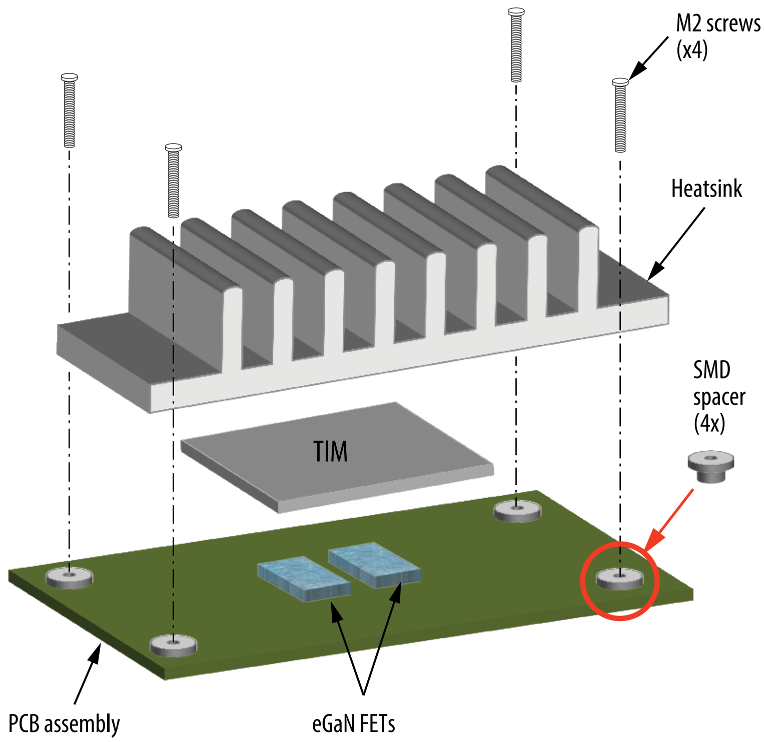


Figure 15: Exploded view of heatsink assembly using screws

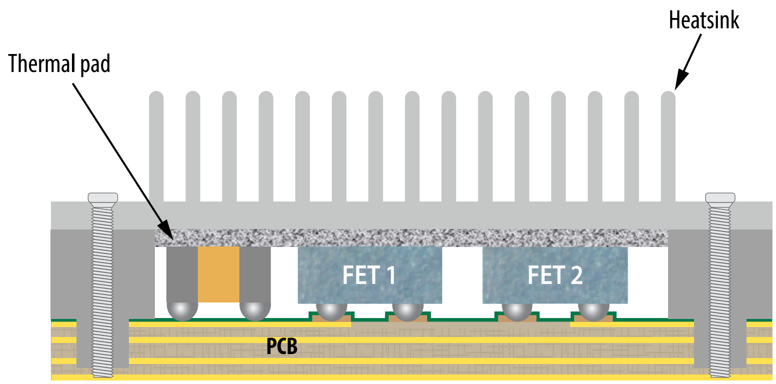


Figure 16: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the ***GaN FET Thermal Calculator*** on EPC's website.

Solder mask defined pads are recommended for best reliability.

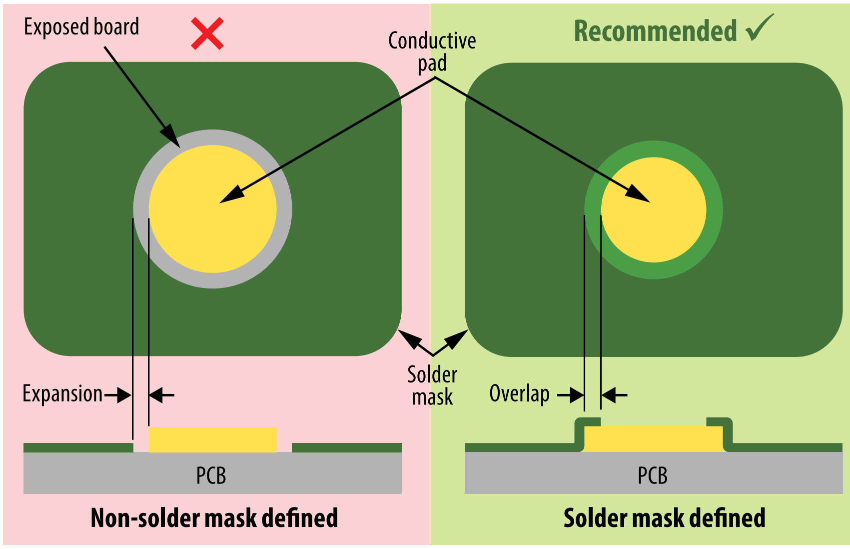


Figure 17: Solder mask defined versus non-solder mask defined pad

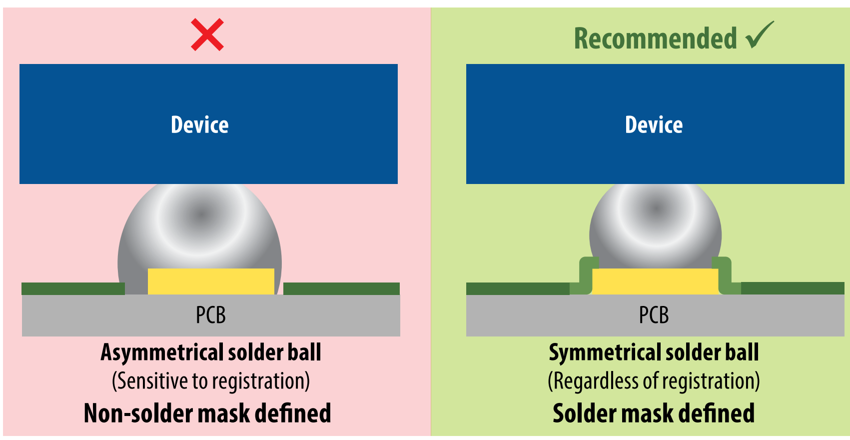


Figure 18: Effect of solder mask design on the solder ball symmetry

- Assembly resources – **https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf**
- Library of Altium footprints for production FETs and ICs – **https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip** (for preliminary device Altium footprints, contact EPC)