

EPC2204A – Automotive 80 V (D-S) Enhancement Mode Power Transistor

 $V_{DS}, 80\text{ V}$
 $R_{DS(on)}, 6\text{ m}\Omega\text{ max}$
 $I_D, 29\text{ A}$

AEC-Q101



Halogen-Free

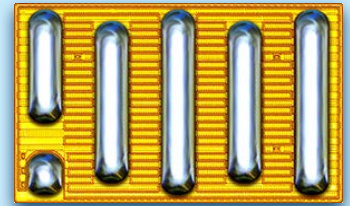
Revised November 27, 2024

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$ while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:



Die Size: 2.5 x 1.5 mm

EPC2204A eGaN® FETs are supplied only in passivated die form with solder bars.

Applications

- DC-DC Converters
- Isolated DC-DC Converters
- Automotive Lidar/ToF
- Sync rectification for AC-DC and DC-DC
- Point of Load Converters
- USB-C
- Class-D Audio
- LED Lighting
- eMobility

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	80	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	96	
I_D	Continuous ($T_A = 25^\circ\text{C}$)	29	A
	Pulsed (25°C, $T_{PULSE} = 10\ \mu\text{s}$)	167	
	Pulsed (125°C, $T_{PULSE} = 10\ \mu\text{s}$)	134	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	2.5	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	64	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 0.2\text{ mA}$	80			V
I_{DSS}	Drain-Source Leakage	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$		0.04	0.2	mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 6\text{ V}$		0.01	1.3	
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 6\text{ V}, T_J = 125^\circ\text{C}$		0.3	6.7	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.03	0.2	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 4\text{ mA}$	0.7	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 16\text{ A}$		4.4	6	mΩ
V_{SD}	Source-Drain Forward Voltage [#]	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$		1.6		V

[#] Defined by design. Not subject to production test.

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2204A>

Dynamic Characteristics[#] (T_J = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V		644	851	pF
C _{RSS}	Reverse Transfer Capacitance			2.3		
C _{OSS}	Output Capacitance			304	456	
C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 2)	V _{DS} = 0 to 50 V, V _{GS} = 0 V		401		
C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 3)			501		
R _G	Gate Resistance			0.4		Ω
Q _G	Total Gate Charge	V _{DS} = 50 V, V _{GS} = 5 V, I _D = 16 A		5.7	7.4	nC
Q _{GS}	Gate-to-Source Charge	V _{DS} = 50 V, I _D = 16 A		1.8		
Q _{GD}	Gate-to-Drain Charge			0.8		
Q _{G(TH)}	Gate Charge at Threshold			1		
Q _{OSS}	Output Charge	V _{DS} = 50 V, V _{GS} = 0 V		25	38	
Q _{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.

All measurements were done with substrate connected to source.

Note 2: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Note 3: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C*

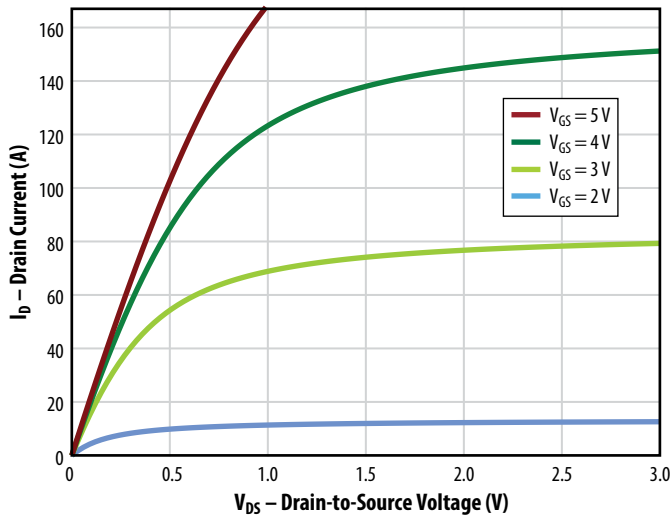


Figure 2: Typical Transfer Characteristics*

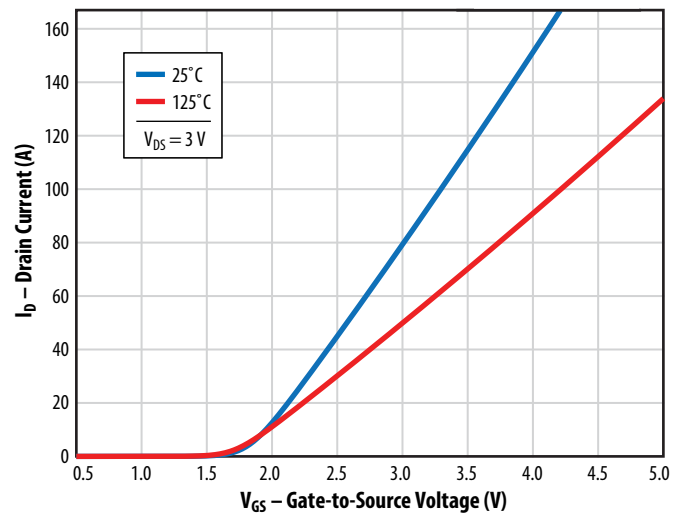


Figure 3: R_{DS(on)} vs. V_{GS} for Various Drain Currents

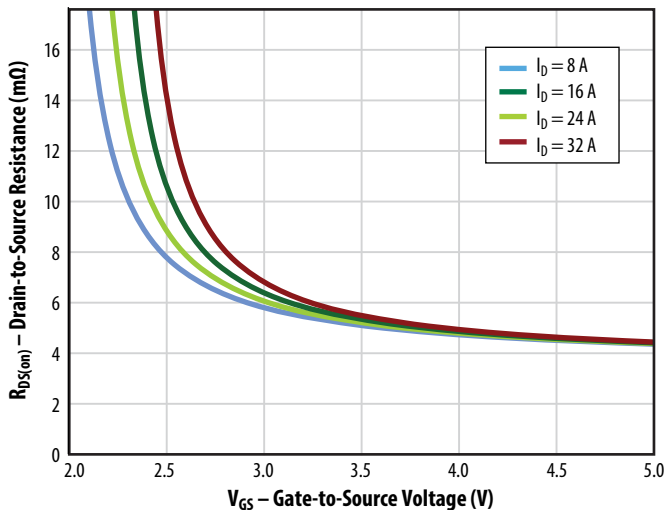
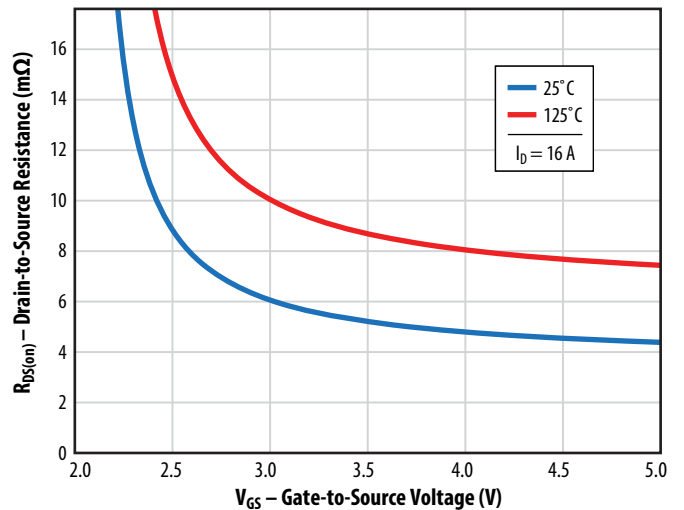


Figure 4: Typical R_{DS(on)} vs. V_{GS} for Various Temperatures



* Generated based on a pulse width of 300 μs.

Figure 5a: Typical Capacitance (Linear Scale)

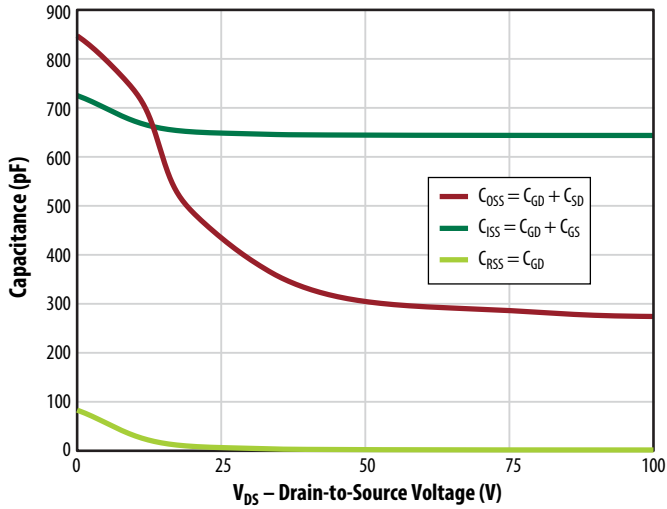


Figure 5b: Typical Capacitance (Log Scale)

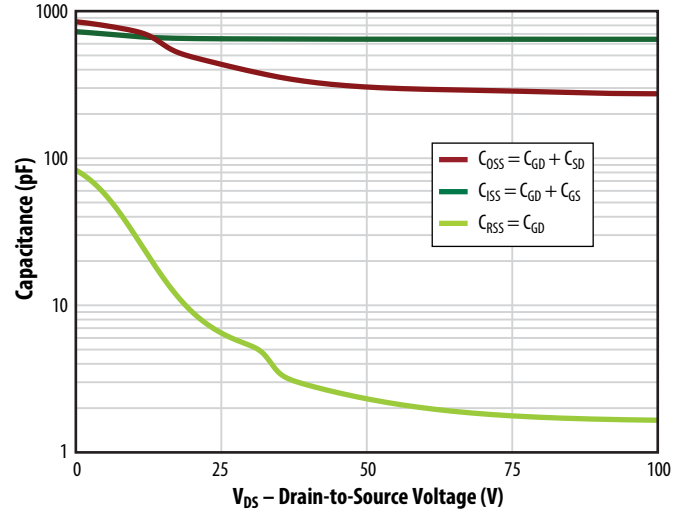


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

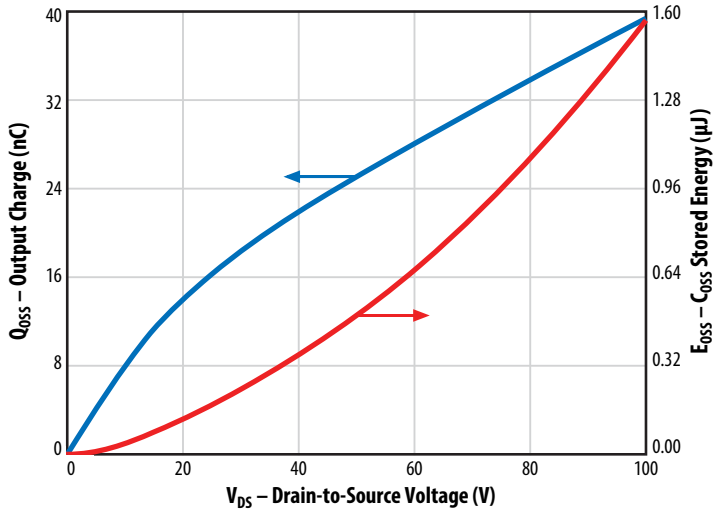


Figure 7: Typical Gate Charge

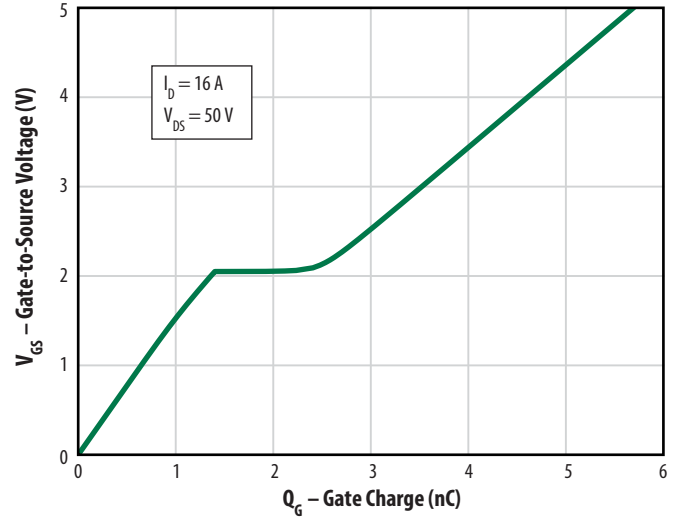


Figure 8: Typical Reverse Drain-Source Characteristics*

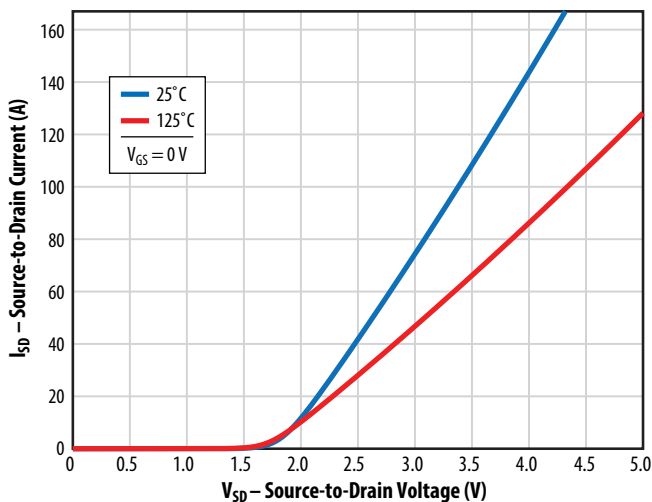
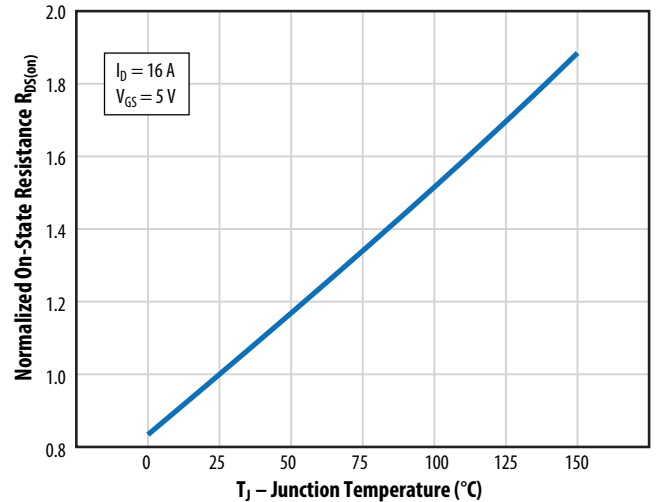


Figure 9: Typical Normalized On-State Resistance vs. Temp.



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0 V for OFF.

* Generated based on a pulse width of 300 μs .

Figure 10: Typical Normalized Threshold Voltage vs. Temp.

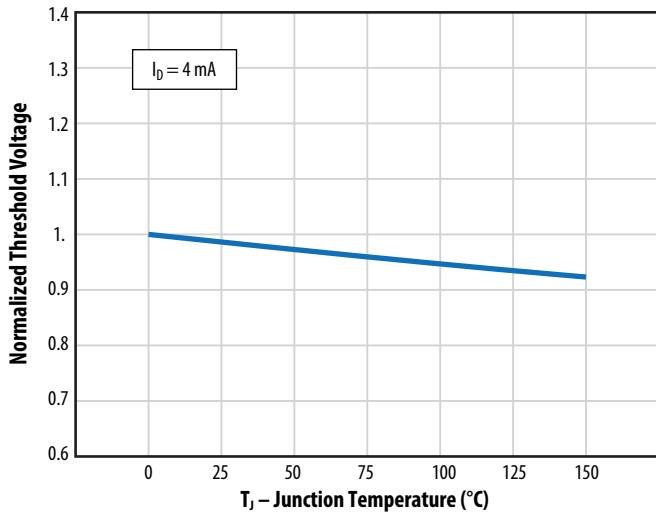


Figure 11: Safe Operating Area

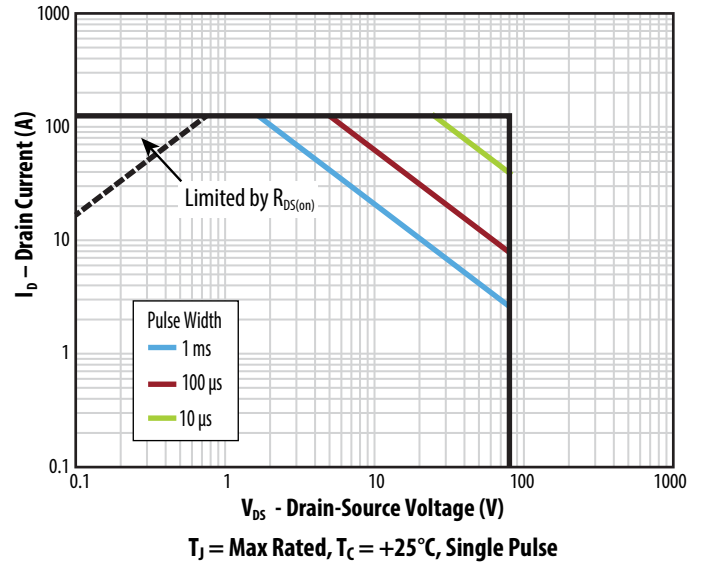
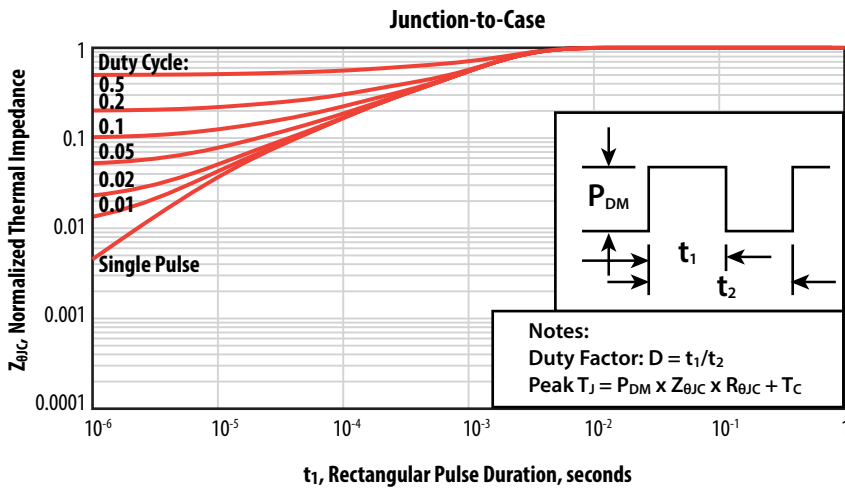
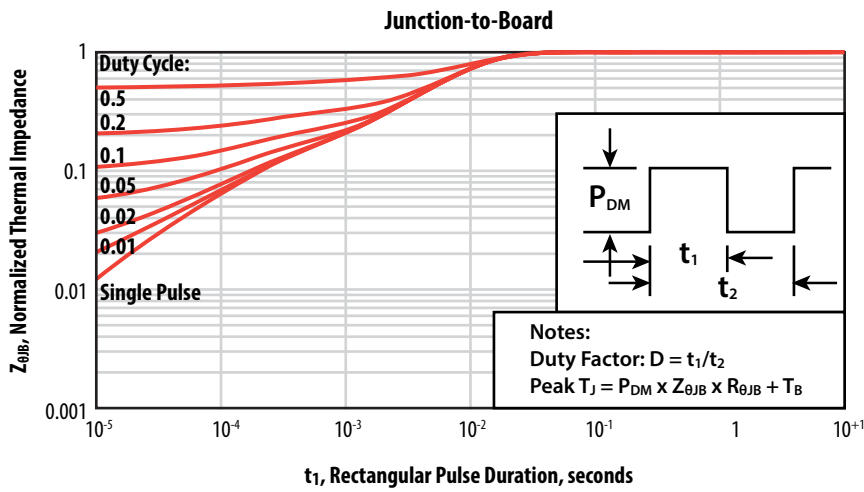
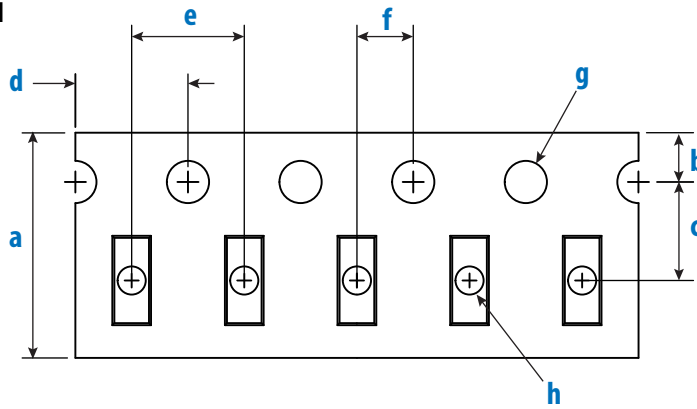
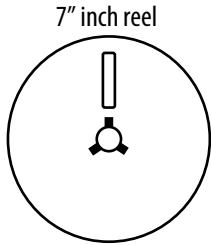


Figure 12: Typical Transient Thermal Response Curves



TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel



Loaded Tape Feed Direction →



Die orientation dot
Gate solder bar is under this corner

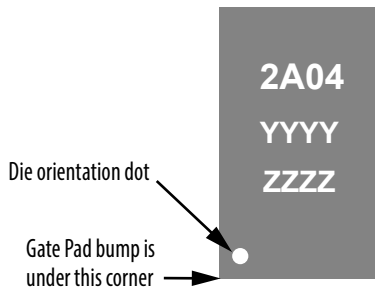
Die is placed into pocket solder bars side down (face side down)

EPC2204A (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	0.50	0.45	0.55

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

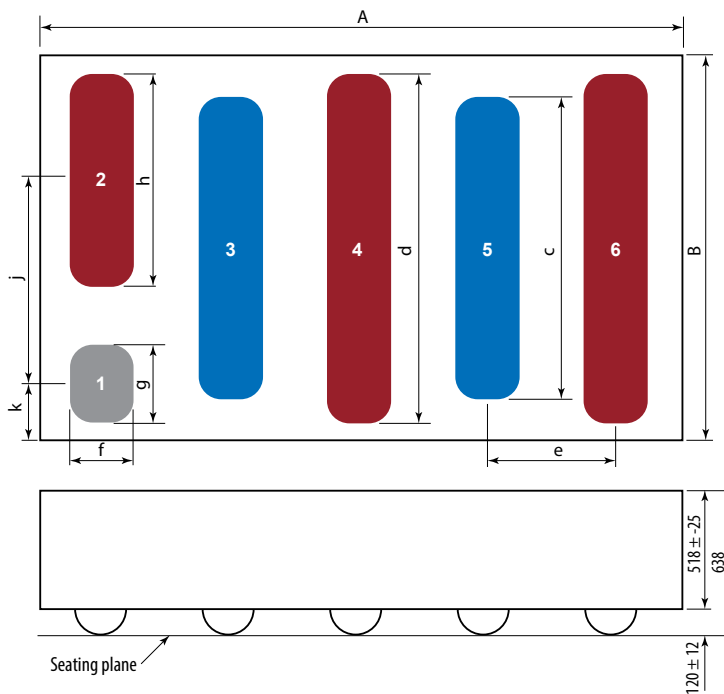
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2204A	2A04	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View

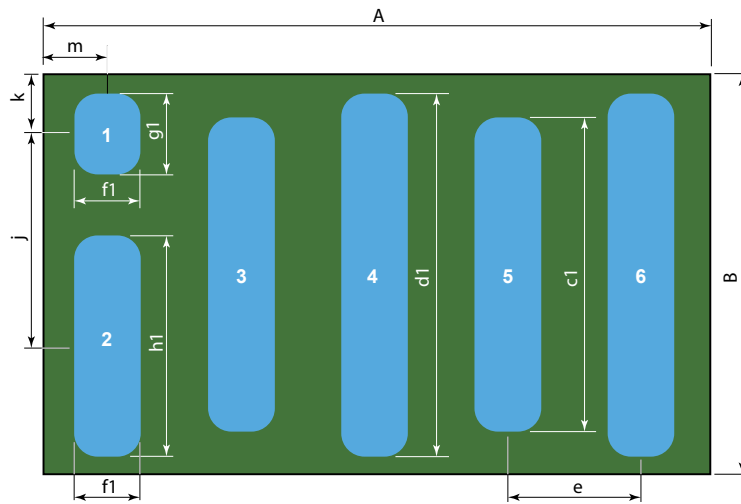


DIM	Micrometers		
	MIN	Nominal	MAX
A	2470	2500	2530
B	1470	1500	1530
c		1175	
d		1350	
e		500	
f		250	
g		300	
h		825	
j		787.5	
k		225	
m		250	

Pad 1 is Gate;
Pads 2, 4, 6 are Source;
Pads 3, 5 are Drain

Note: Substrate (top side) connected to source

RECOMMENDED LAND PATTERN
(units in μm)

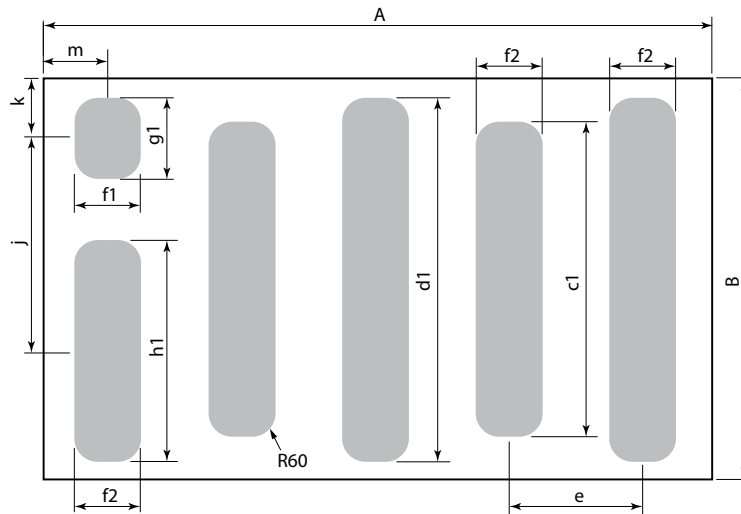


Land pattern is solder mask defined

DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
g1	280
h1	805
j	787.5
k	225
m	250

Pad 1 is Gate;
Pads 2, 4, 6 are Source;
Pads 3, 5 are Drain

RECOMMENDED STENCIL DRAWING
(units in μm)



DIM	Nominal
A	2500
B	1500
c1	1155
d1	1330
e	500
f1	230
f2	210
g1	280
h1	805
j	787.5
k	225
m	250

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at <https://epc-co.com/epc/design-support>

Efficient Power Conversion Corporation (EPC) reserves the right to make changes without further notice to any products herein to improve reliability, function or design. EPC does not assume any liability arising out of the application or use of any product or circuit described herein; neither does it convey any license under its patent rights, nor the rights of others.

eGaN® is a registered trademark of Efficient Power Conversion Corporation.

EPC Patent Listing: <https://epc-co.com/epc/about-epc/patents>