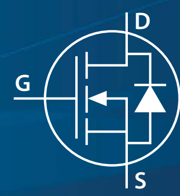
EPC2307 – Enhancement Mode Power Transistor

V_{DS} , 200 V
$R_{DS(on)}$, 10 mΩ max

PRELIMINARY



EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

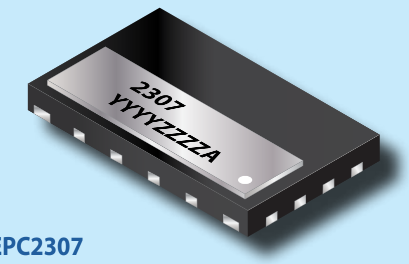
Application Notes:
- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions: EPC GaN Talk Support Forum FORUM

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	200	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	240	
I_D	Continuous (T_A = 25°C)	48	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	130	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = [TBD]	200			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 160 V		0.002		mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.006		
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.4		
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.002		
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 4 mA	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 16 A		8.2	10	mΩ
V_{SD}	Source-Drain Forward Voltage#	I_S = 0.5 A, V_{GS} = 0 V		1.6		V

Defined by design. Not subject to production test.



EPC2307
Package size: 3 x 5 mm

Applications
- Synchronous Rectification
- AC/DC chargers, SMPS, adaptors
- High Frequency DC-DC Conversion
- Class D audio
- Wireless Power
- High power lidar & dToF

Benefits
- Higher Efficiency – Lower conduction and switching losses, zero reverse recovery losses
- Ultra Small Footprint – Higher power density

Scan QR code or click link below for more information including reliability reports, device models, demo boards!

https://l.ead.me/EPC2307

Dynamic Characteristics# (T_J = 25°C unless otherwise stated)							
PARAMETER		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
C_{ISS}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V		1401		pF
C_{RSS}	Reverse Transfer Capacitance			1.2		
C_{OSS}	Output Capacitance			326		
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	V_{DS} = 0 to 100 V, V_{GS} = 0 V		445		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			579		
Q_G	Total Gate Charge	V_{DS} = 100 V, V_{GS} = 5 V, I_D = 16 A		10.6		nC
Q_{GD}	Gate-to-Drain Charge	V_{DS} = 100 V, I_D = 16 A		1.3		
Q_{OSS}	Output Charge	V_{DS} = 100 V, V_{GS} = 0 V		58		
Q_{RR}	Source-Drain Recovery Charge			0		

All measurements were done with substrate shorted to source.
Defined by design. Not subject to production test.
Note 1: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 2: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

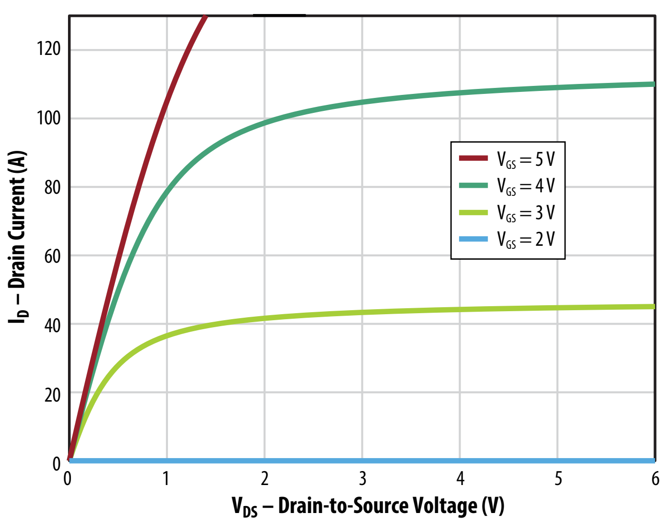


Figure 2: Typical Transfer Characteristics

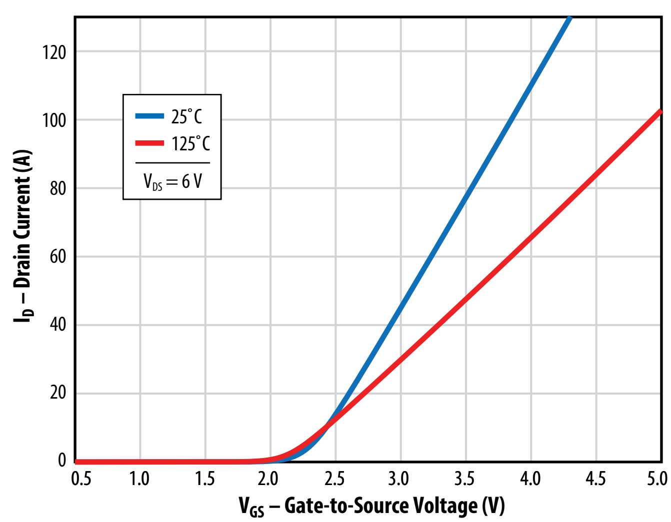


Figure 3: Typical $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

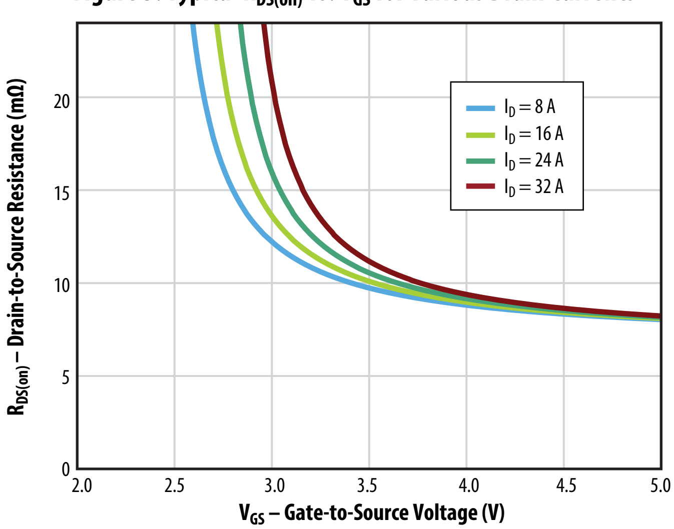


Figure 4: Typical $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

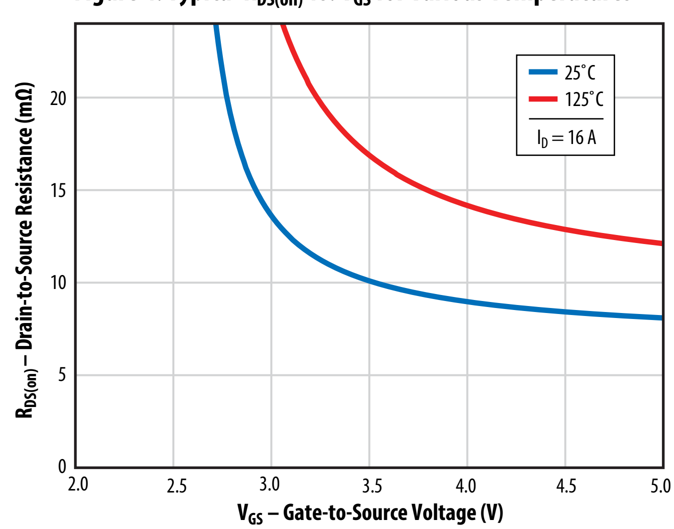


Figure 5a: Typical Capacitance (Linear Scale)

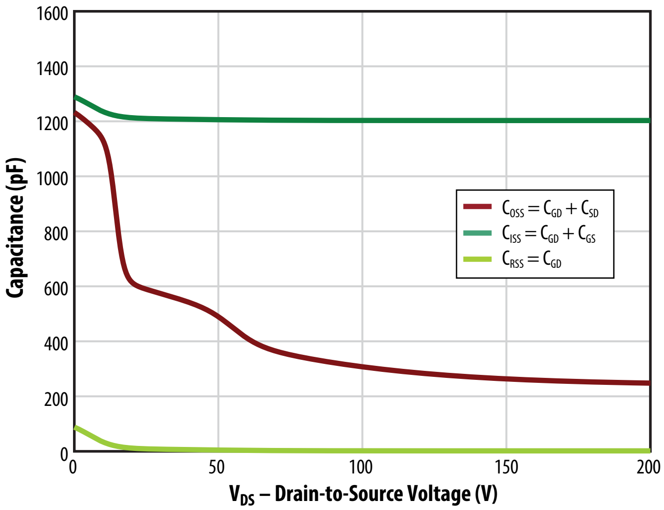


Figure 5b: Typical Capacitance (Log Scale)

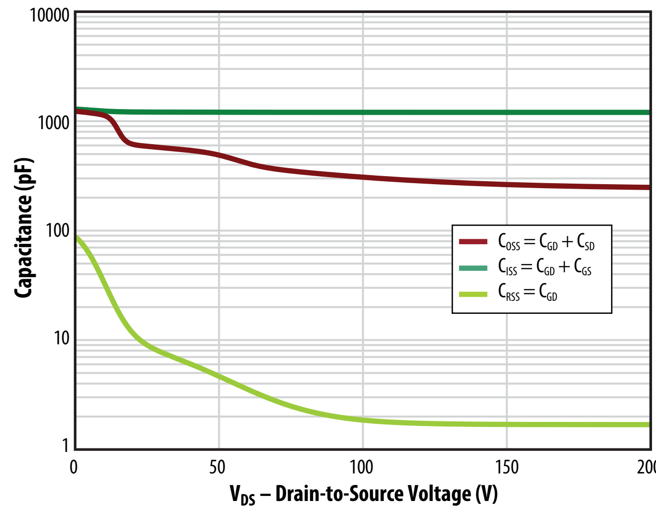


Figure 6: Typical Output Charge and C_{OSS} Stored Energy

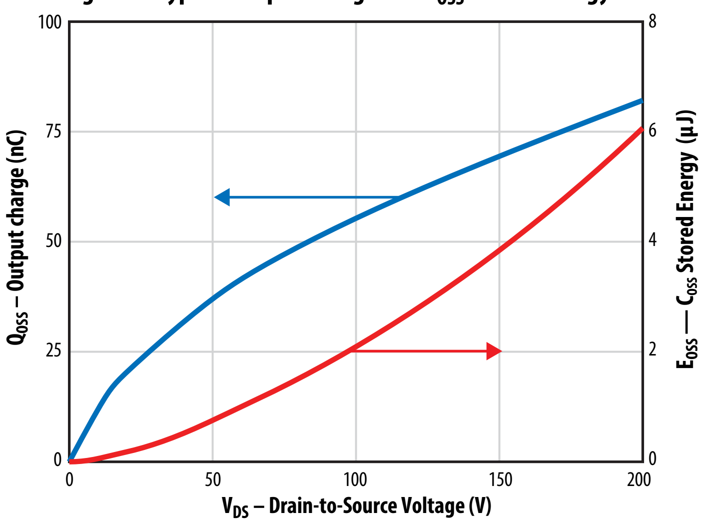


Figure 7: Typical Gate Charge

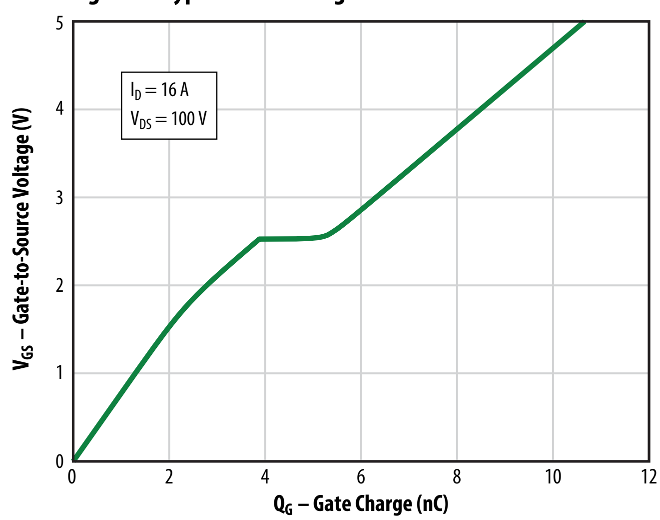
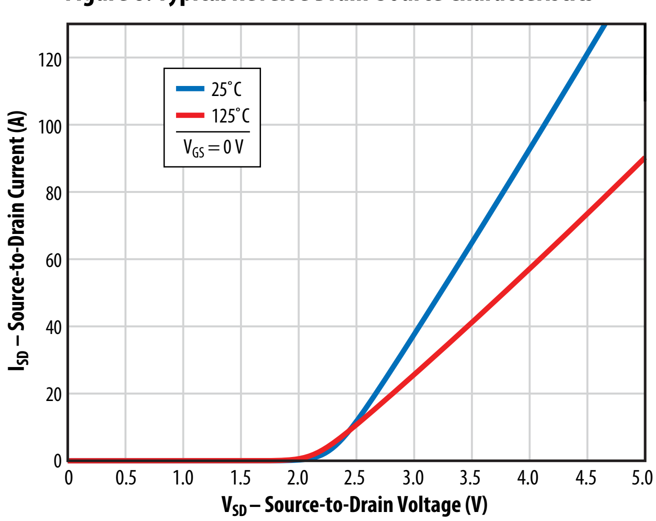


Figure 8: Typical Reverse Drain-Source Characteristics



Note: Negative gate drive voltage increases the reverse drain-source voltage.
EPC recommends 0 V for OFF.

Figure 9: Typical Normalized On-State Resistance vs. Temp.

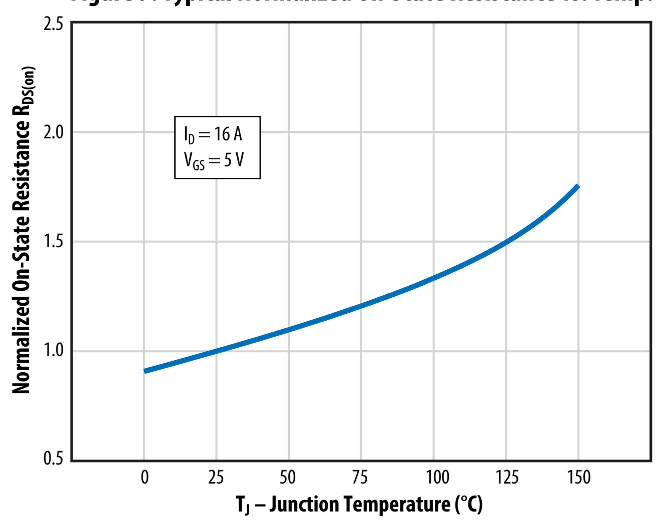
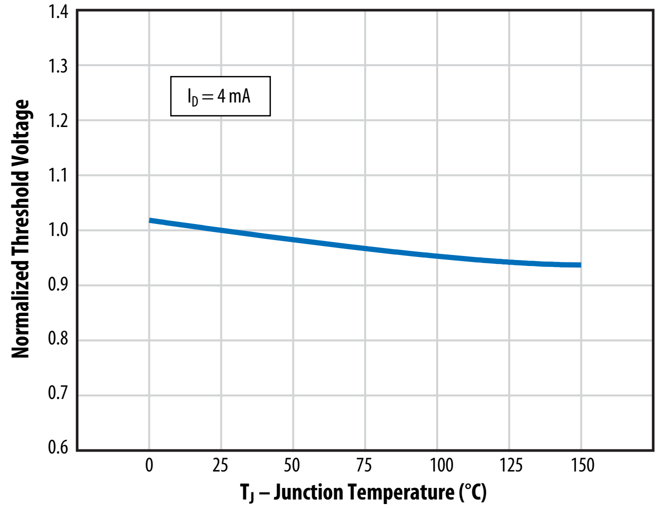
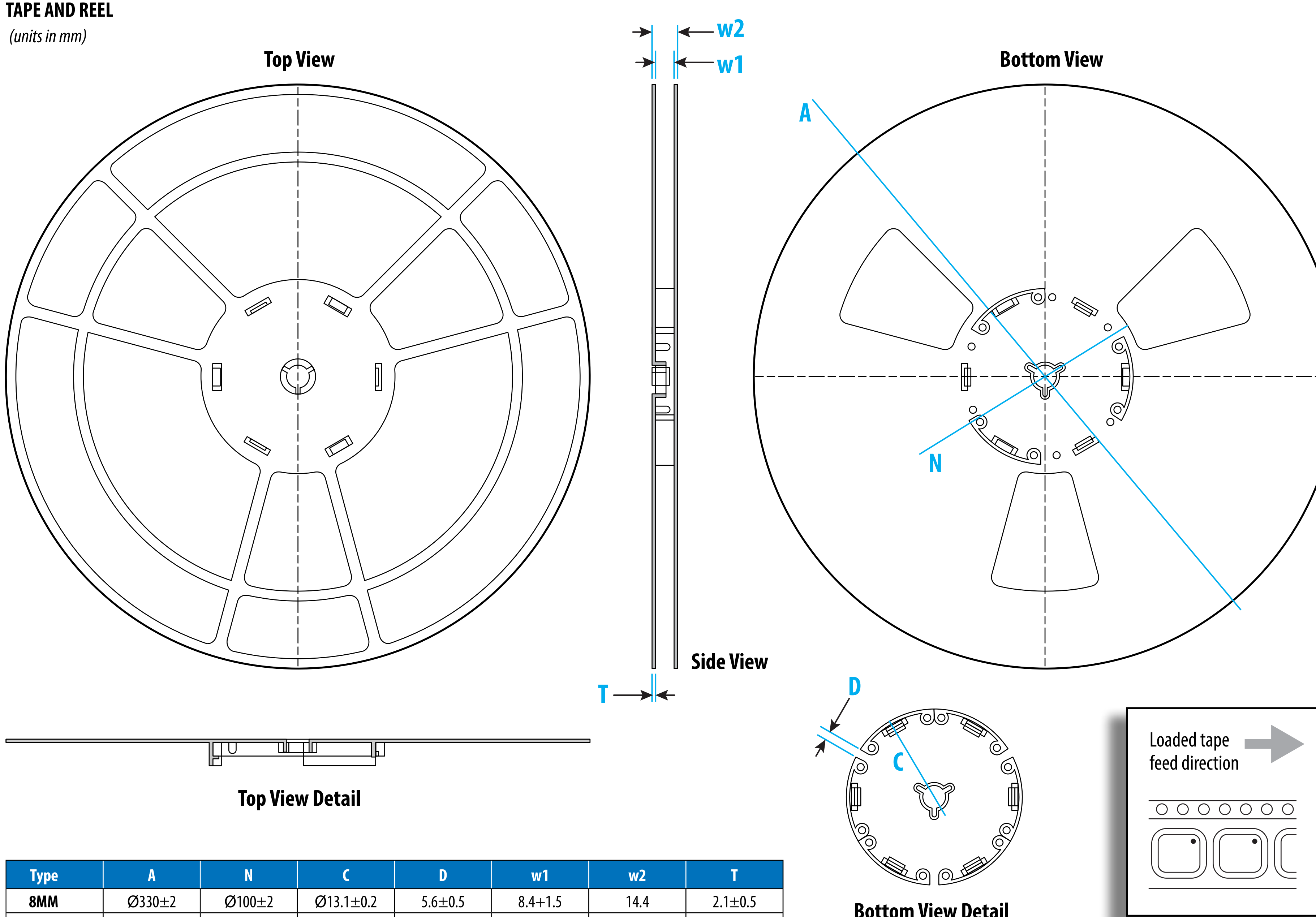


Figure 10: Typical Normalized Threshold Voltage vs. Temp.

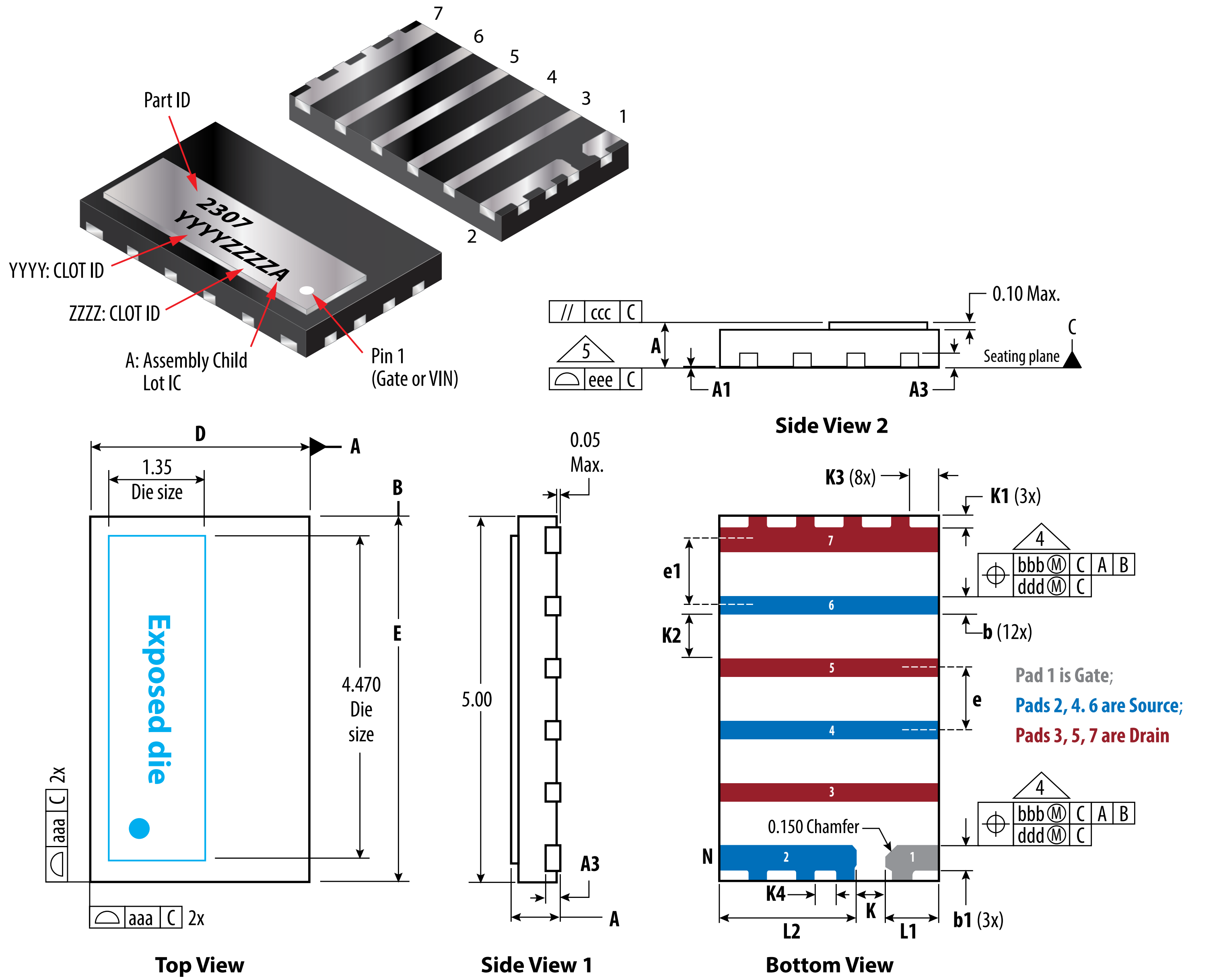


TAPE AND REEL

(units in mm)



Type	A	N	C	D	w1	w2	T
8MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	8.4+1.5	14.4	2.1±0.5
12MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	12.4+1.5	18.4	2.1±0.5
16MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	16.4+1.5	22.4	2.1±0.5
24MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	24.4+1.5	30,4	2.1±0.5



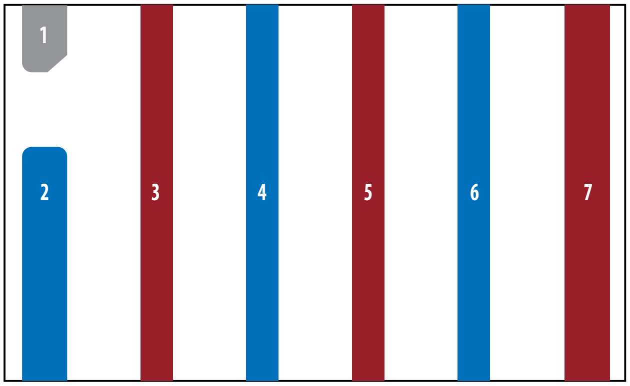
SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
b	0.20	0.25	0.30	4
b1	0.30	0.35	0.40	4
b2	0.20	0.25	0.30	4
D		3.00 BSC		
E		5.00 BSC		
e		0.85 BSC		
e1		0.90 BSC		
L1	0.625	0.725	0.825	
L2	1.775	1.875	1.975	

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
K	0.35	0.40	0.45	
K1	0.10	0.15	0.20	
K2	0.55	0.60	0.65	
K3	0.35	0.40	0.45	
K4	0.25	0.30	0.35	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		15		3
NE		6		

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals
4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.

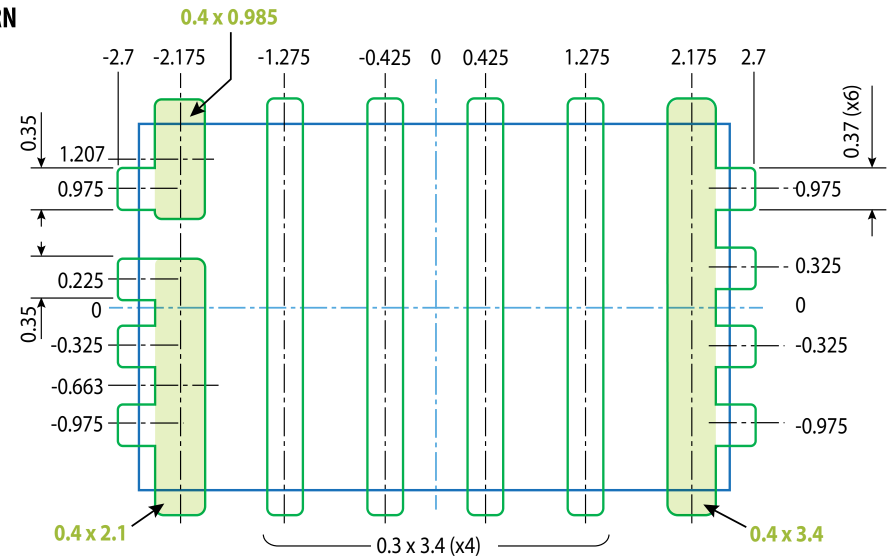
TRANSPARENT VIEW



PIN	DESCRIPTION
1	Gate
2	Source
3	Drain
4	Source
5	Drain
6	Source
7	Drain

RECOMMENDED LAND PATTERN

(units in mm)



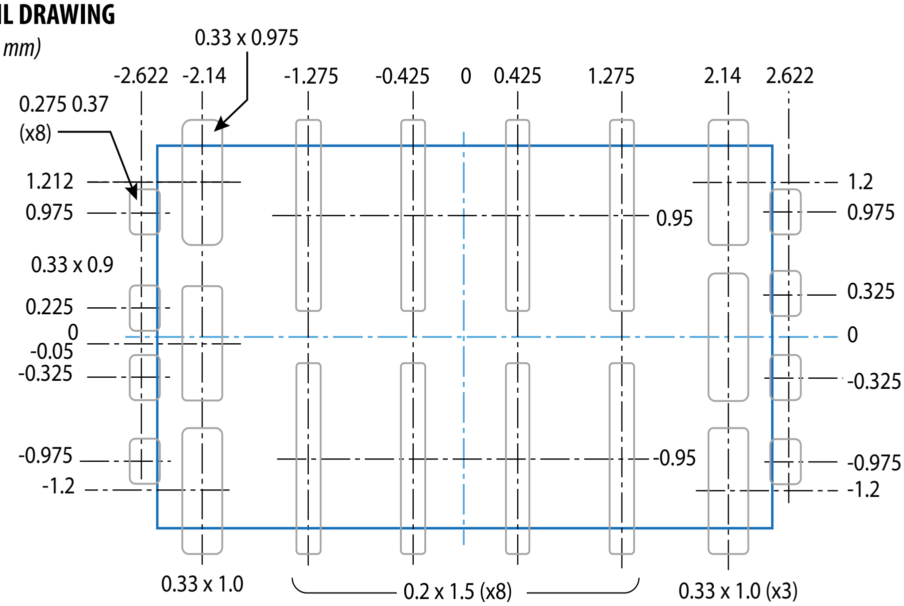
Legend:
Part outline
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING

(units in mm)



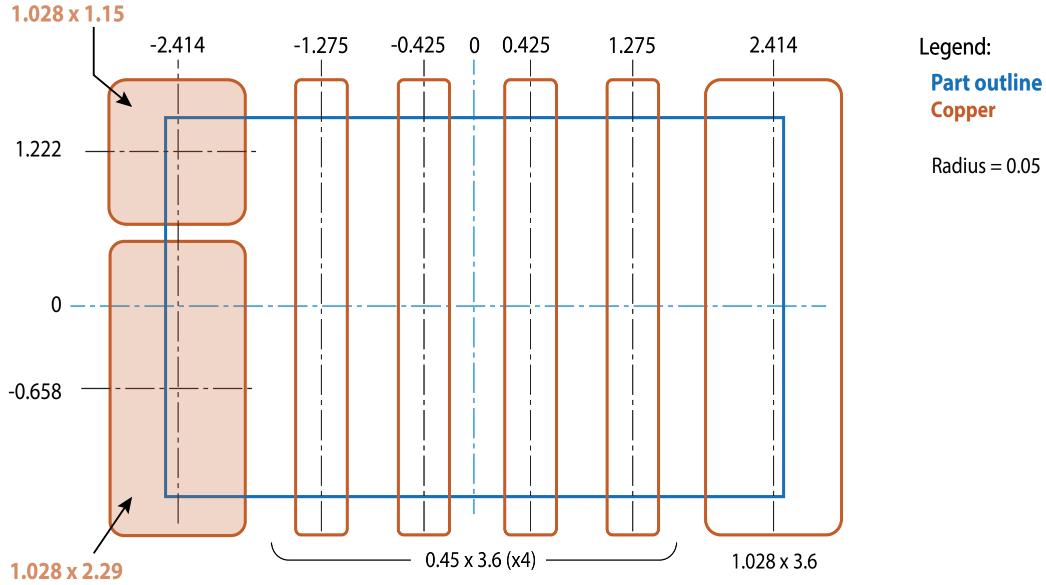
Legend:
Part outline
Stencil opening

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

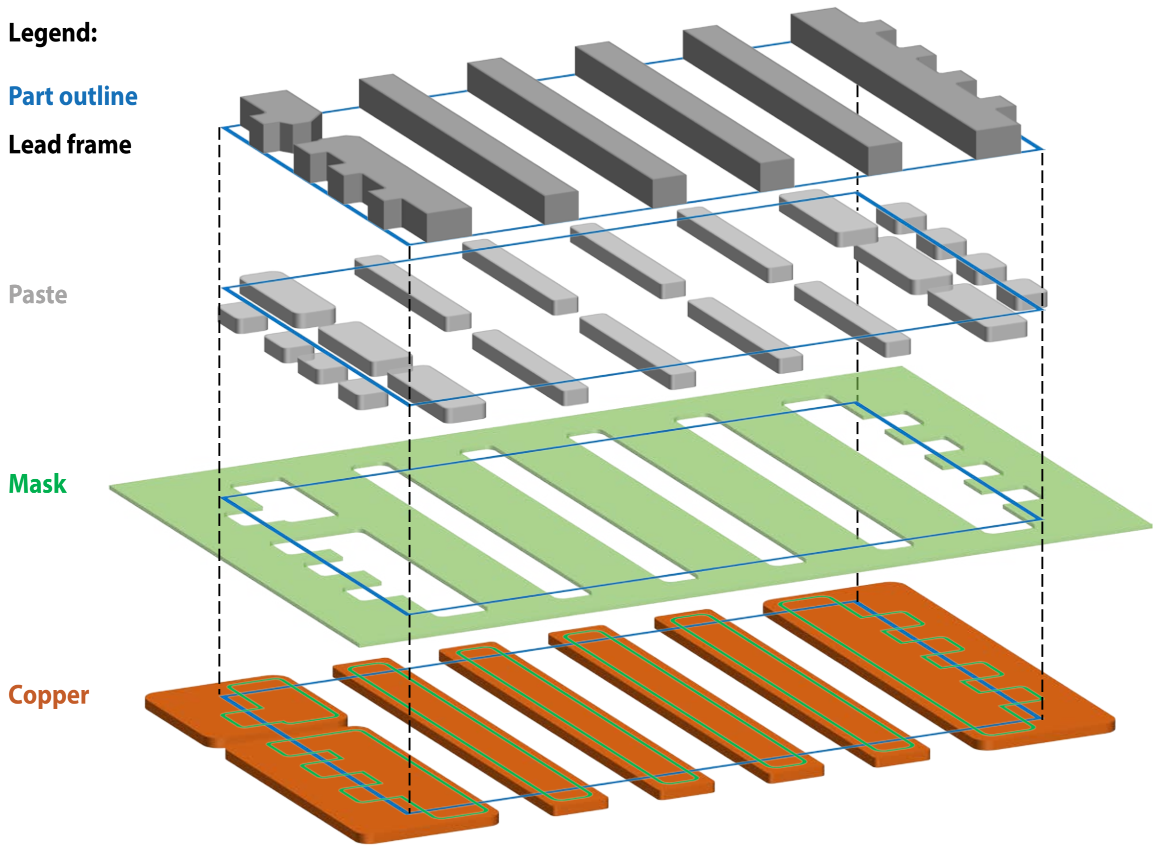
The corner has a radius of 0.1.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

RECOMMENDED COPPER DRAWING
(units in mm)



3D COMPOSITE



Additional resources available:

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip
  (for preliminary device Altium footprints, contact EPC)

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