

EPC2361 – Enhancement Mode Power Transistor

V_{DS} , 100 V

$R_{DS(on)}$, 1.0 m Ω typical

I_D , 101 A

PRELIMINARY



RoHS



Halogen-Free

Description

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR} . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Application notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

Questions:
Ask a GaN
Expert

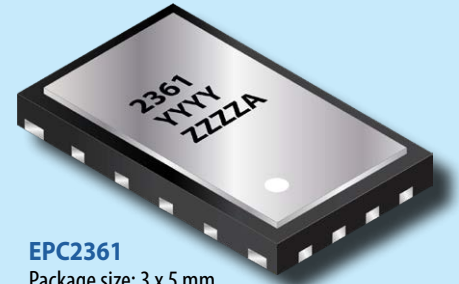


Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150 °C)	120	
I_D	Continuous ($T_A = 25^\circ\text{C}$)	101	A
	Pulsed (25°C , $T_{PULSE} = 300 \mu\text{s}$)	519	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	$^\circ\text{C}$
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.2	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.5	
$R_{\theta JA_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	45	
$R_{\theta JA_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC9097 EVB)	21	

Static Characteristics ($T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}$, $I_D = \text{TBD}$	100			V
I_{DSS}	Drain-Source Leakage	$V_{DS} = 80\text{ V}$, $V_{GS} = 0\text{ V}$		0.03		mA
I_{GSS}	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.06		
	Gate-to-Source Forward Leakage [#]	$V_{GS} = 5\text{ V}$, $T_J = 125^\circ\text{C}$		0.15		
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.02		
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 15\text{ mA}$	0.8	1.1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}$, $I_D = 50\text{ A}$		1.0		m Ω
V_{SD}	Source-to-Drain Forward Voltage [#]	$I_S = 0.5\text{ A}$, $V_{GS} = 0\text{ V}$		1.6		V

[#] Defined by design. Not subject to production test.



EPC2361

Package size: 3 x 5 mm

Applications

- High Power PSU AC-DC Synchronous Rectification
- High Frequency DC-DC Conversion up to 80 V input (Buck, Boost, Buck-Boost and LLC)
- 24 V–60 V Motor Drives
- High Power Density DC-DC modules from 40 V–60 V to 5 V–12 V
- Synchronous Rectification
- Solar MPPT

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint
- Excellent Thermal

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2361>

Dynamic Characteristics[#] (T_j = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C _{ISS}	Input Capacitance	V _{DS} = 50 V, V _{GS} = 0 V		4094		pF
C _{RSS}	Reverse Transfer Capacitance			12		
C _{OSS}	Output Capacitance			1147		
C _{OSS(ER)}	Effective Output Capacitance, Energy Related (Note 1)	V _{DS} = 0 to 50 V, V _{GS} = 0 V		1398		pF
C _{OSS(TR)}	Effective Output Capacitance, Time Related (Note 2)			1726		
Q _G	Total Gate Charge	V _{DS} = 50 V, V _{GS} = 5 V, I _D = 50 A		28		nC
Q _{GS}	Gate-to-Source Charge	V _{DS} = 50 V, I _D = 50 A		7.2		
Q _{GD}	Gate-to-Drain Charge			2.5		
Q _{G(TH)}	Gate Charge at Threshold			4.9		
Q _{OSS}	Output Charge	V _{DS} = 50 V, V _{GS} = 0 V		86		
Q _{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.

All measurements were done with substrate shorted to source.

Note 1: C_{OSS(ER)} is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50 V.

Note 2: C_{OSS(TR)} is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50 V.

Figure 1: Typical Output Characteristics at 25°C

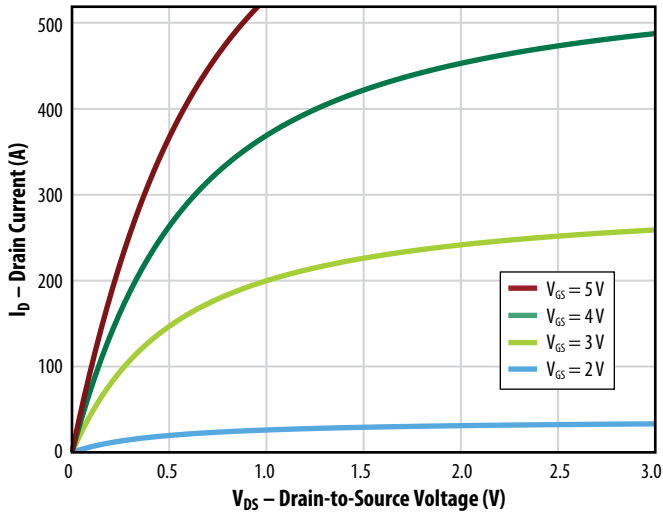


Figure 2: Typical Transfer Characteristics

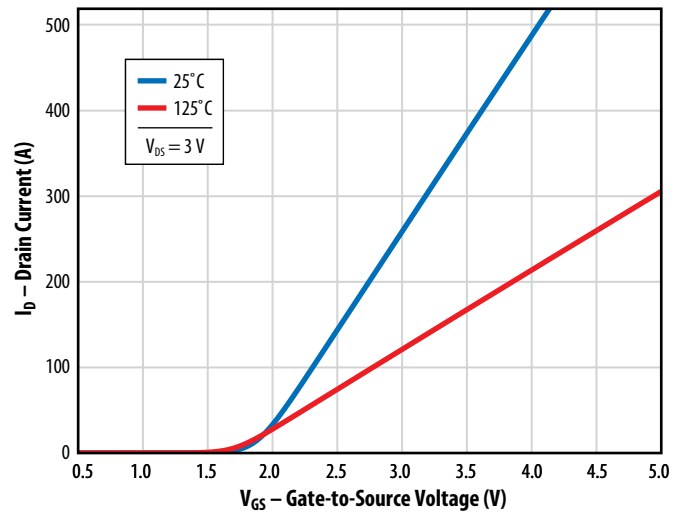


Figure 3: R_{DS(on)} vs. V_{GS} for Various Drain Currents

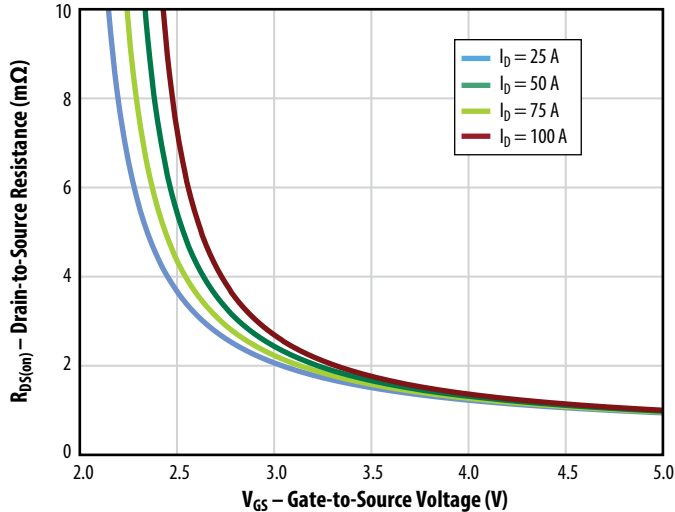


Figure 4: R_{DS(on)} vs. V_{GS} for Various Temperatures

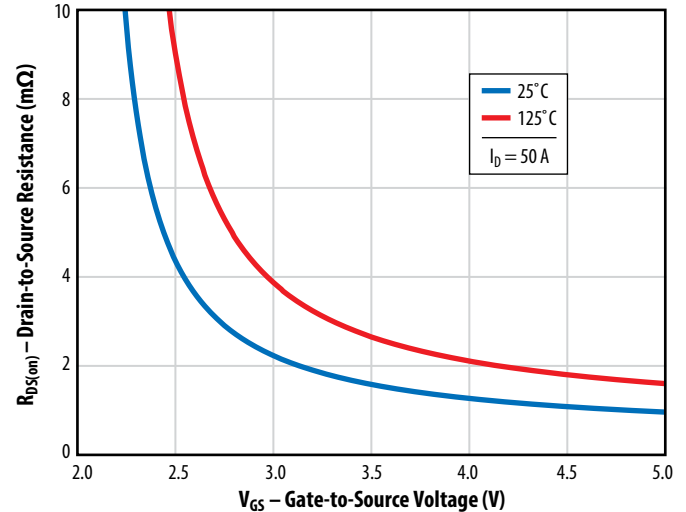


Figure 5a: Typical Capacitance (Linear Scale)

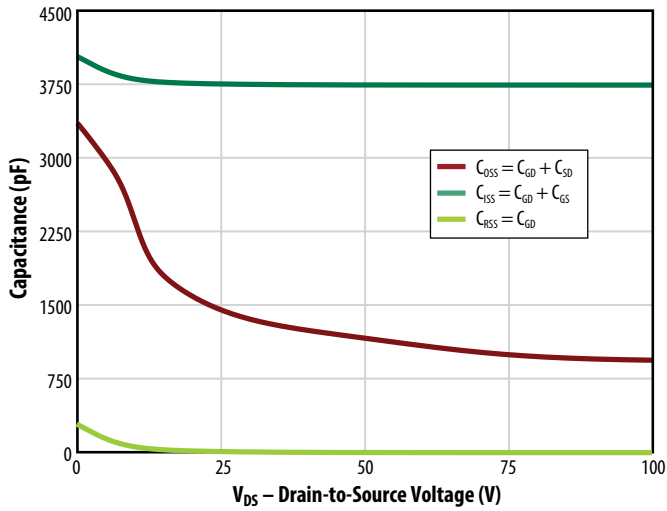


Figure 5b: Typical Capacitance (Log Scale)

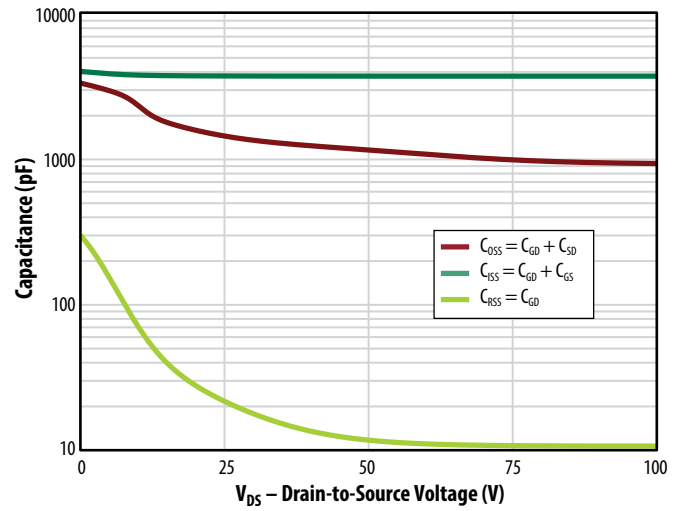


Figure 6: Typical Output Charge and C_oss Stored Energy

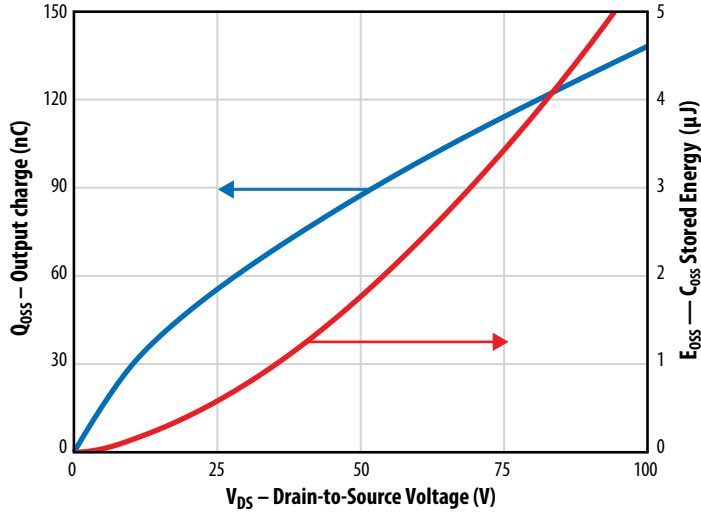


Figure 7: Typical Gate Charge

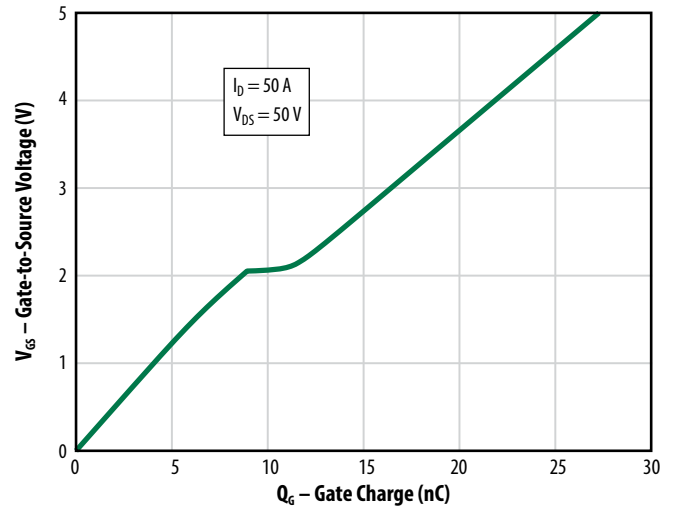


Figure 8: Reverse Drain-Source Characteristics

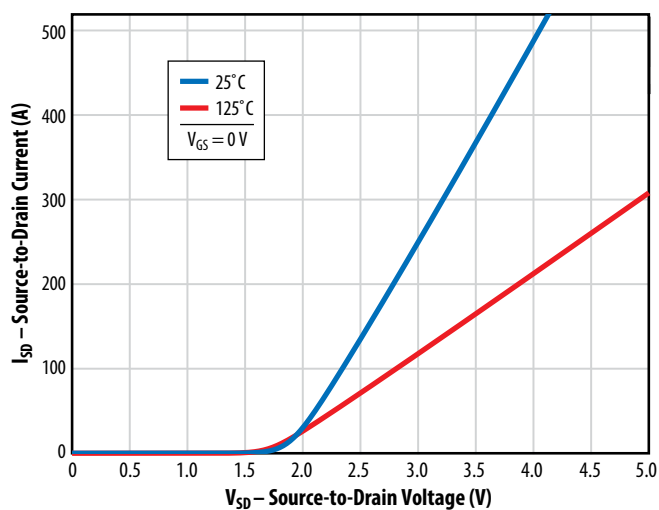
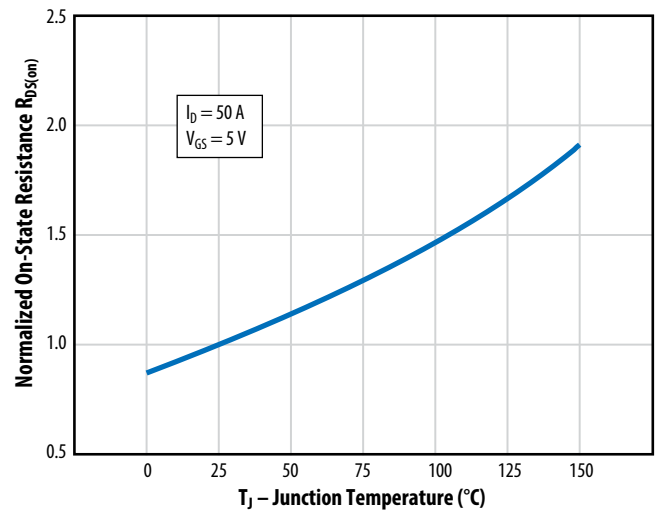


Figure 9: Normalized On-State Resistance vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage. EPC recommends 0V for OFF.

Figure 10: Normalized Threshold Voltage vs. Temperature

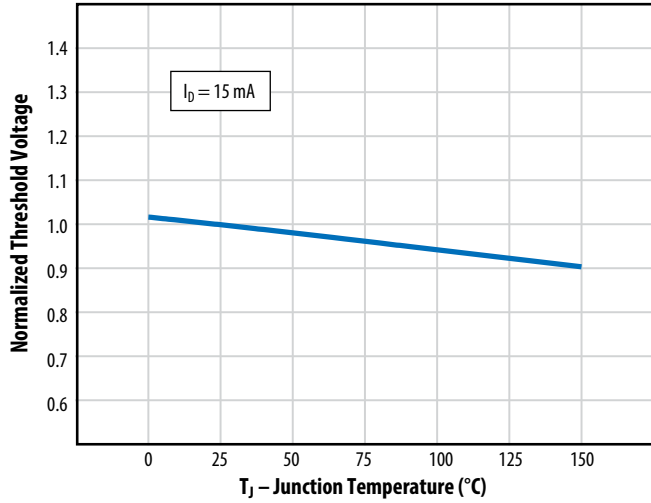


Figure 11: Safe Operating Area

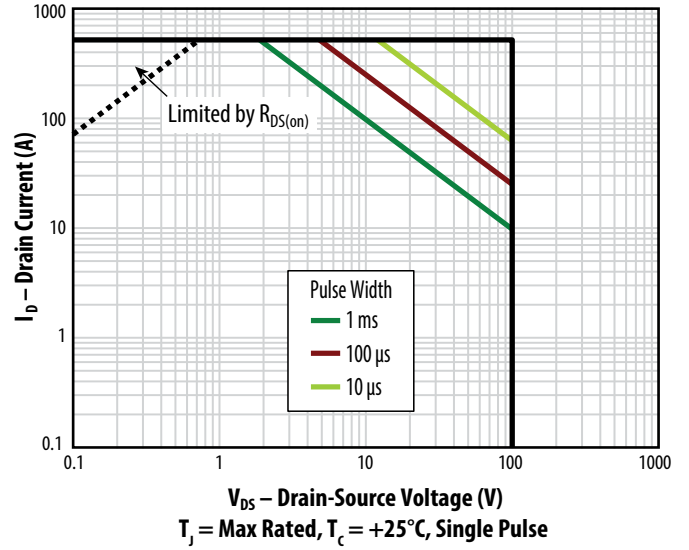
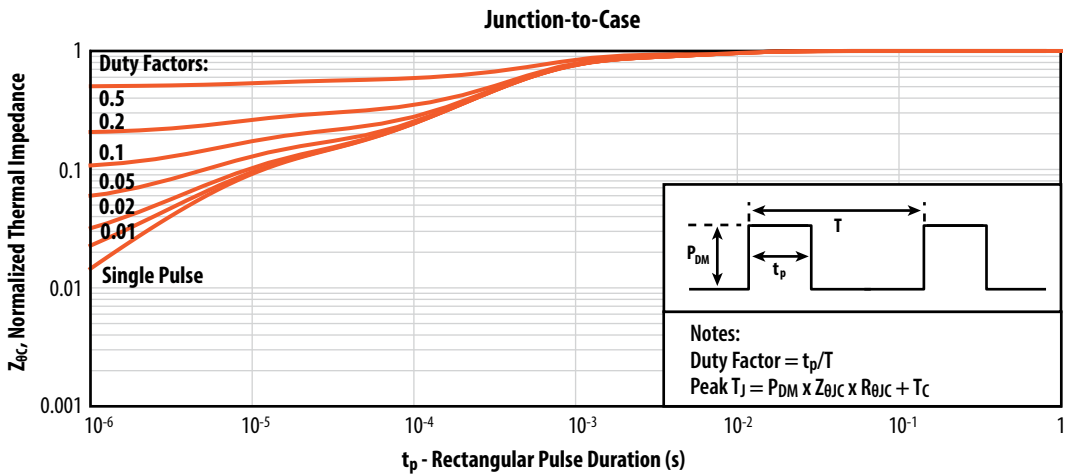
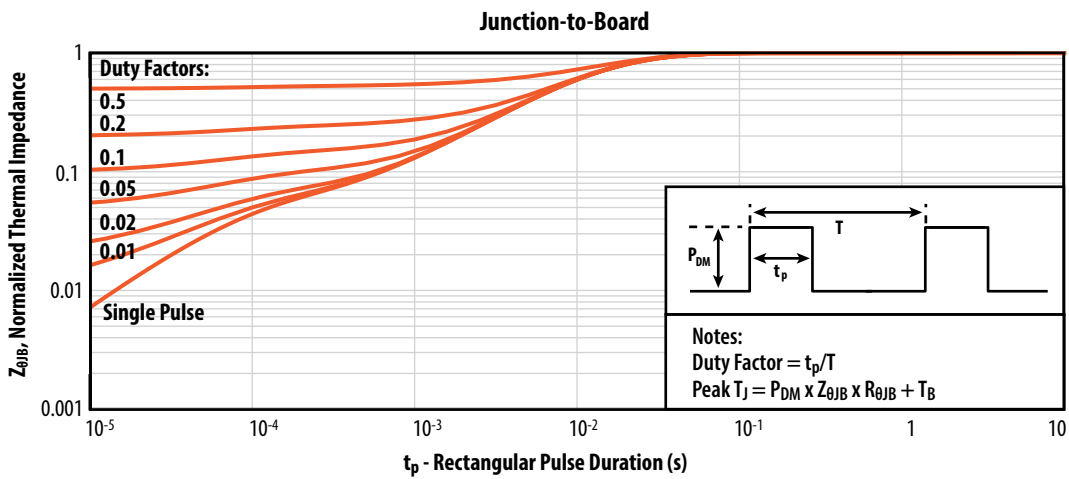


Figure 12: Transient Thermal Response Curves



TYPICAL THERMAL CONCEPT

The EPC2361 can take advantage of dual sided cooling to maximize its heat dissipation capabilities in high power density designs. **Note that the top of EPC FETs are connected to source potential, so for half-bridge topologies the Thermal Interface Material (TIM) needs to provide electrical isolation to the heatsink.**

Recommended best practice thermal solutions are covered in detail in [How2AppNote012 - How to Get More Power Out of an eGaN Converter.pdf](#).

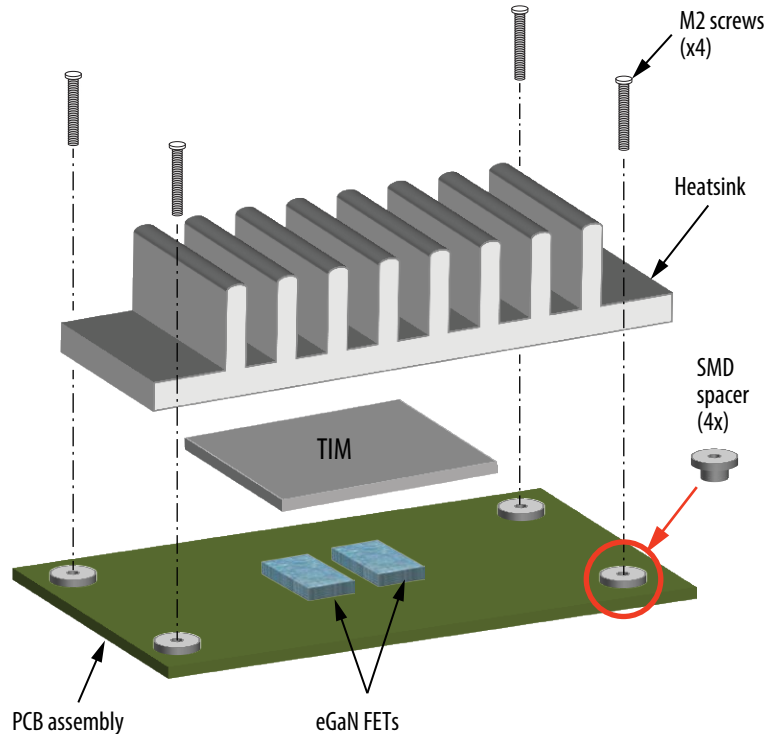


Figure 13: Exploded view of heatsink assembly using screws

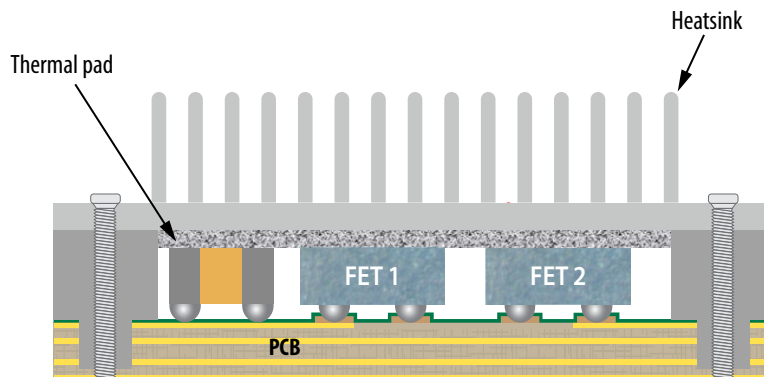


Figure 14: A cross-section image of dual sided thermal solution

Note: Connecting the heatsink to ground is recommended and can significantly improve radiated EMI

The thermal design can be optimized by using the [GaN FET Thermal Calculator](#) on EPC's website.

LAYOUT CONSIDERATIONS

GaN transistors generally behave like power MOSFETs, but at much higher switching speeds and power densities, therefore layout considerations are very important, and care must be taken to minimize layout parasitic inductances. The recommended design utilizes the first inner layer as a power loop return path. This return path is located directly beneath the top layer’s power loop allowing for the smallest physical loop size. This method is also commonly referred to as flux cancellation. Variations of this concept can be implemented by placing the bus capacitors either next to the high side device, next to the low side device, or between the low and high side devices, but in all cases the loop is closed using the first inner layer right beneath the devices.

A similar concept is also used for the gate loop, with the return gate loop located directly under the turn ON and OFF gate resistors.

Furthermore, to minimize the common source inductance between power and gate loops, the power and gate loops are laid out perpendicular to each other, and a via next to the source pad closest to the gate pad is used as Kelvin connection for the gate driver return path.

The **EPC90156 Half-Bridge Development Board Using EPC2361** implements our recommended vertical inner layout.

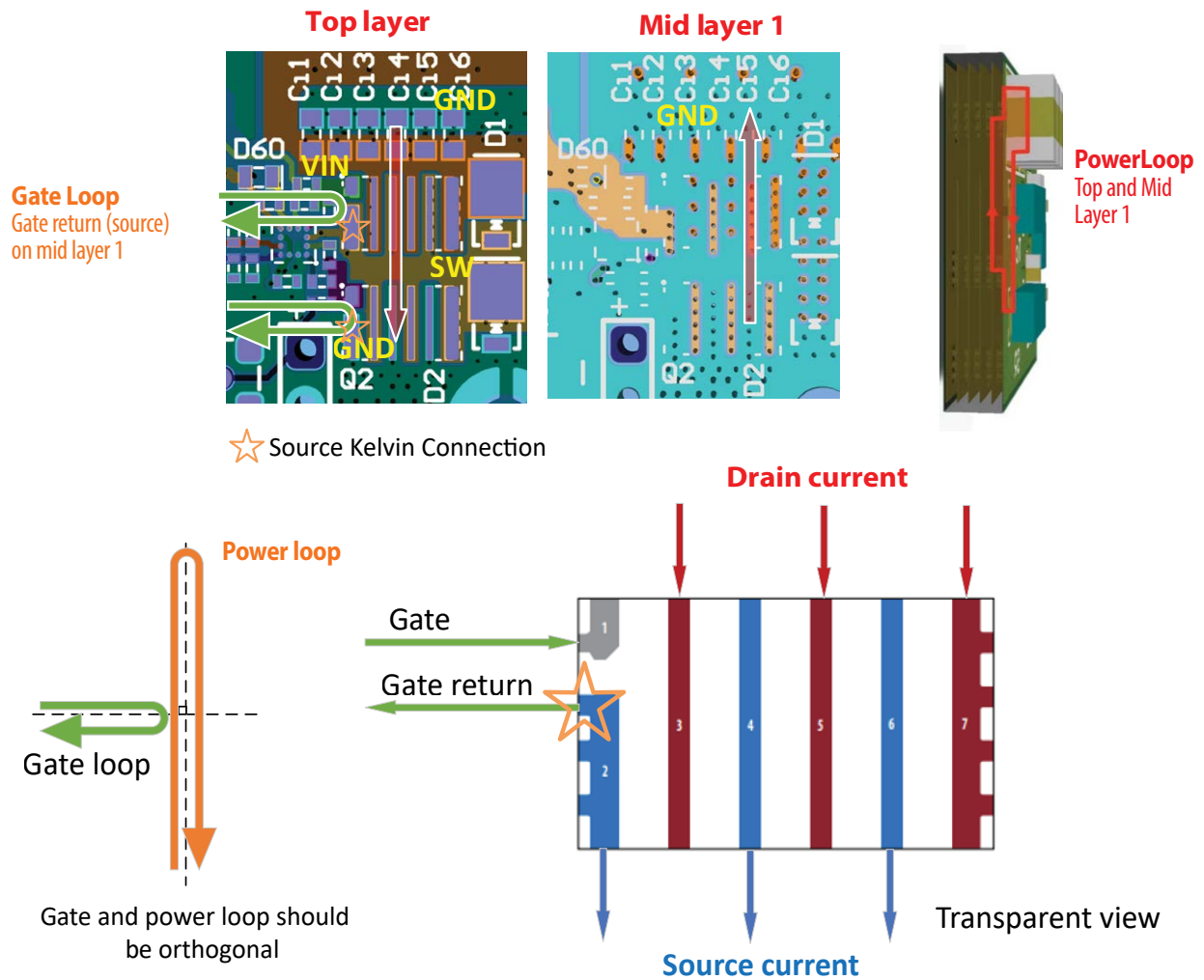
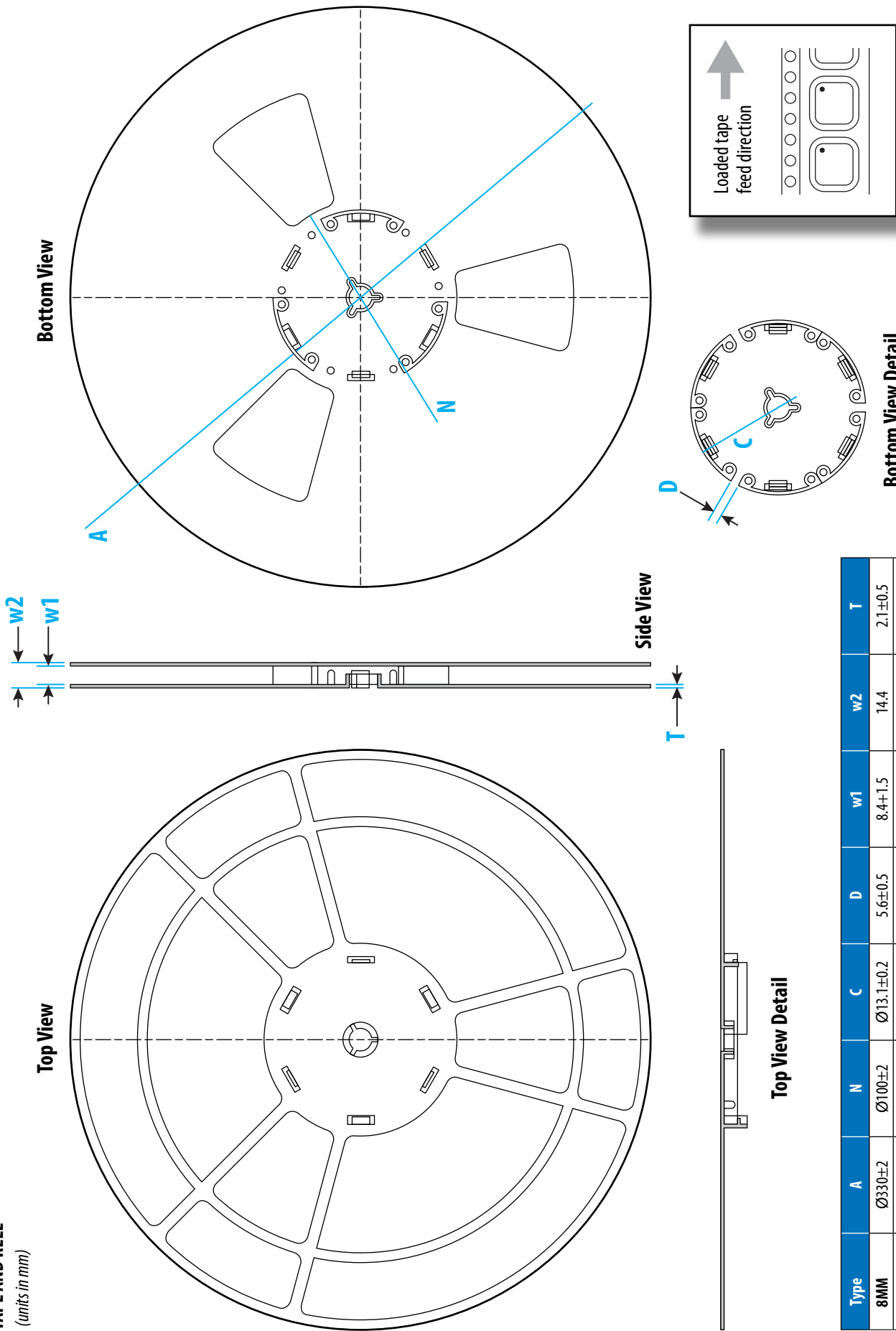


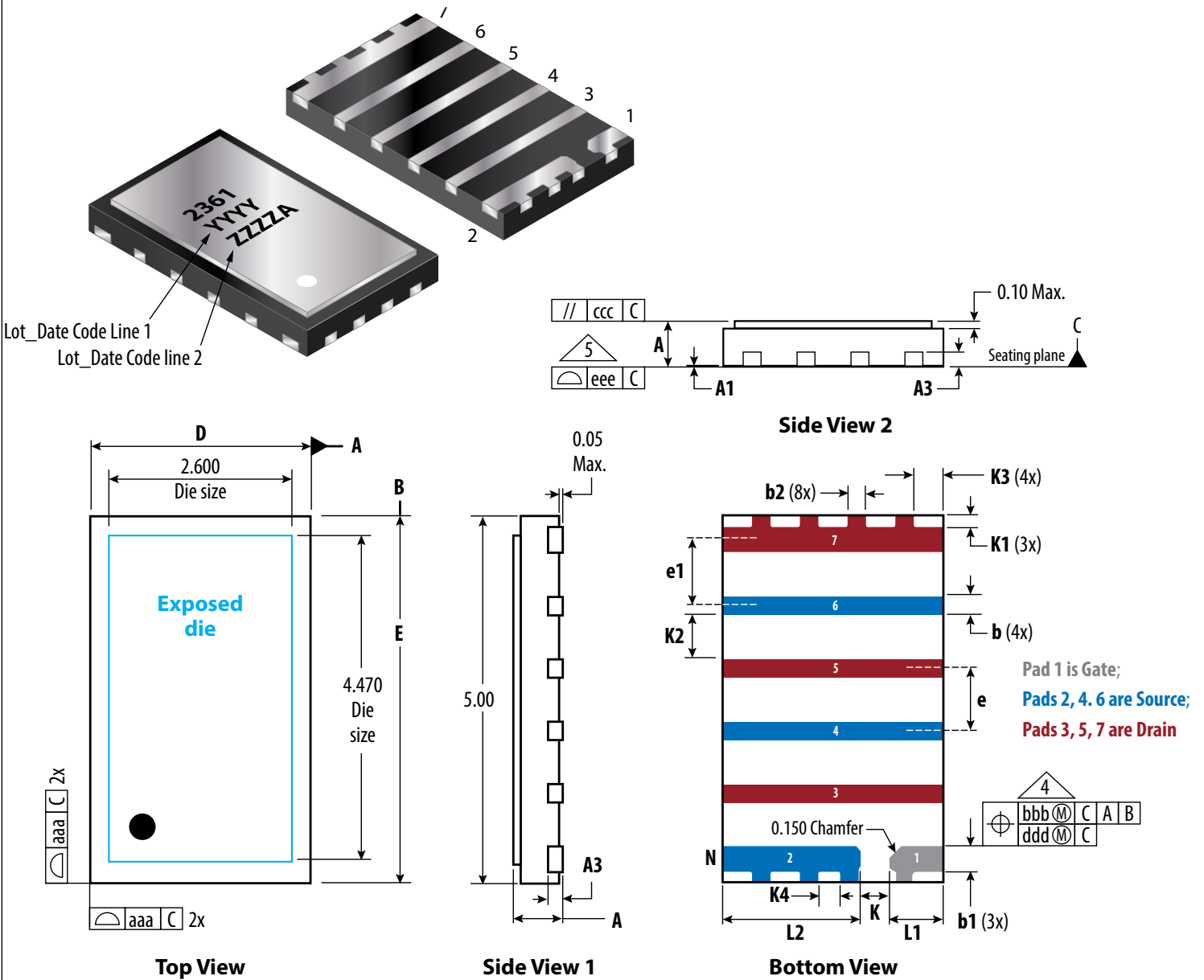
Figure 13: Inner Vertical Layout for Power and Gate Loops from EPC90156

Detailed recommendations on layout can be found on EPC’s website: [Optimizing PCB Layout with eGaN FETs.pdf](#)

TAPE AND REEL
(units in mm)



Type	A	N	C	D	w1	w2	T
8MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	8.4±1.5	14.4	2.1±0.5
12MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	12.4±1.5	18.4	2.1±0.5
16MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	16.4±1.5	22.4	2.1±0.5
24MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	24.4±1.5	30.4	2.1±0.5



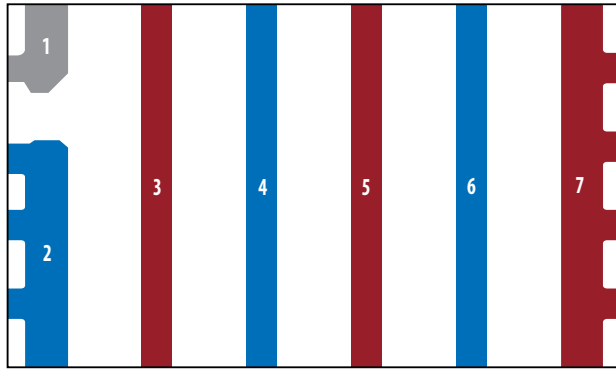
SYMBOL	Dimension (mm)			Note
	MIN	Nominal	MAX	
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
b	0.20	0.25	0.30	4
b1	0.30	0.35	0.40	4
b2	0.20	0.25	0.30	4
D		3.00 BSC		
E		5.00 BSC		
e		0.85 BSC		
e1		0.90 BSC		
L1	0.625	0.725	0.825	
L2	1.775	1.875	1.975	

SYMBOL	Dimension (mm)			Note
	MIN	Nominal	MAX	
K	0.35	0.40	0.45	
K1	0.10	0.15	0.20	
K2	0.55	0.60	0.65	
K3	0.35	0.40	0.45	
K4	0.25	0.30	0.35	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		15		3
NE		6		

Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. N is the total number of terminals
4. Dimension b applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension b should not be measured in that radius area.
5. Coplanarity applies to the terminals and all the other bottom surface metallization.

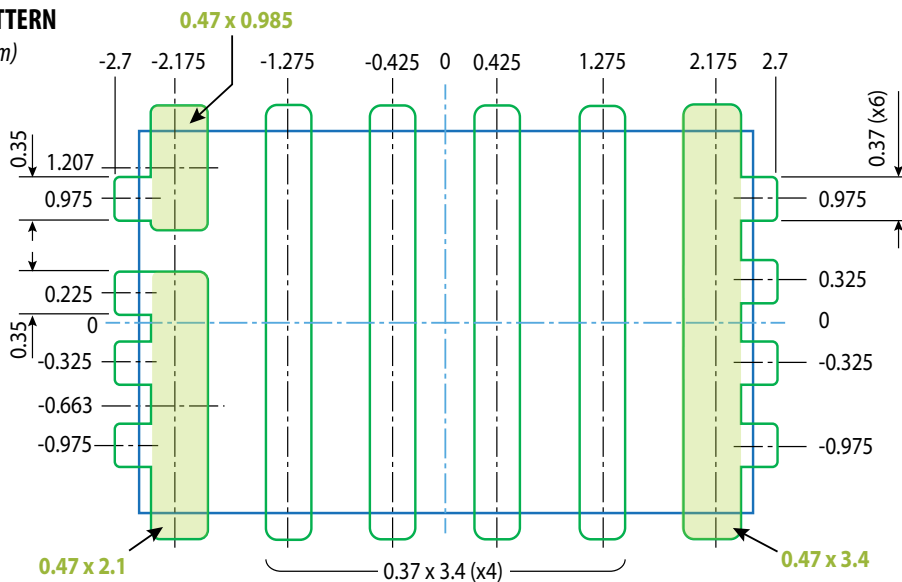
TRANSPARENT VIEW



PIN	Description
1	Gate
2	Source
3	Drain
4	Source
5	Drain
6	Source
7	Drain

RECOMMENDED LAND PATTERN

(units in mm)



Legend:

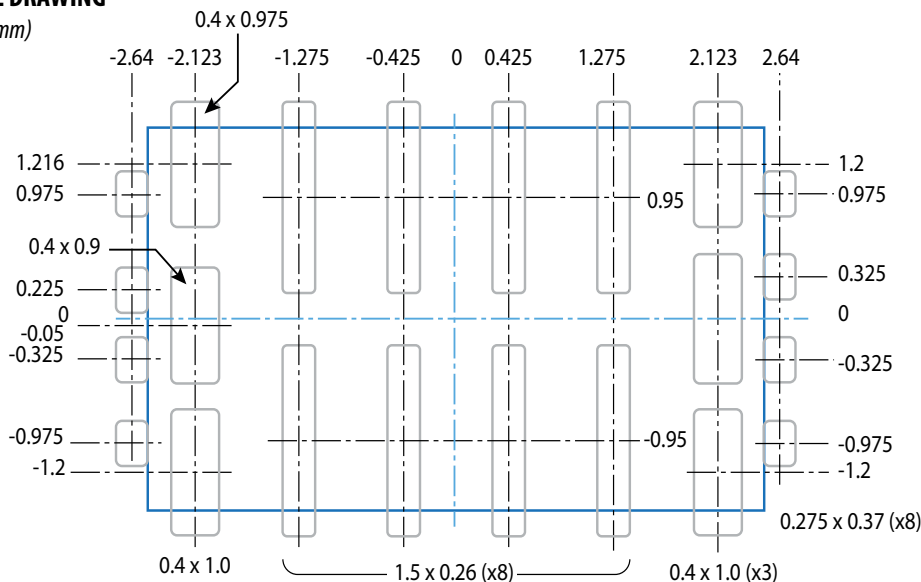
Part outline
Mask Opening

Radius = 0.05

Land pattern is solder mask defined

RECOMMENDED STENCIL DRAWING

(units in mm)



Legend:

Part outline
Stencil opening

Recommended stencil should be 4 mil (100 μm) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

The corner has a radius of R60.

EPC has tested this stencil design and not found any scooping issues.

ADDITIONAL RESOURCES AVAILABLE

Solder mask defined pads are recommended for best reliability.

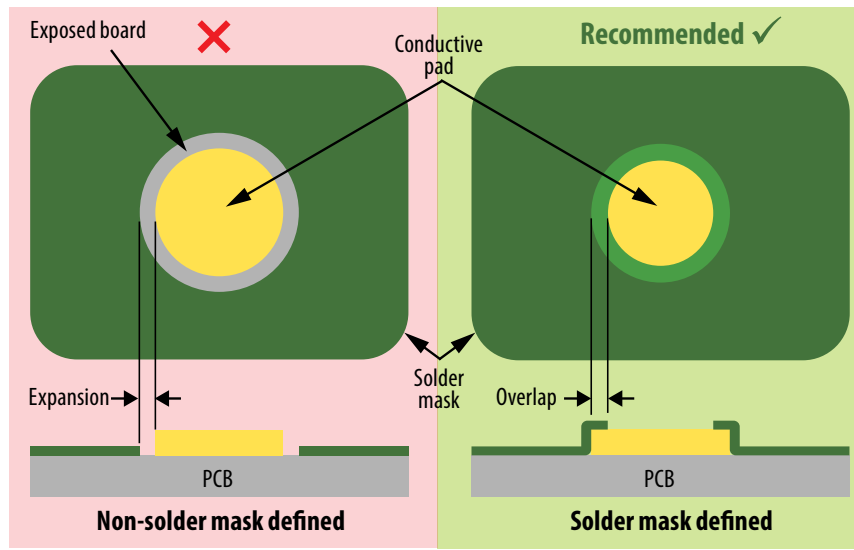


Figure 15: Solder mask defined versus non-solder mask defined pad

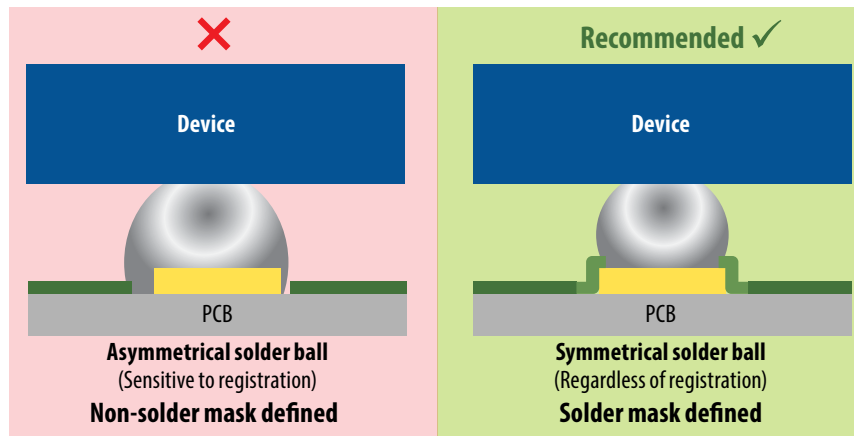


Figure 16: Effect of solder mask design on the solder ball symmetry

- Assembly resources – https://epc-co.com/epc/Portals/0/epc/documents/product-training/Appnote_GaNassembly.pdf
- Library of Altium footprints for production FETs and ICs – <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>
(for preliminary device Altium footprints, contact EPC)

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