

# MOSFET – Dual, P-Channel, POWERTRENCH<sup>®</sup>

**-20 V, -3.0 A, 120 mΩ**

## FDMA1027P

### General Description

This device is designed specifically as a single package solution for the battery charge switch in cellular handset and other ultra-portable applications. It features two independent P-Channel MOSFETs with low on-state resistance for minimum conduction losses. When connected in the typical common source configuration, bi-directional current flow is possible.

The MicroFET<sup>™</sup> 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

### Features

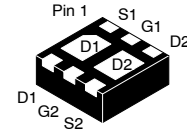
- -3.0 A, -20 V
  - ♦  $R_{DS(on)} = 120\text{ m}\Omega$  at  $V_{GS} = -4.5\text{ V}$
  - ♦  $R_{DS(on)} = 160\text{ m}\Omega$  at  $V_{GS} = -2.5\text{ V}$
  - ♦  $R_{DS(on)} = 240\text{ m}\Omega$  at  $V_{GS} = -1.8\text{ V}$
- Low Profile – 0.8 mm Maximum – In the New Package MicroFET 2x2 mm
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free, Halide Free and is RoHS Compliant

### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	MOSFET Drain-Source Voltage	-20	V
$V_{GSS}$	MOSFET Gate-Source Voltage	$\pm 8$	V
$I_D$	Drain Current –Continuous (Note 1a) –Pulsed	-3.0 -6	A
$P_D$	Power Dissipation (Note 1a) (Note 1b) (Note 1c) (Note 1d)	1.4 0.7 1.8 0.8	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

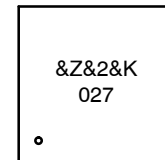
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
-20 V	120 mΩ @ -4.5 V	-3.0 A
	160 mΩ @ -2.5 V	
	240 mΩ @ -1.8 V	



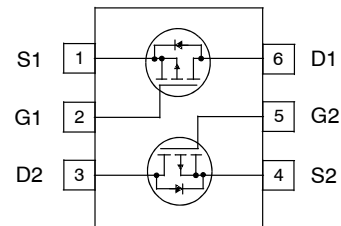
**WDFN6 2x2, 0.65P  
(MicroFET 2x2)  
CASE 511DA**

### MARKING DIAGRAM



&Z = Assembly Plant Code  
 &2 = 2-Digit Date Code  
 &K = 2-Digits Lot Run Traceability Code  
 027 = Device Code

### PIN CONNECTIONS



### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
FDMA1027P	WDFN6 (Pb-Free, Halide Free)	3000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](http://www.onsemi.com/BRD8011/D).

**THERMAL CHARACTERISTICS**

Symbol	Parameter	Ratings	Unit
$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient (Note 1a)	86	°C/W
$R_{\theta JA}$	Thermal Resistance for Single Operation, Junction to Ambient (Note 1b)	173	
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1c)	69	
$R_{\theta JA}$	Thermal Resistance for Dual Operation, Junction to Ambient (Note 1d)	151	

**ELECTRICAL CHARACTERISTICS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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**OFF CHARACTERISTICS**

$BV_{DSS}$	Drain-Source Breakdown Voltage	$I_D = -250\ \mu\text{A}$ , $V_{GS} = 0\ \text{V}$	-20	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	-12	-	mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\ \text{V}$ , $V_{GS} = 0\ \text{V}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	Gate-Body Leakage Current	$V_{GS} = \pm 8\ \text{V}$ , $V_{DS} = 0\ \text{V}$	-	-	$\pm 100$	nA

**ON CHARACTERISTICS** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$I_D = -250\ \mu\text{A}$ , $V_{DS} = V_{GS}$	-0.4	-0.7	-1.3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	2	-	mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\ \text{V}$ , $I_D = -3.0\ \text{A}$	-	90	120	m $\Omega$
		$V_{GS} = -2.5\ \text{V}$ , $I_D = -2.5\ \text{A}$	-	120	160	
		$V_{GS} = -1.8\ \text{V}$ , $I_D = -1.0\ \text{A}$	-	172	240	
		$V_{GS} = -4.5\ \text{V}$ , $I_D = -3.0\ \text{A}$ , $T_J = 125^\circ\text{C}$	-	118	160	
$g_{FS}$	Forward Transconductance	$I_D = -3.0\ \text{A}$ , $V_{DS} = -5\ \text{V}$	-	7	-	S

**DYNAMIC CHARACTERISTICS**

$C_{iss}$	Input Capacitance	$V_{DS} = -10\ \text{V}$ , $V_{GS} = 0\ \text{V}$ , $f = 1\ \text{MHz}$	-	435	-	pF
$C_{oss}$	Output Capacitance		-	80	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	45	-	pF

**SWITCHING CHARACTERISTICS** (Note 2)

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\ \text{V}$ , $I_D = -1\ \text{A}$ $V_{GS} = -4.5\ \text{V}$ , $R_{GEN} = 6\ \Omega$	-	9	18	ns
$t_r$	Turn-On Rise Time		-	11	19	ns
$t_{d(off)}$	Turn-Off Delay Time		-	15	27	ns
$t_f$	Turn-Off Fall Time		-	6	12	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\ \text{V}$ , $I_D = -3.0\ \text{A}$ , $V_{GS} = -4.5\ \text{V}$	-	4	6	nC
$Q_{gs}$	Gate-Source Charge		-	0.8	-	nC
$Q_{gd}$	Gate-Drain Charge		-	0.9	-	nC

**DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS**

I <sub>S</sub>	Maximum Continuous Drain–Source Diode Forward Current		–	–	–1.1	A
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = –1.1 A (Note 2)	–	–0.8	–1.2	V
t <sub>rr</sub>	Diode Reverse Recovery Time	I <sub>F</sub> = –3.0 A, di <sub>F</sub> /dt = 100 A/μs	–	17	–	ns
Q <sub>rr</sub>	Diode Reverse Recovery Charge		–	6	–	nC

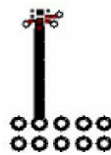
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

## NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
  - a.  $R_{\theta JA} = 86^{\circ}\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For single operation.
  - b.  $R_{\theta JA} = 173^{\circ}\text{C/W}$  when mounted on a minimum pad of 2 oz copper. For single operation.
  - c.  $R_{\theta JA} = 69^{\circ}\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick PCB. For dual operation, configured in parallel.
  - d.  $R_{\theta JA} = 151^{\circ}\text{C/W}$  when mounted on a minimum pad of 2 oz copper. For dual operation, configured in parallel.



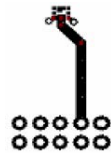
a.  $86^{\circ}\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b.  $173^{\circ}\text{C/W}$  when mounted on a minimum pad of 2 oz copper.



c.  $69^{\circ}\text{C/W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



d.  $151^{\circ}\text{C/W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%

## TYPICAL CHARACTERISTICS

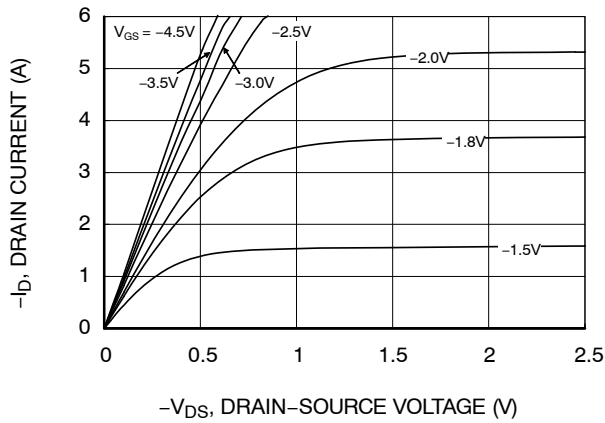


Figure 1. On-Region Characteristics

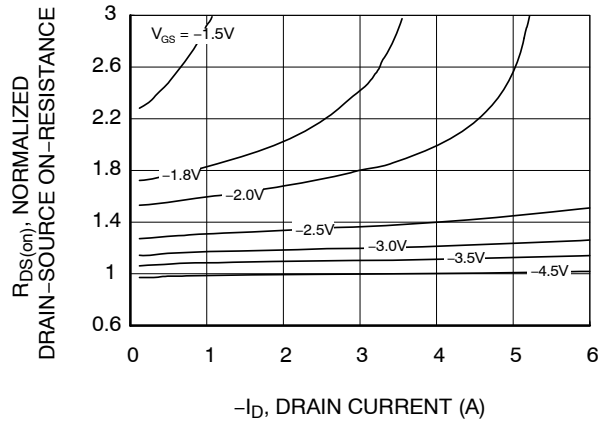


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

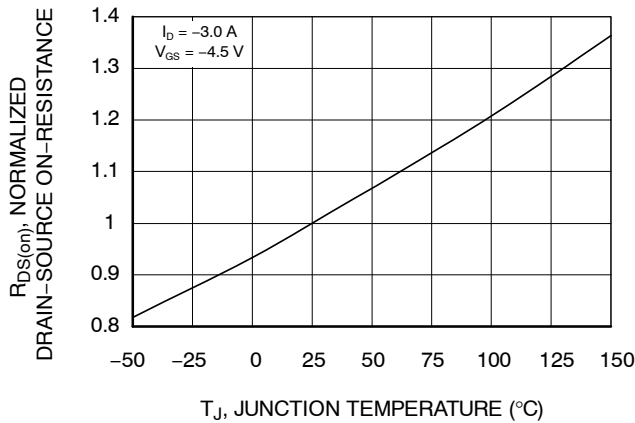


Figure 3. On-Resistance Variation with Temperature

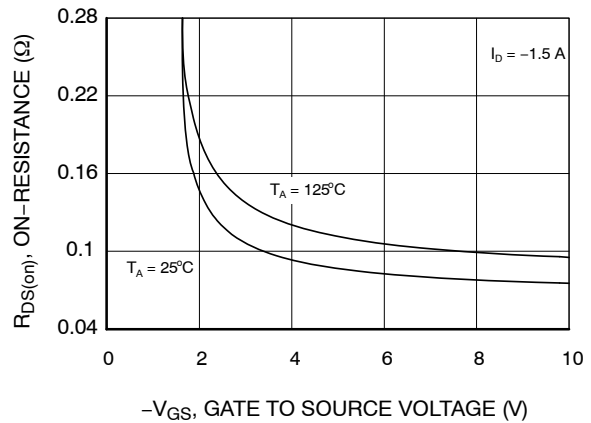


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

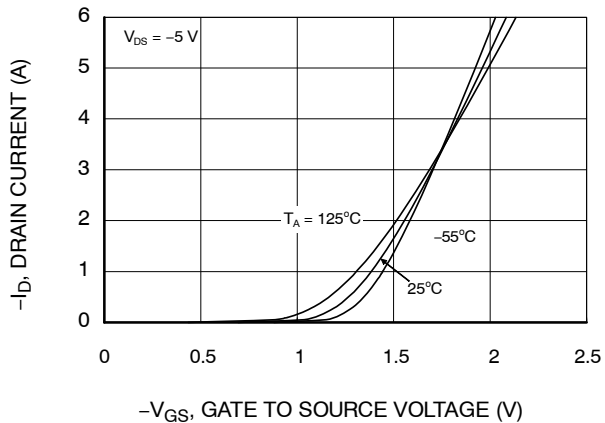


Figure 5. Transfer Characteristics

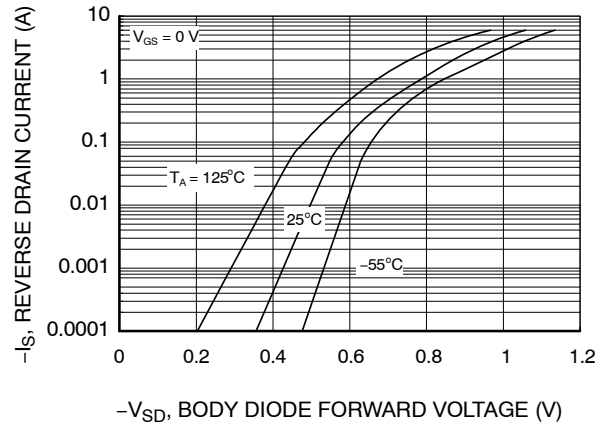


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

## TYPICAL CHARACTERISTICS (continued)

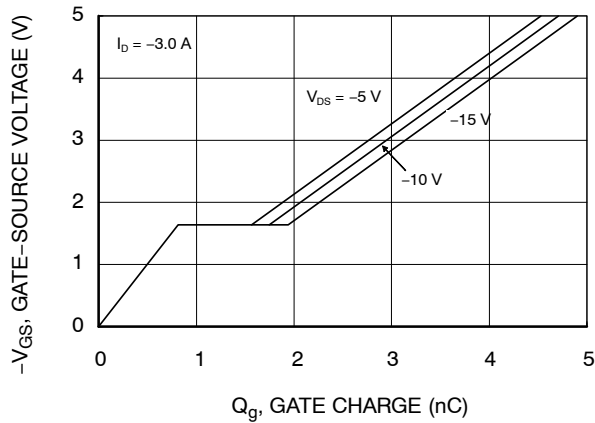


Figure 7. Gate Charge Characteristics

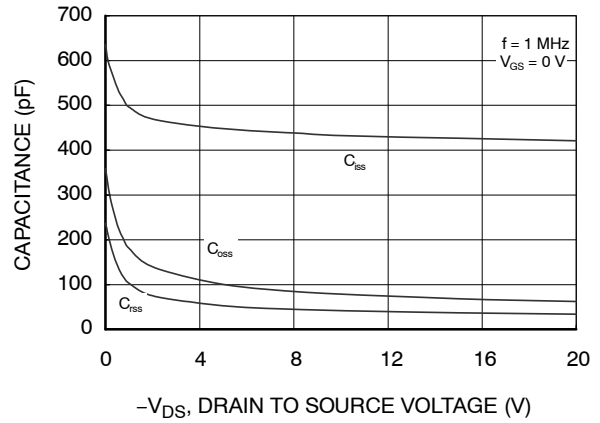


Figure 8. Capacitance Characteristics

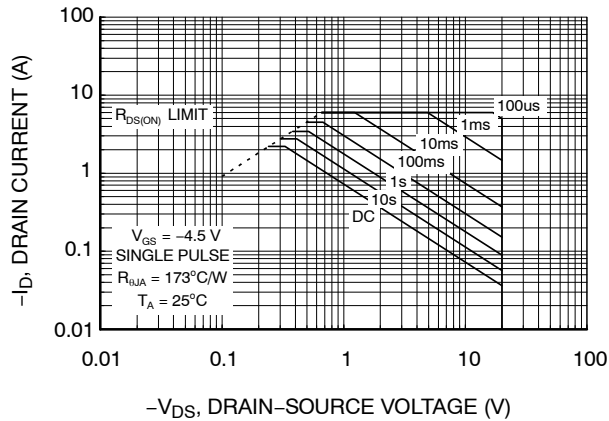


Figure 9. Maximum Safe Operating Area

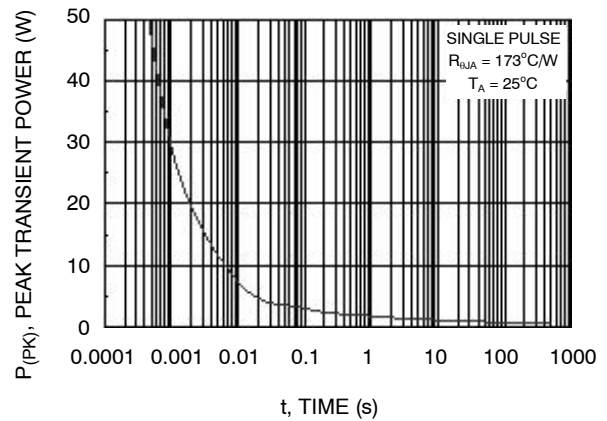


Figure 10. Single Pulse Maximum Power Dissipation

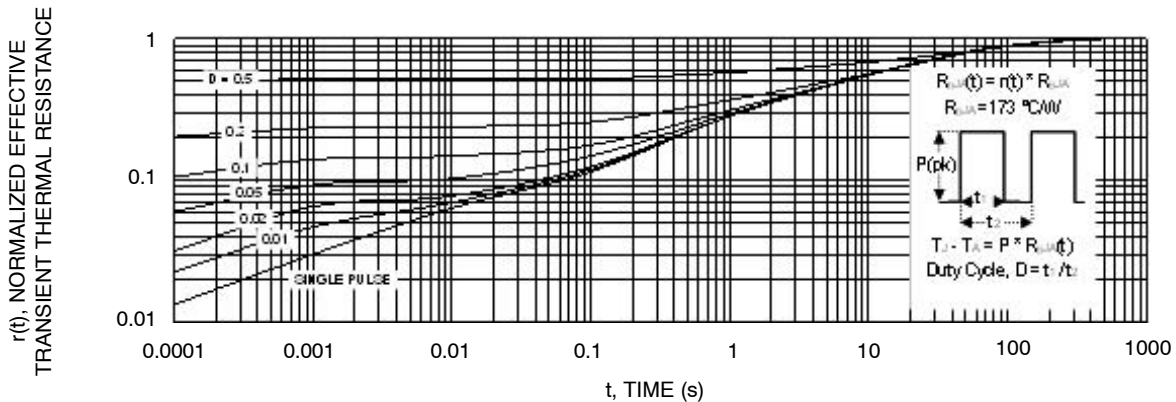
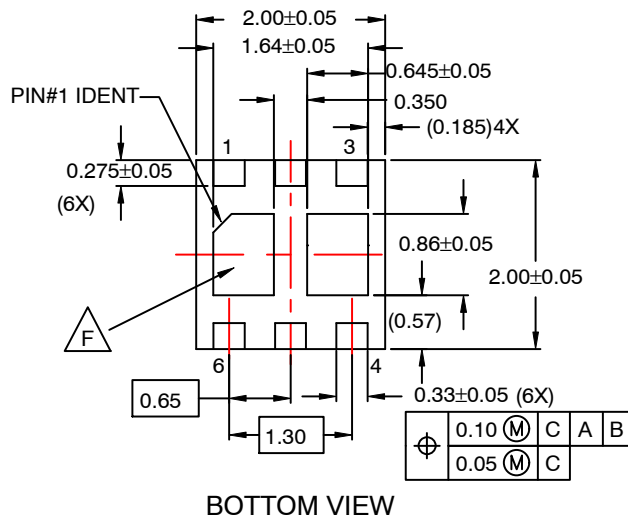
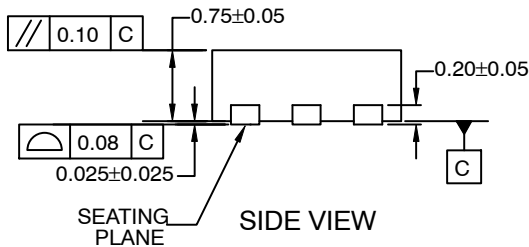
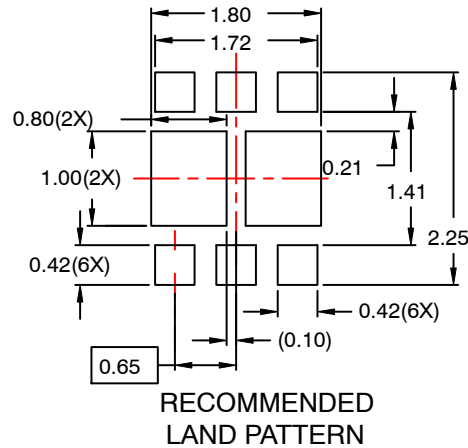
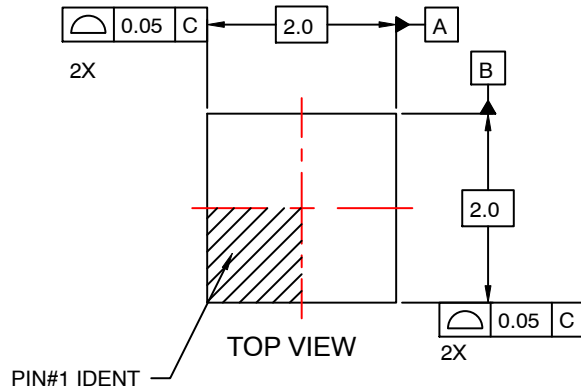


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.  
Transient thermal response will change depending on the circuit board design.

**WDFN6 2x2, 0.65P**  
**CASE 511DA**  
**ISSUE O**

DATE 31 JUL 2016



**NOTES:**

- CONFORM TO JEDEC REGISTRATIONS MO-229, VARIATION VCCC, EXCEPT WHERE NOTED.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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