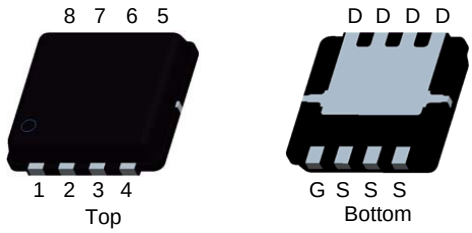
MOSFET – N-Channel, POWERTRENCH®

40 V, 18 A, 26 mΩ

FDMC8015L

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
40 V	26 mΩ @ 10 V	18 A
	36 mΩ @ 4.5 V	



WDFN8 3.3x3.3, 0.65P
CASE 511DR

General Description

This N−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain superior switching performance.

Features

- Max $R_{DS(on)}$ = 26 mΩ at V_{GS} = 10 V, I_D = 7 A
- Max $R_{DS(on)}$ = 36 mΩ at V_{GS} = 4.5 V, I_D = 6 A
- Low Profile − 1 mm Max in Power 33
- 100% UIL Tested
- This Device is Pb−Free, Halide Free and is RoHS Compliant

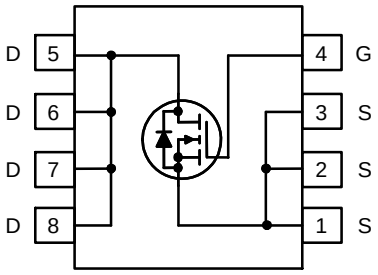
Applications

- Load Switch
- Motor Bridge Switch

MARKING DIAGRAM

&Z = Assembly Plant Code
&3 = 3−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
FDMC8015L = Device Code

PIN ASSIGNMENT



MOSFET MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current − Continuous (Package Limited) T_C = 25°C − Continuous (Silicon Limited) T_C = 25°C − Continuous T_A = 25°C (Note 1a) − Pulsed	 18 22 7 30	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	32	mJ
P_D	Power Dissipation T_C = 25°C T_A = 25°C (Note 1a)	 24 2.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	5.1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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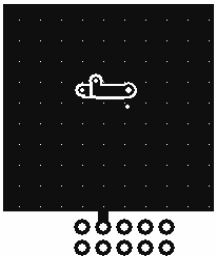
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

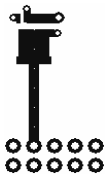
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	40	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	36	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 32 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1	1.8	3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	–	−6	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 7 A	–	19.7	26	mΩ
		V_{GS} = 4.5 V, I_D = 6 A	–	24	36	mΩ
		V_{GS} = 10 V, I_D = 7 A, T_J = 125°C	–	29	39	mΩ
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 7 A	–	30	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 20 V, V_{GS} = 0 V, f = 1 MHz	–	710	945	pF
C_{oss}	Output Capacitance		–	94	125	pF
C_{rss}	Reverse Transfer Capacitance		–	58	90	pF
R_g	Gate Resistance		–	1.2	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 20 V, I_D = 7 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	6.3	13	ns
t_r	Rise Time		–	1.9	10	ns
$t_{d(off)}$	Turn−Off Delay Time		–	18	33	ns
t_f	Fall Time		–	1.7	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 20 V, I_D = 7 A	–	13.6	19	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V, V_{DD} = 20 V, I_D = 7 A	–	6.6	10	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 20 V, I_D = 7 A	–	1.9	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 20 V, I_D = 7 A	–	2.5	–	nC
DRAIN−SOURCE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7 A (Note 2)	–	0.84	1.2	V
		V_{GS} = 0 V, I_S = 2 A (Note 2)	–	0.76	1.1	V
t_{rr}	Reverse Recovery Time	I_F = 7 A, di/dt = 100 A/μs	–	18	33	ns
Q_{rr}	Reverse Recovery Charge		–	8.6	18	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Starting T_J = 25°C; N−ch: L = 1 mH, I_{AS} = 8 A, V_{DD} = 36 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted)

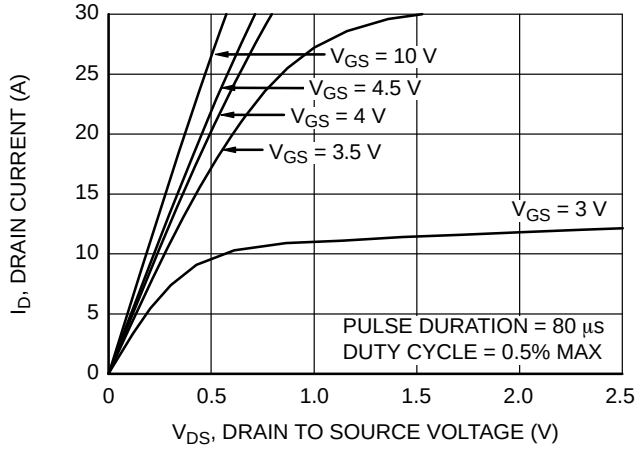


Figure 1. On Region Characteristics

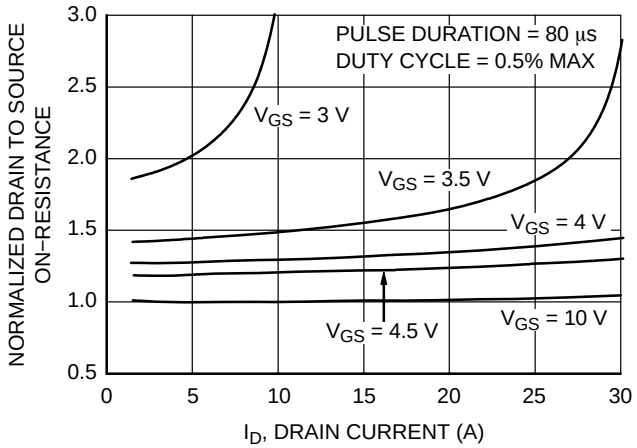


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

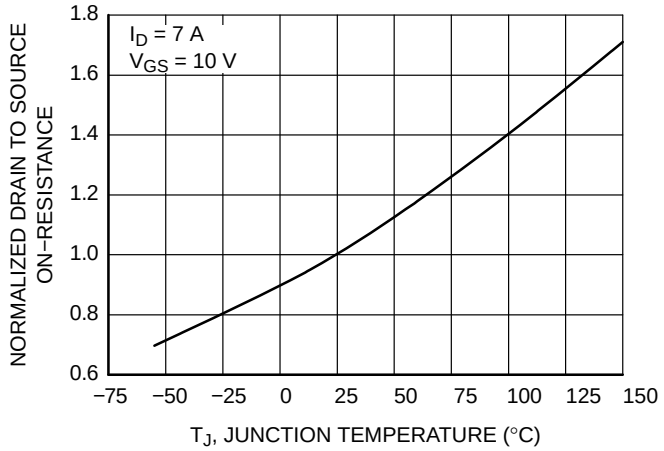


Figure 3. Normalized On Resistance vs. Junction Temperature

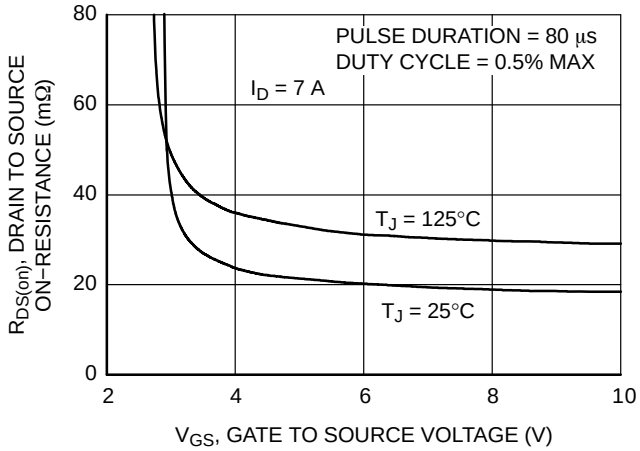


Figure 4. On−Resistance vs. Gate to Source Voltage

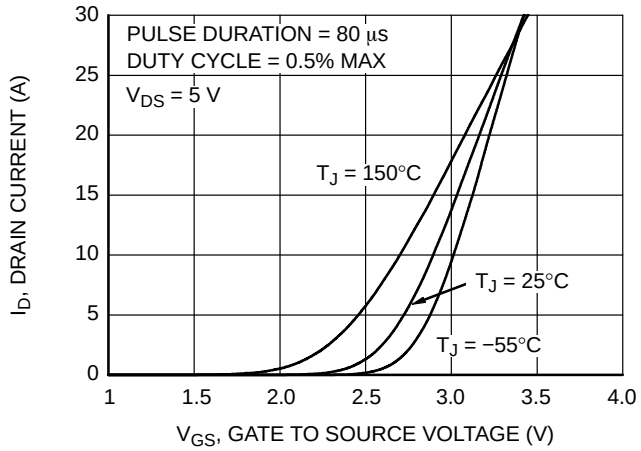


Figure 5. Transfer Characteristics

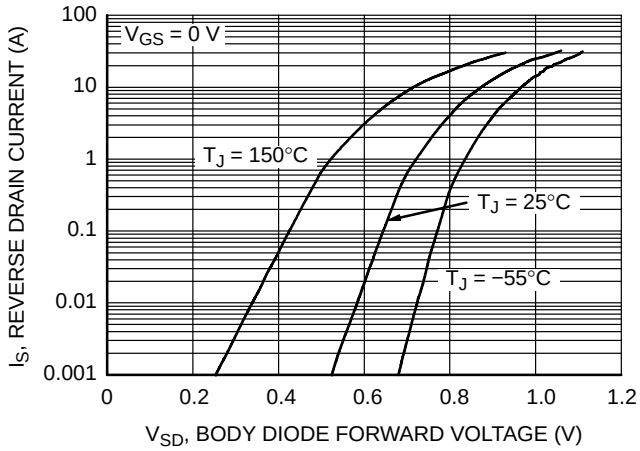


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

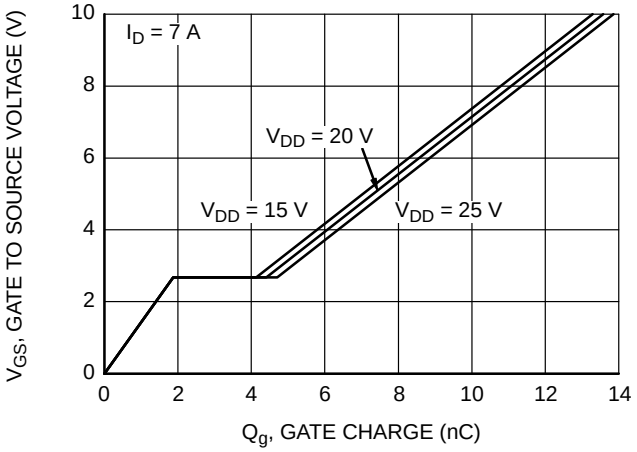


Figure 7. Gate Charge Characteristics

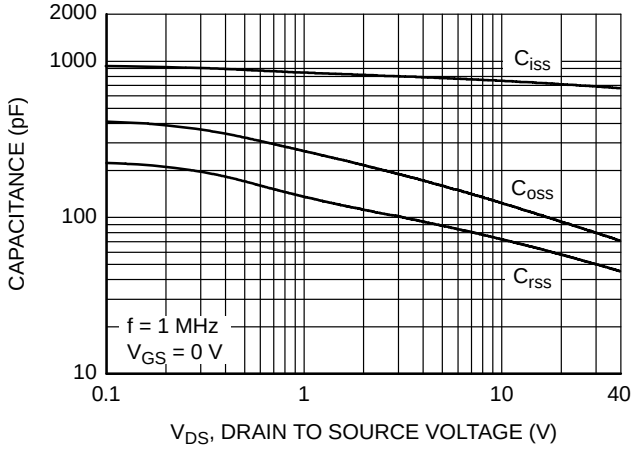


Figure 8. Capacitance vs. Drain to Source Voltage

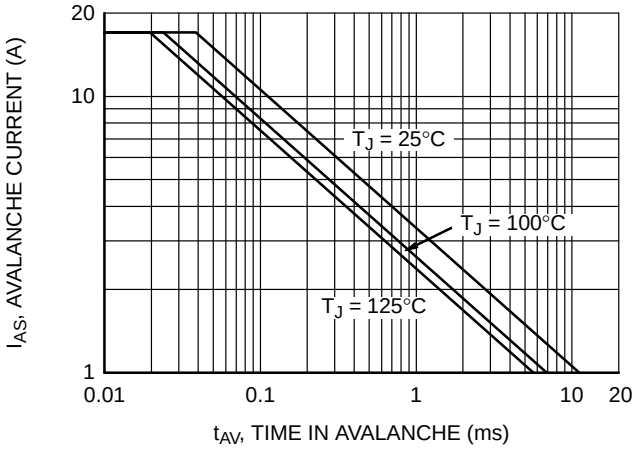


Figure 9. Unclamped Inductive Switching Capability

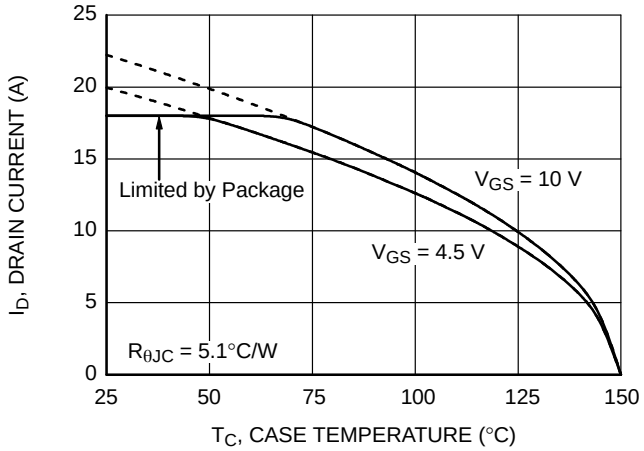


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

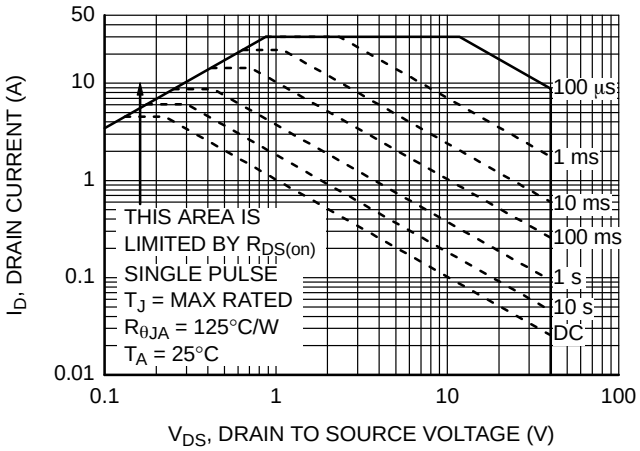


Figure 11. Forward Bias Safe Operating Area

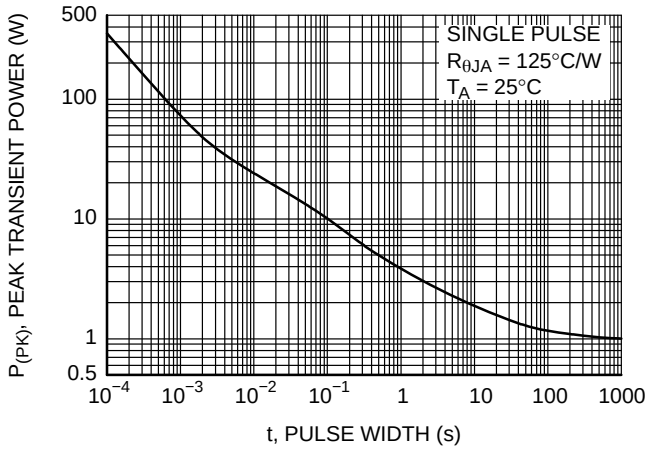


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25°C, unless otherwise noted) (continued)

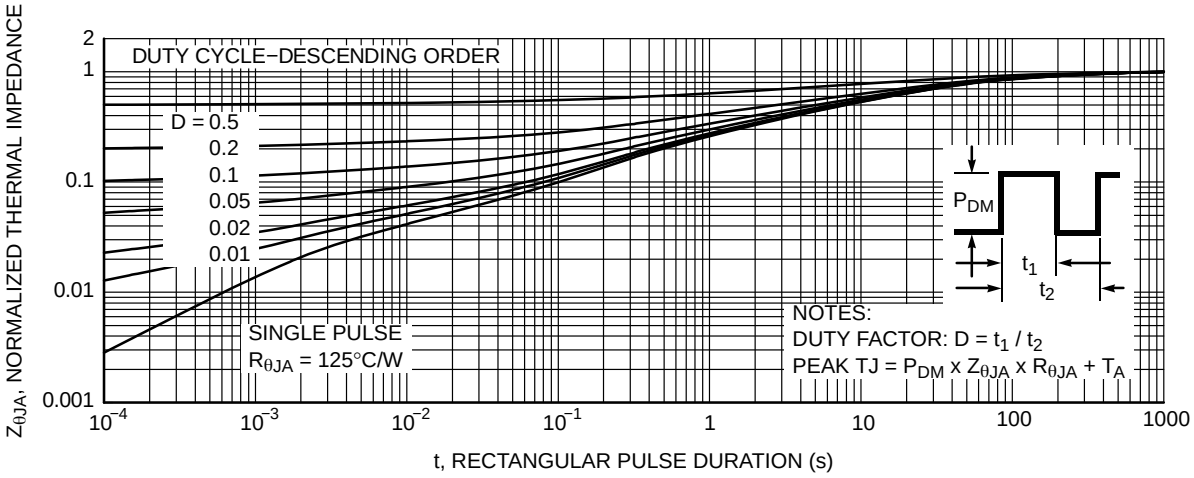


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMC8015L	FDMC8015L	WDFN8 3.3x3.3, 0.65P (Pb−Free, Halide Free)	13”	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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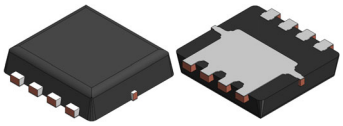
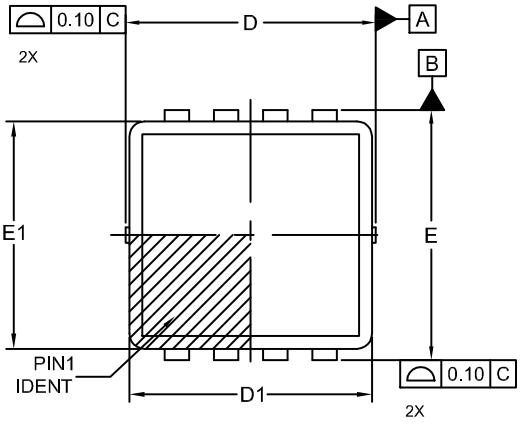
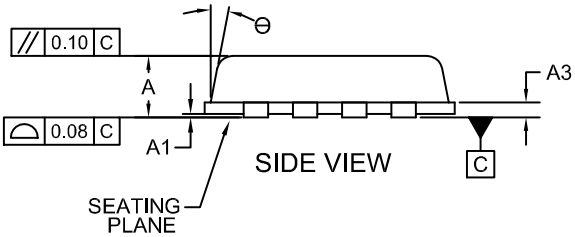


WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE B

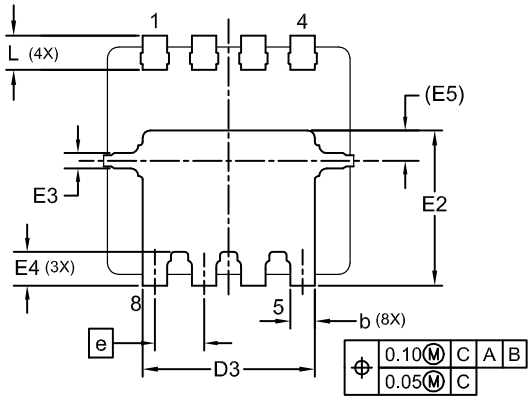
DATE 02 FEB 2022



TOP VIEW



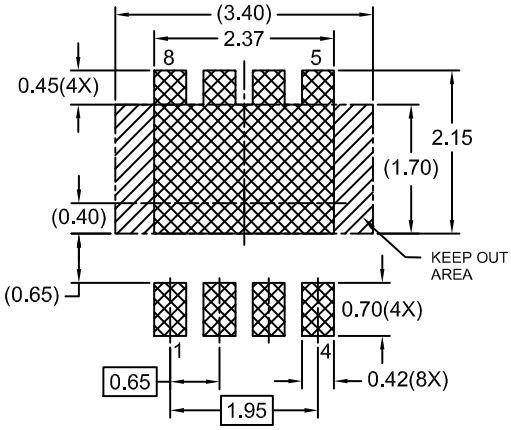
SIDE VIEW



BOTTOM VIEW

NOTES:
A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
Θ	0°	-	12°



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	WDFN8 3.3x3.3, 0.65P	PAGE 1 OF 1

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