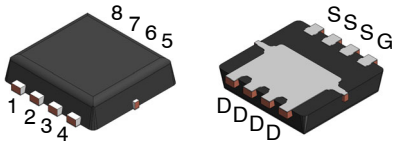
# MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

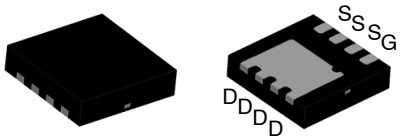
## 100 V, 7.5 A, 103 mΩ

# FDMC86116LZ, FDMC86116LZ-L701




Top Bottom

**WDFN8 3.3x3.3, 0.65P**
**CASE 511DR**
FDMC86116LZ




Top Bottom

**WDFN8 3.3x3.3, 0.65P**
**CASE 511DQ**
FDMC86116LZ−L701

### General Description

This N−Channel logic Level MOSFETs are produced using **onsemi**'s advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized for the on−state resistance and yet maintain superior switching performance. G−S zener has been added to enhance ESD voltage level.

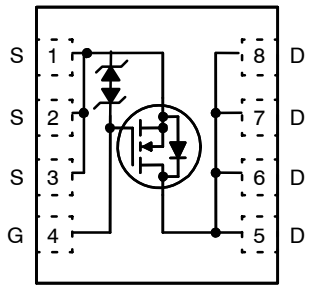
### Features

- Max $R_{DS(on)}$ = 103 mΩ at $V_{GS}$ = 10 V, $I_D$ = 3.3 A
- Max $R_{DS(on)}$ = 153 mΩ at $V_{GS}$ = 4.5 V, $I_D$ = 2.7 A
- HBM ESD Protection Level > 3 kV Typical (Note 1)
- 100% UIL Tested
- These Devices are Pb−Free and are RoHS Compliant

### Applications

- DC−DC Conversion

### PIN ASSIGNMENT




### MARKING DIAGRAM

FDMC86116LZ FDMC86116LZ−L701

| | |
|---|---|
| FDMC86116Z | = Specific Device Code |
| A | = Assembly Site |
| XY | = 2−Digit Date Code |
| KK | = 2−Digit Lot Run Traceability Code |
| L | = Wafer Lot Number |
| YW | = Assembly Start Week |

### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

1. The diode connected between gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

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**MOSFET MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | | | Ratings | Unit |
|---|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | | 100 | V |
| $V_{GS}$ | Gate to Source Voltage | | | ±20 | V |
| $I_D$ | Drain Current | Continuous | $T_C$ = 25°C | 7.5 | A |
| | | Continuous (Note 3a) | $T_A$ = 25°C | 3.3 | |
| | | Pulsed | | 15 | |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 2) | | | 12 | mJ |
| $P_D$ | Power Dissipation | | $T_C$ = 25°C | 19 | W |
| | Power Dissipation (Note 3a) | | $T_A$ = 25°C | 2.3 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | | −55 to +150 | °C |

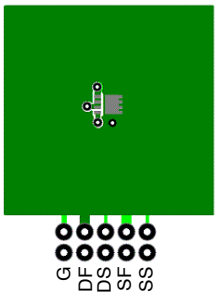
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Starting $T_J$ = 25°C; N−ch: L = 1 mH, $I_{AS}$ = 5.0 A, $V_{DD}$ = 90 V, $V_{GS}$ = 10 V.

**THERMAL CHARACTERISTICS**

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | 6.5 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 3a) | 53 | |

3. $R_{\theta JA}$ is determined with the device mounted on a 1 in$^2$ pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined bythe user's board design.




a. 53°C/W when mounted on a 1 in$^2$ pad of 2 oz copper

b. 125°C/W when mounted on a minimum pad of 2 oz copper

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 100 | – | – | V |
| $\Delta BV_{DSS}$ / $\Delta T_J$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | 73 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 80 V, $V_{GS}$ = 0 V | – | – | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | – | – | ±10 | μA |
| **ON CHARACTERISTICS** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 1.0 | 1.8 | 2.2 | V |
| $\Delta V_{GS(th)}$ / $\Delta T_J$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25°C | – | –6 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 3.3 A | – | 79 | 103 | mΩ |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 2.7 A | – | 105 | 153 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 3.3 A, $T_J$ = 125°C | – | 136 | 178 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 5 V, $I_D$ = 3.3 A | – | 11 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 50 V, $V_{GS}$ = 0 V, f = 1 MHz | – | 232 | 310 | pF |
| $C_{oss}$ | Output Capacitance | | – | 45 | 60 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 2.4 | 5 | pF |
| $R_g$ | Gate Resistance | | – | 0.7 | – | Ω |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| $t_{d(on)}$ | Turn−On Delay Time | $V_{DD}$ = 50 V, $I_D$ = 3.3 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | – | 4.5 | 10 | ns |
| $t_r$ | Rise Time | | – | 1.3 | 10 | ns |
| $t_{d(off)}$ | Turn−Off Delay Time | | – | 10 | 20 | ns |
| $t_f$ | Fall Time | | – | 1.4 | 10 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V, $V_{DD}$ = 50 V, $I_D$ = 3.3 A | – | 4 | 6 | nC |
| $Q_{g(TOT)}$ | Total Gate Charge | $V_{GS}$ = 0 V to 4.5 V, $V_{DD}$ = 50 V, $I_D$ = 3.3 A | – | 2 | 3 | nC |
| $Q_{gs}$ | Total Gate Charge | $V_{DD}$ = 50 V, $I_D$ = 3.3 A | – | 0.8 | – | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | – | 0.7 | – | nC |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 3.3 A (Note 4) | – | 0.85 | 1.3 | V |
| | | $V_{GS}$ = 0 V, $I_S$ = 2 A (Note 4) | – | 0.82 | 1.2 | |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 3.3 A, di/dt = 100 A/μs | – | 33 | 54 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | – | 23 | 38 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

## TYPICAL CHARACTERISTICS ($T_J$ = 25°C UNLESS OTHERWISE NOTED)

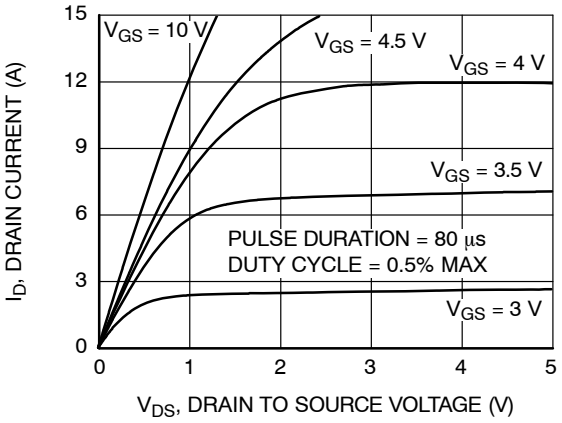



**Figure 1. On Region Characteristics**

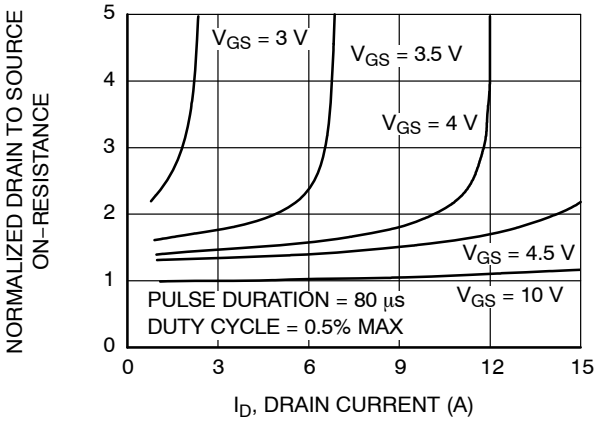



**Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage**

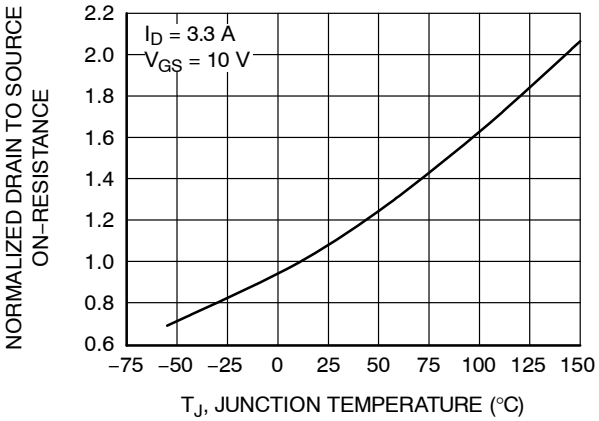



**Figure 3. Normalized On Resistance vs. Junction Temperature**

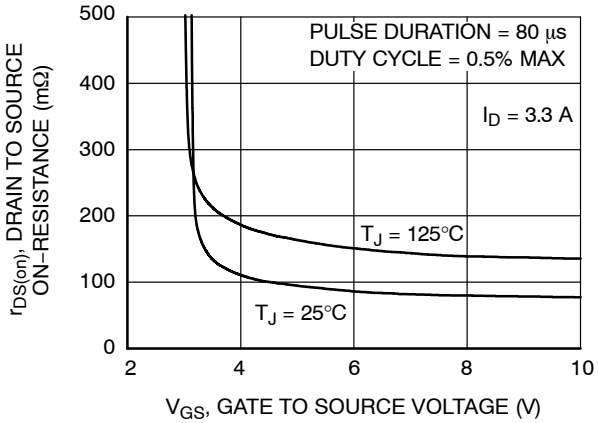



**Figure 4. On−Resistance vs. Gate to Source Voltage**

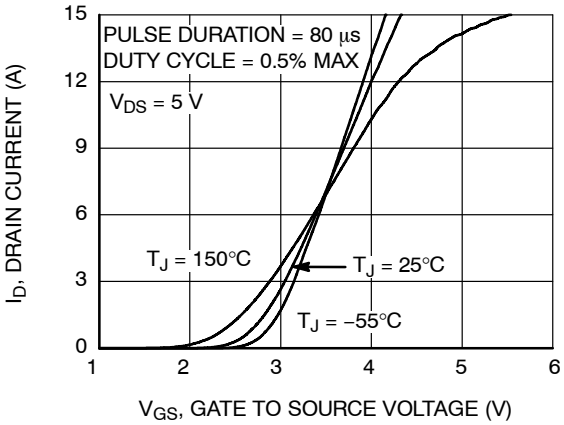



**Figure 5. Transfer Characteristics**

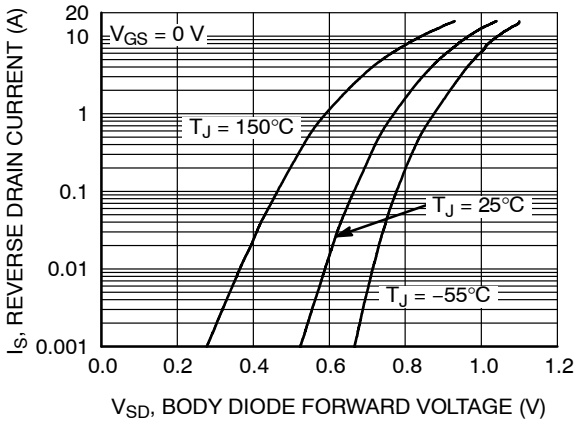



**Figure 6. Source to Drain Diode Forward Voltage vs. Source Current**

## TYPICAL CHARACTERISTICS (CONTINUED)

($T_J$ = 25°C UNLESS OTHERWISE NOTED)

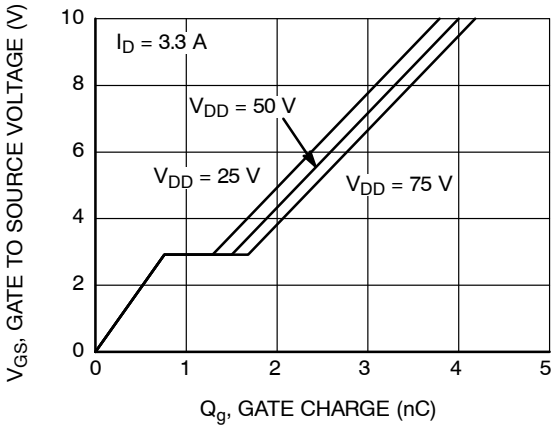



**Figure 7. Gate Charge Characteristics**

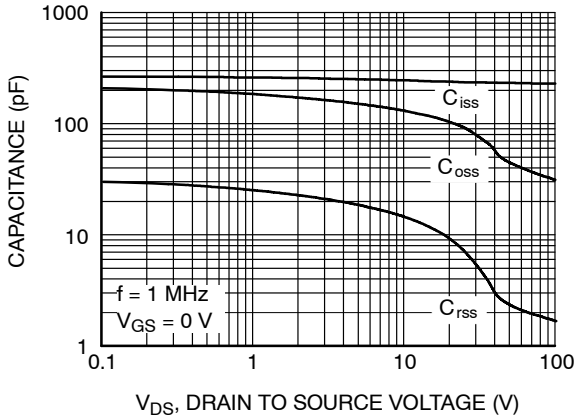



**Figure 8. Capacitance vs. Drain to Source Voltage**

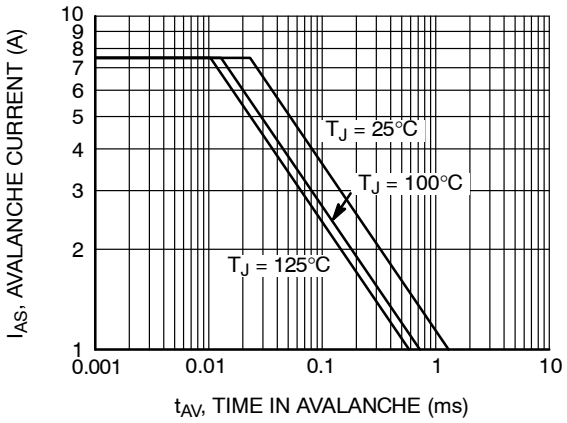



**Figure 9. Unclamped Inductive Switching Capability**

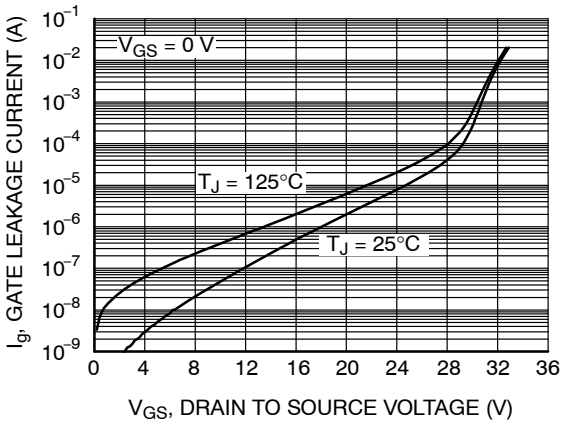



**Figure 10. Gate Leakage Current vs. Gate to Source Voltage**

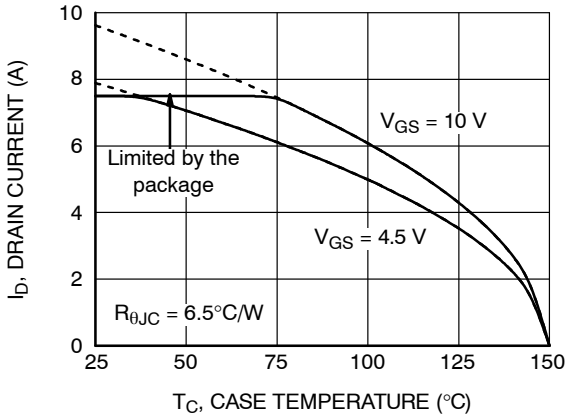



**Figure 11. Maximum Continuous Drain Current vs. Case Temperature**

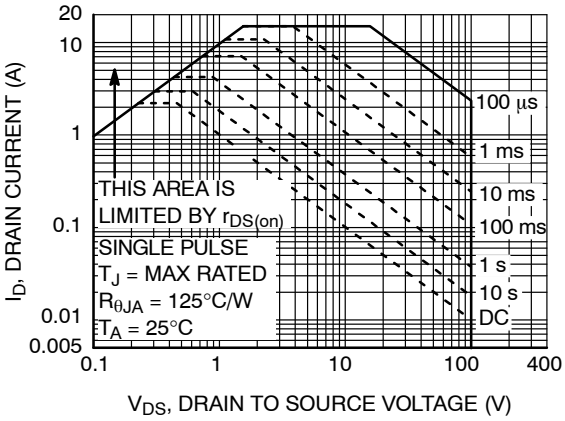



**Figure 12. Forward Bias Safe Operating Area**

## TYPICAL CHARACTERISTICS (CONTINUED)

($T_J$ = 25°C UNLESS OTHERWISE NOTED)

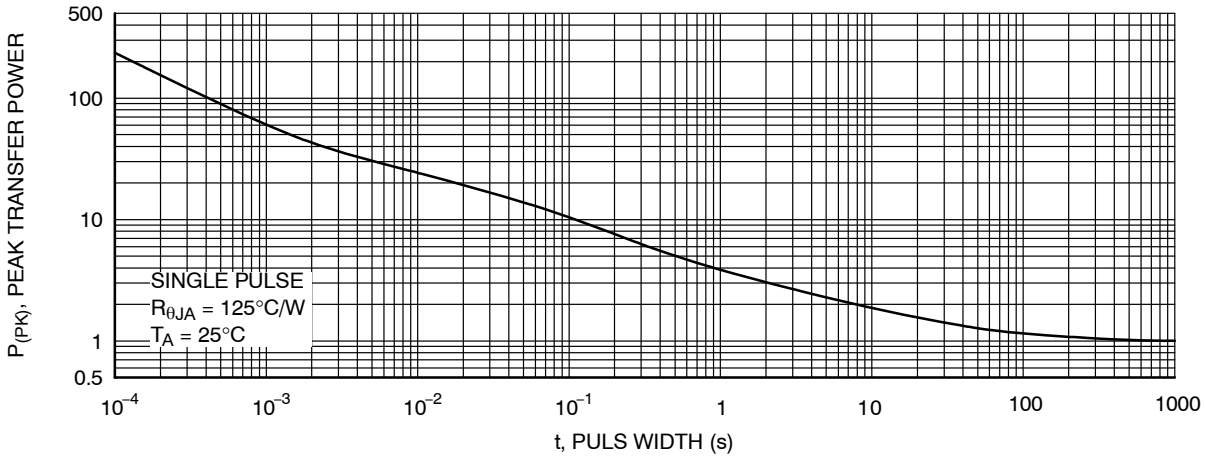



**Figure 13. Single pulse Maximum Power Dissipation**

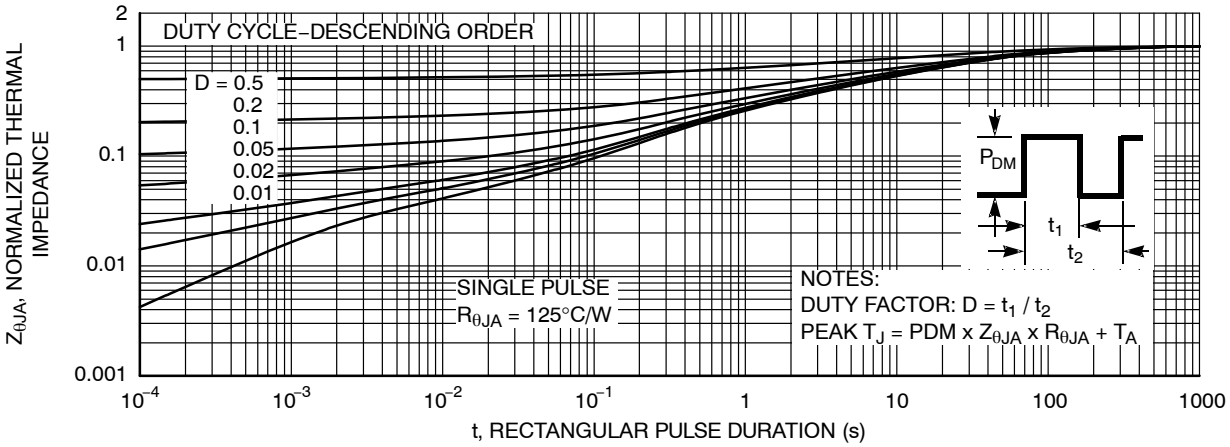



**Figure 14. Junction−to−Ambient Transient Thermal Response Curve**

## ORDERING INFORMATION

| Device | Device Marking | Package Type | Reel Size | Tape Width | Shipping† |
|---|---|---|---|---|---|
| FDMC86116LZ | FDMC86116Z | WDFN8 3.3x3.3, 0.65P Power 33 (Pb−Free) | 13” | 12 mm | 3000 / Tape & Reel |
| FDMC86116LZ−L701 | FDMC86116Z | WDFN8 3.3x3.3, 0.65P Power 33 (Pb−Free) | 13” | 12 mm | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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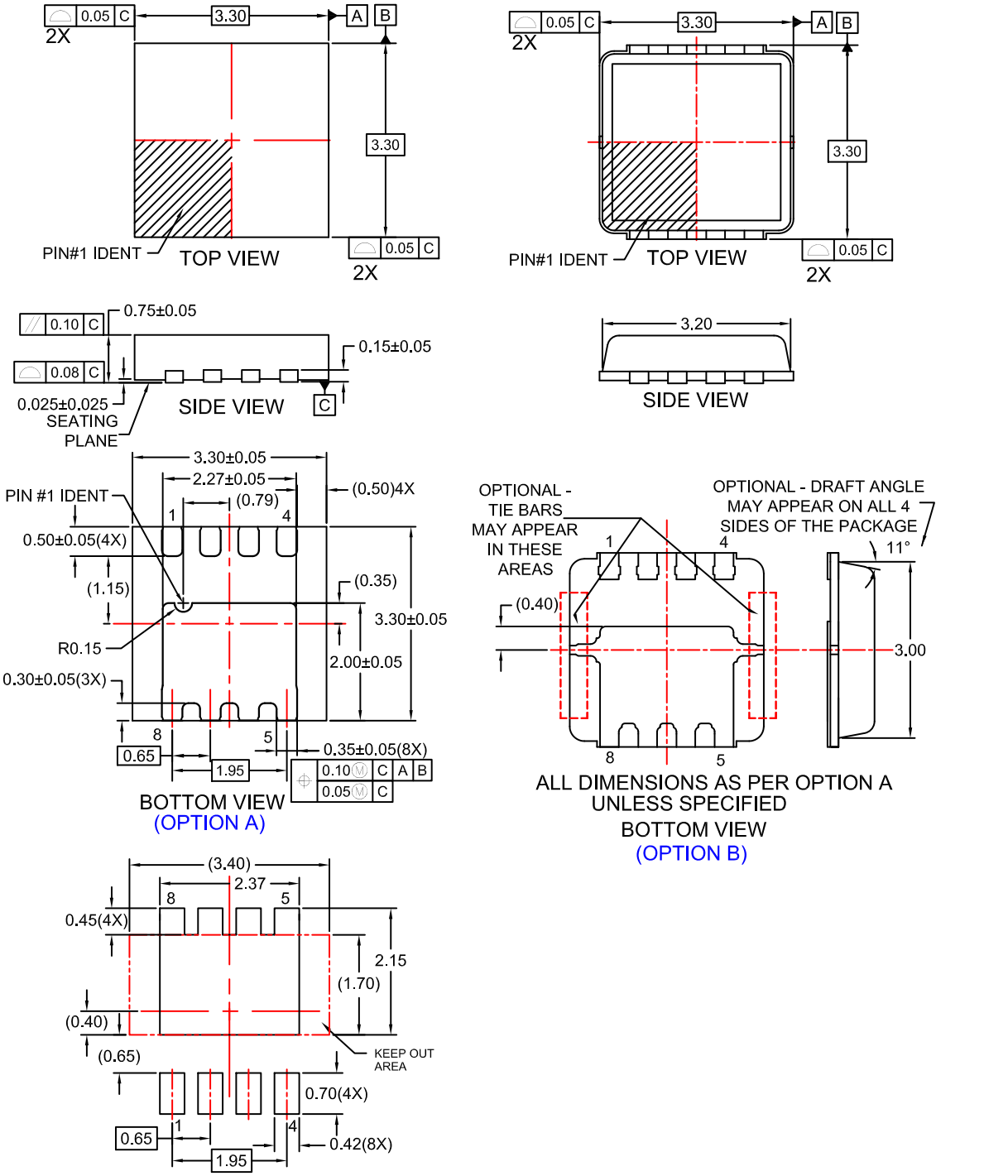
**WDFN8 3.3x3.3, 0.65P**
CASE 511DQ
ISSUE O

DATE 31 OCT 2016

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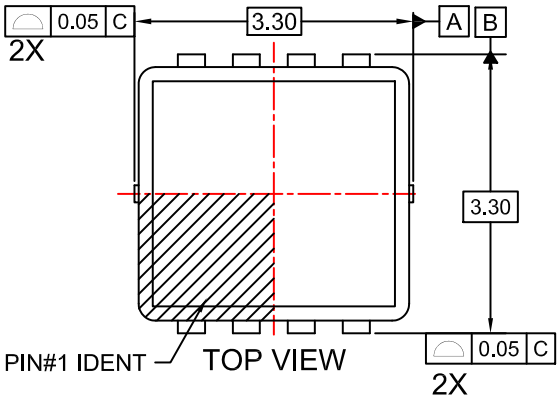
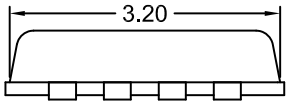
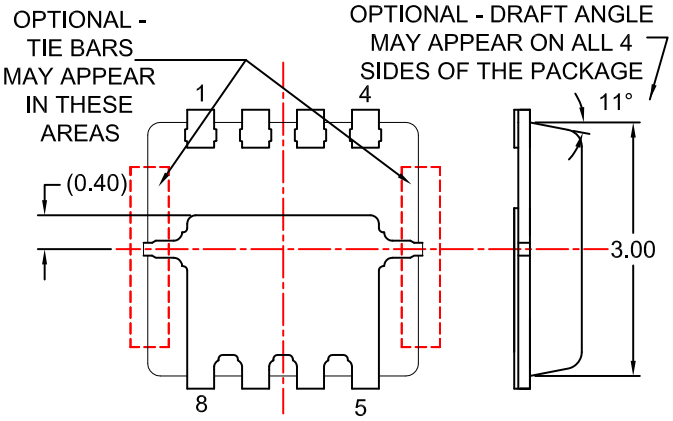
**WDFN8 3.3x3.3, 0.65P**
CASE 511DQ
ISSUE O

DATE 31 OCT 2016




SIDE VIEW




ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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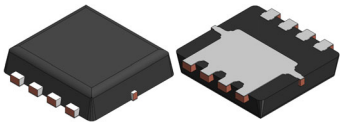
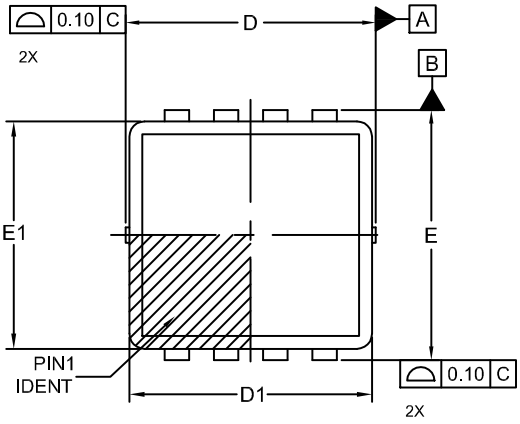
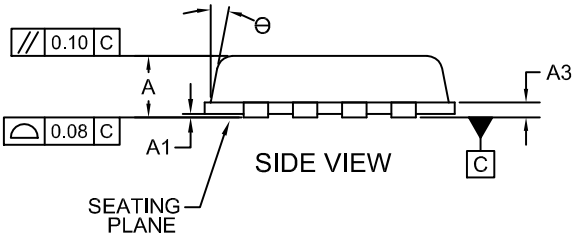


**WDFN8 3.3x3.3, 0.65P**
CASE 511DR
ISSUE B

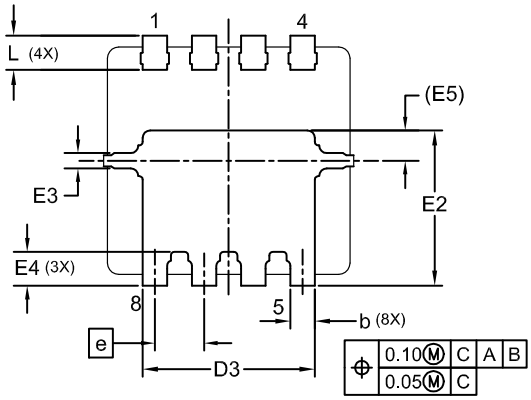
DATE 02 FEB 2022




TOP VIEW



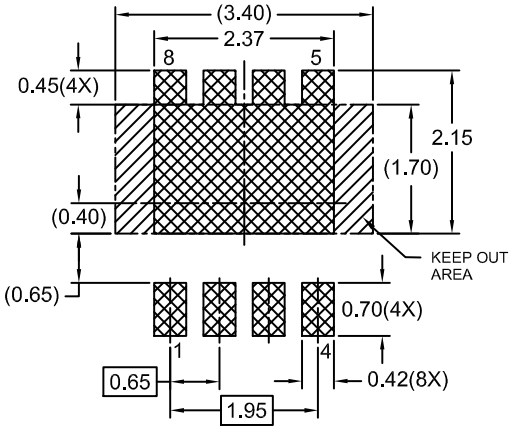

SIDE VIEW




BOTTOM VIEW

NOTES:
A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | - | 0.05 |
| A3 | 0.15 | 0.20 | 0.25 |
| b | 0.27 | 0.32 | 0.37 |
| D | 3.20 | 3.30 | 3.40 |
| D1 | 3.10 | 3.20 | 3.30 |
| D3 | 2.17 | 2.27 | 2.37 |
| E | 3.20 | 3.30 | 3.40 |
| E1 | 2.90 | 3.00 | 3.10 |
| E2 | 1.95 | 2.05 | 2.15 |
| E3 | 0.15 | 0.20 | 0.25 |
| E4 | 0.30 | 0.40 | 0.50 |
| E5 | 0.40 REF | | |
| e | 0.65 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| Θ | 0° | - | 12° |




RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

**GENERIC MARKING DIAGRAM***

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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