

MOSFET – Dual, N-Channel POWERTRENCH®

40 V, 103 A, 2.6 mΩ

FDMD8240LET40

Description

This Device Includes Two 40V N-Channel MOSFETs in a Dual Power (3.3 mm x 5 mm) package. HS source and LS Drain are internally connected for half/full bridge, low source inductance package, low $R_{DS(on)}$ /Qg FOM silicon.

Features

- Extended T_J Rating to 175°C
- Max $R_{DS(on)}$ = 2.6 mΩ at V_{GS} = 10 V, I_D = 23 A
- Max $R_{DS(on)}$ = 3.95 mΩ at V_{GS} = 4.5 V, I_D = 19 A
- Ideal for Flexible Layout in Primary Side of Bridge Topology
- 100% UIL Tested
- Kelvin High Side MOSFET Drive Pin-out Capability
- These Device is Pb-Free, Halide Free, and is RoHS Compliant

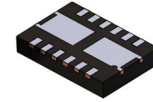
Typical Applications

- Synchronous Buck : Primary Switch of Half / Full Bridge Converter for Telecom
- Motor Bridge : Primary Switch of Half / Full bridge Converter for BLDC Motor
- MV POL : Synchronous Buck Switch

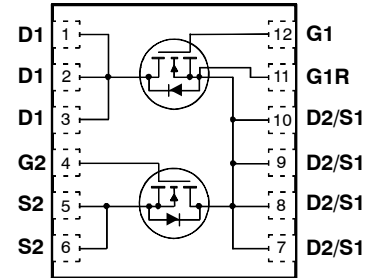
MOSFET MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current – Continuous $T_C = 25^\circ\text{C}$ (Note 5) – Continuous $T_C = 100^\circ\text{C}$ (Note 5) – Continuous $T_A = 25^\circ\text{C}$ (Note 1 a) – Pulsed (Note 4)	103 73 24 489	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	216	mJ
P_D	Power Dissipation $T_C = 25^\circ\text{C}$	50	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1 a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +175	°C

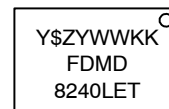
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



PQFN12 3.3X5, 0.65P
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MARKING DIAGRAM



\$Y	= onsemi Logo
Z	= Assembly Plant Code
YWW	= Date Code (Year & Week)
KK	= Lot Traceability Code
FDMD8240LET	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMD8240LET40	PQFN12 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

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THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1 a)	60	°C/W

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	40	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	23	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	1.0	2.0	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	–6	–	mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 23\ \text{A}$ $V_{GS} = 4.5\ \text{V}$, $I_D = 19\ \text{A}$, $V_{GS} = 10\ \text{V}$, $I_D = 23\ \text{A}$, $T_J = 150^\circ\text{C}$	–	2.0 3.2 3.3	2.6 3.95 4.3	m Ω
g_{FS}	Forward Transconductance	$V_{DD} = 5\ \text{V}$, $I_D = 23\ \text{A}$	–	107	–	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 20\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	3020	4230	pF
C_{oss}	Output Capacitance		–	876	1230	pF
C_{rss}	Reverse Transfer Capacitance		–	33	52	pF
R_g	Gate Resistance		0.1	2.8	6	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 20\ \text{V}$, $I_D = 23\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	12	22	ns
t_r	Rise Time		–	8	16	ns
$t_{d(off)}$	Turn-Off Delay Time		–	36	58	ns
t_f	Fall Time		–	9	18	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$, to $10\ \text{V}$, $V_{DD} = 20\ \text{V}$, $I_D = 23\ \text{A}$	–	40	56	nC
	Total Gate Charge	$V_{GS} = 0\ \text{V}$, to $5\ \text{V}$, $V_{DD} = 20\ \text{V}$, $I_D = 23\ \text{A}$	–	21	30	nC
Q_{gs}	Gate-Source Charge	$V_{DD} = 20\ \text{V}$, $I_D = 23\ \text{A}$	–	9	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	5	–	nC

Drain-Source Diode Characteristics

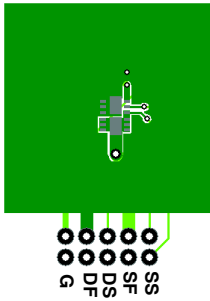
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 23\ \text{A}$ (Note 2)	–	0.8	1.3	V
		$V_{GS} = 0\ \text{V}$, $I_S = 1.6\ \text{A}$ (Note 2)	–	0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 23\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	–	41	65	ns
Q_{rr}	Reverse Recovery Charge		–	21	32	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

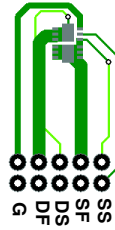
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NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 60 °C/W when mounted on
a 1 in² pad of 2 oz copper



b. 130 °C/W when mounted on
a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2.0\%$
3. E_{AS} of 216 mJ is based on starting $T_J = 25^\circ C$, $L = 3 mH$, $I_{AS} = 12 A$, $V_{DD} = 40 V$, $V_{GS} = 10 V$. 100% tested at $L = 0.1 mH$, $I_{AS} = 37 A$.
4. Pulsed I_d please refer to Figure 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED

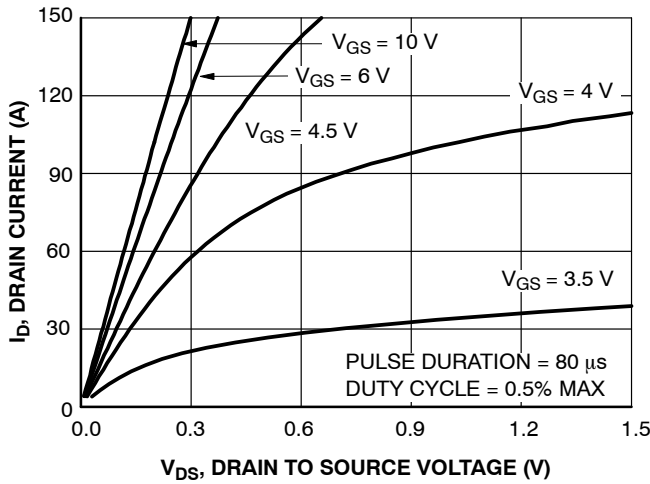


Figure 1. On-Region Characteristics

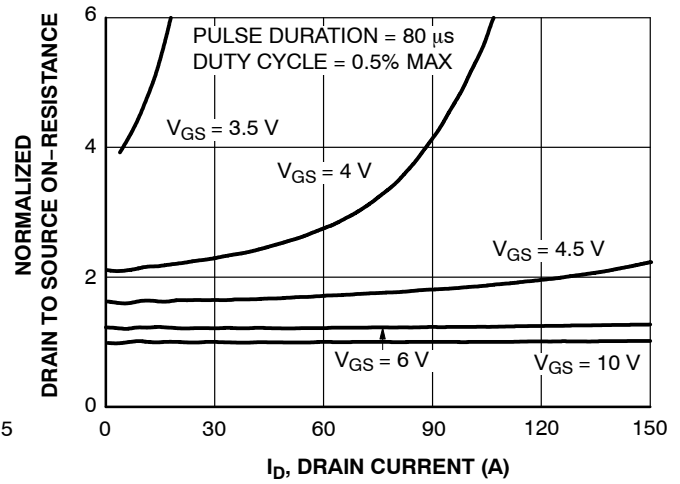


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

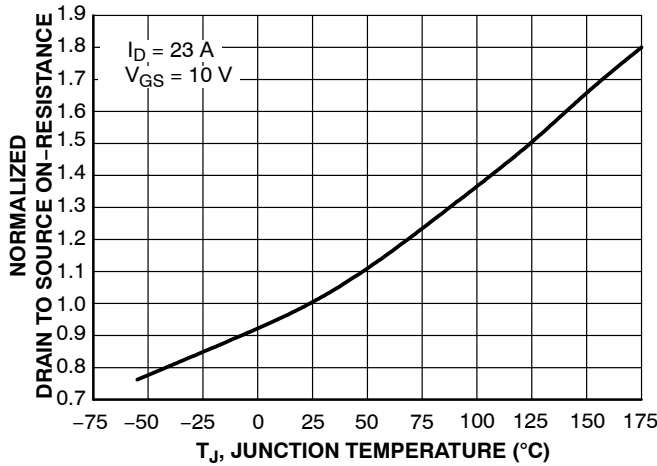


Figure 3. Normalized On Resistance vs. Junction Temperature

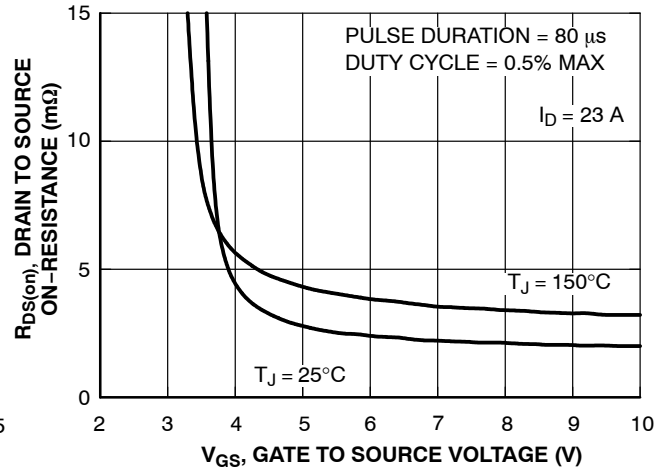


Figure 4. On Resistance vs. Gate to Source Voltage

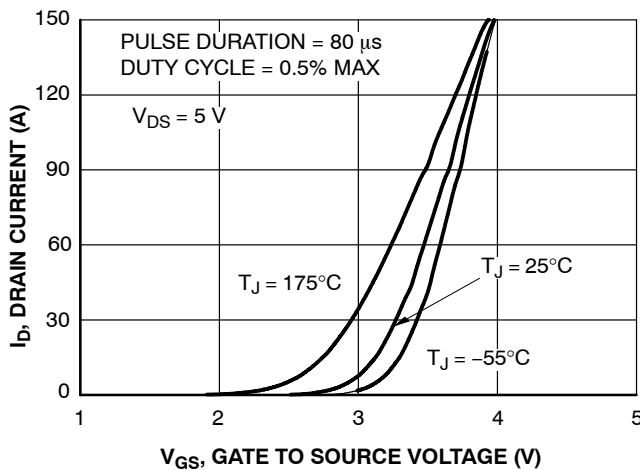


Figure 5. Transfer Characteristics

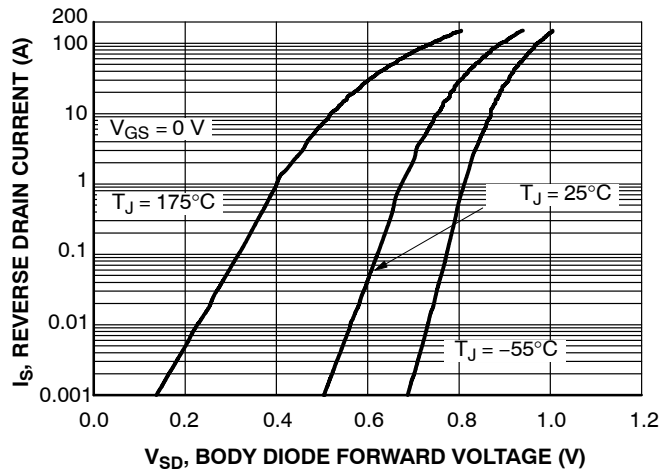


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (CONTINUED) $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED

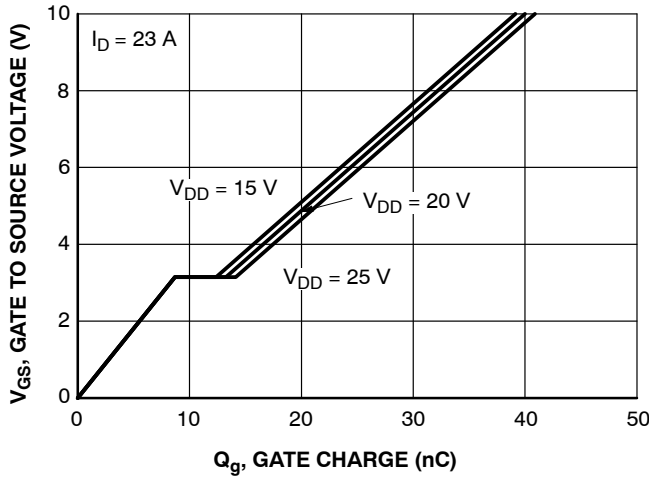


Figure 7. Gate Charge Characteristics

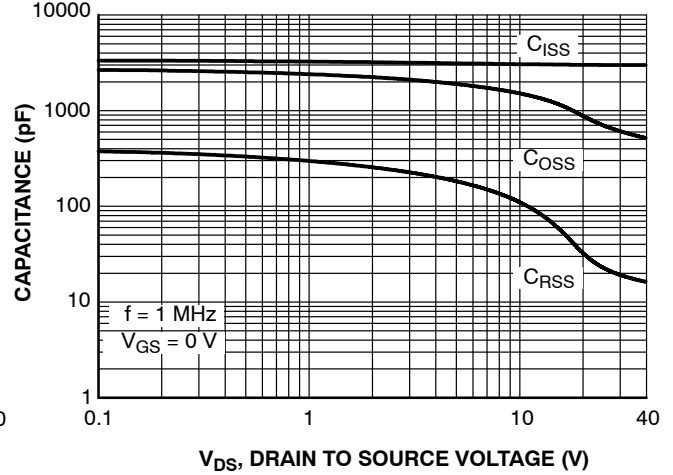


Figure 8. Capacitance vs. Drain to Source Voltage

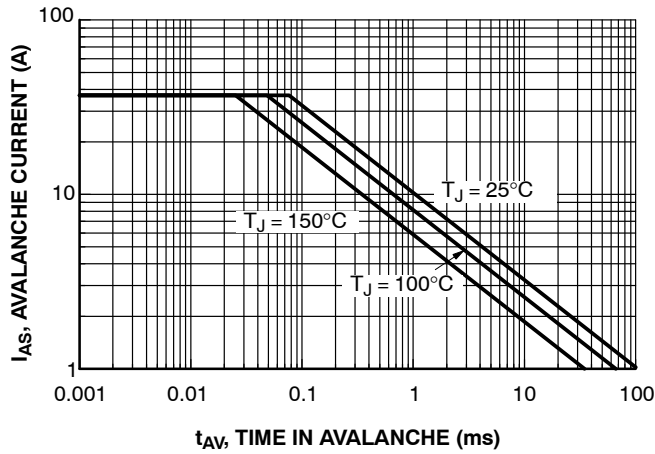


Figure 9. Unclamped Inductive Switching Capability

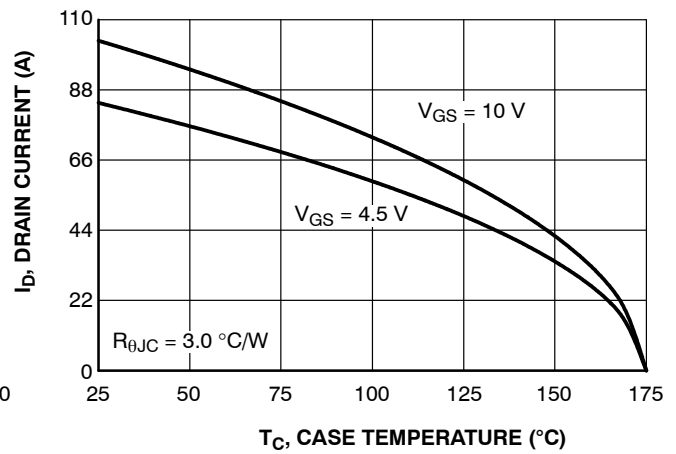


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

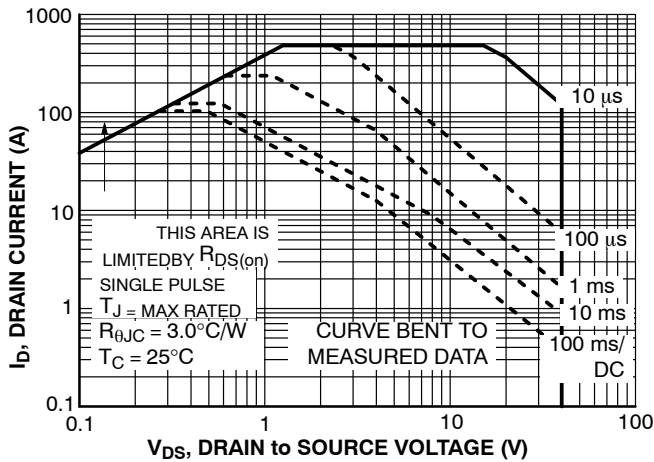


Figure 11. Forward Bias Safe Operating Area

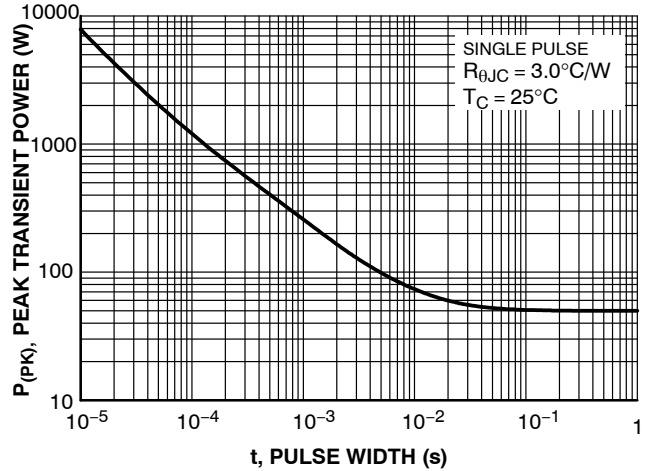


Figure 12. Single Pulse Maximum Power Dissipation

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TYPICAL CHARACTERISTICS (CONTINUED) $T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED

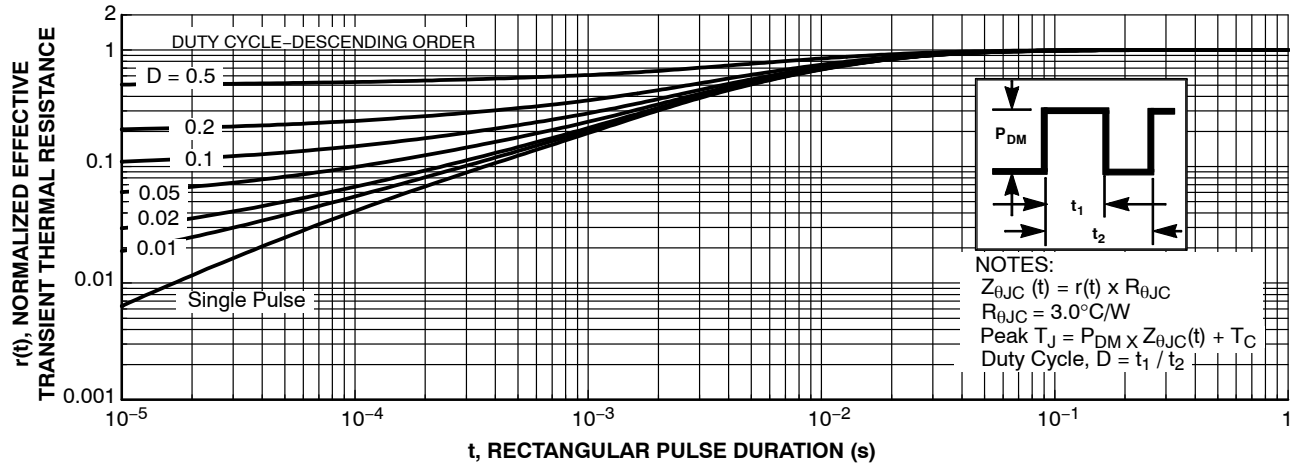
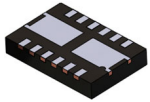
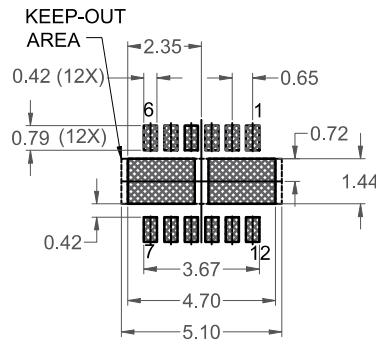
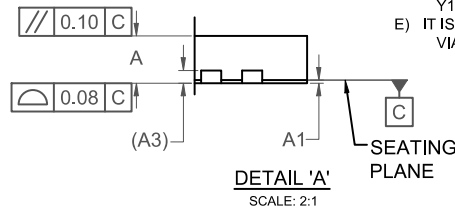
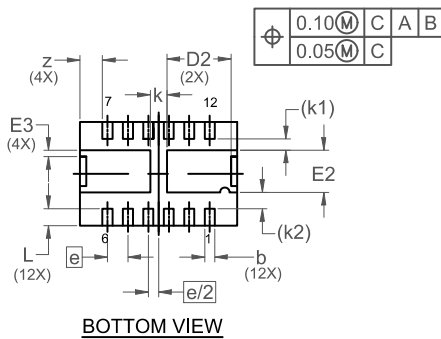
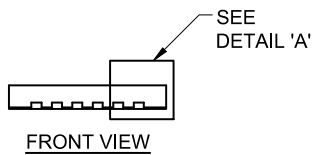
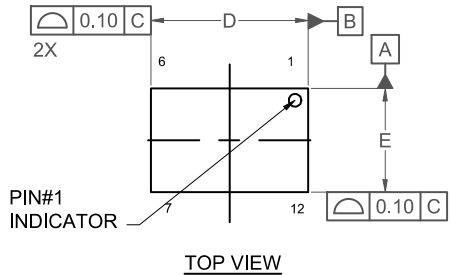


Figure 13. Junction-to-Case Transient Thermal Response Curve



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DATE 26 AUG 2021



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

- NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC MO-240, VARIATION BA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	4.90	5.00	5.10
D2	1.92	2.04	2.14
E	3.20	3.30	3.40
E2	1.24	1.34	1.44
E3	0.10	0.20	0.30
e	0.65 BSC		
e/2	0.325 BSC		
k	0.53 REF		
k1	0.36 REF		
k2	0.52 REF		
L	0.44	0.54	0.64
z	0.72 REF		

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