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## **MOSFET** – N-Channel, POWERTRENCH<sup>®</sup>

## 100 V, 40 A, 8.5 m $\Omega$

## FDPF085N10A

#### Description

This N–Channel MOSFET is Produced using **onsemi**'s advanced PowerTrench Process that has been tailored to minimize the on–state resistance while maintaining superior switching performance.

#### Features

- $R_{DS(on)} = 6.5 \text{ m}\Omega \text{ (Typ.)} @ V_{GS} = 10 \text{ V}, I_D = 40 \text{ A}$
- Fast Switching Speed
- Low Gate Charge, Qg = 31 nC (Typ.)
- High Performance Trench Technology for Extremely Low R<sub>DS(on)</sub>
- High Power and Current Handling Capability
- This Device is Pb-Free Halide, Free and RoHS Compliant

#### Applications

- Consumer Appliances
- LED TV
- Synchronous Rectification for ATX / Sever / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

#### **ABSOLUTE MAXIMUM RATINGS**

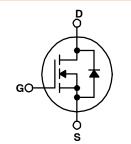
(T<sub>C</sub> =  $25^{\circ}$ C unless otherwise noted.)

Symbol	Parameter	Value	Unit
V <sub>DSS</sub>	Drain to Source Voltage	100	V
V <sub>GSS</sub>	Gate to Source Voltage	±20	V
Ι <sub>D</sub>	Drain Current – Continuous (T <sub>C</sub> = 25°C) – Continuous (T <sub>C</sub> = 100°C)	40 28	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	160	А
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	269	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	6.0	V/ns
P <sub>D</sub>	Power Dissipation - (T <sub>C</sub> = 25°C) - Derate Above 25°C	33.3 0.22	W W/°C
T <sub>J</sub> ,T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
ΤL	T <sub>L</sub> Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



TO-220F CASE 221AT



#### MARKING DIAGRAM



= Specific Device Code
= Assembly Location
= Date Code (Year and Week)
= Assembly Lot Code

#### ORDERING INFORMATION

Device	Package	Shipping
FDPF085N10A	TO-220-3 FullPack	1000 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, <u>BRD8011/D</u>.

#### **THERMAL CHARACTERISTICS**

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	4.5	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient, Max.	62.5	

#### **ELECTRICAL CHARACTERISTICS** (T<sub>C</sub> = $25^{\circ}$ C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Charac	teristics	•	-			
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0 \ V$	100	-	_	V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, Referenced to $25^{\circ}$ C	_	0.07	-	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1	μΑ
		$V_{DS} = 80 \text{ V}, \text{ T}_{C} = 150^{\circ}\text{C}$	-	-	500	
I <sub>GSS</sub>	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	±100	nA
On Charac	teristics		-	-	-	
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \ \mu A$	2.0	-	4.0	V
R <sub>DS(on)</sub>	Static Drain to Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 96 A	-	6.5	8.5	mΩ
9fs	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 96 A	-	76	_	S
Dynamic C	Characteristics					
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	2025	2695	pF
C <sub>oss</sub>	Output Capacitance		-	468	620	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1	-	20	_	pF
C <sub>oss</sub> (er)	Engry Related Output Capacitance	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	752	_	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10 V	$V_{GS}$ = 10 V, $V_{DS}$ = 50 V, $I_{D}$ = 96 A	-	31	40	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	(Note 4)	-	9.7	-	nC
Q <sub>gs2</sub>	Gate Charge Threshold to Plateau	1	-	5.0	_	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge	1	-	7.5	_	nC
ESR	Equivalent Series Resistance (G-S)	f = 1 MHz	-	0.97	_	Ω
Switching	Characteristics			-	-	
t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 96 A,	-	18	46	ns
t <sub>r</sub>	Turn-On Rise Time	V <sub>GS</sub> = 10 V, R <sub>G</sub> = 4.7 Ω (Note 4)	-	22	54	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	7	-	29	68	ns
t <sub>f</sub>	Turn-Off Fall Time		-	8	26	ns
Drain-Sou	rce Diode Characteristics and Maximum	Ratings				
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	40	Α
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	160	Α
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 V, I_{SD} = 96 A$	-	-	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{DD} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ I}_{SD} = 96 \text{ A},$	-	59	_	ns
Q <sub>rr</sub>	Reverse Recovery Charge	dl <sub>F</sub> /dt = 100 A/μs	-	80	_	nC

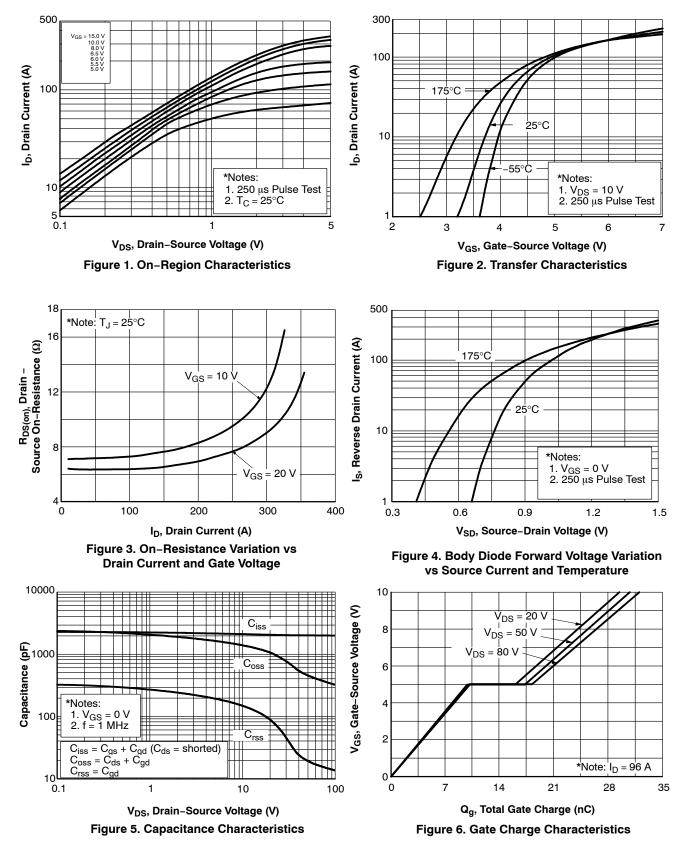
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

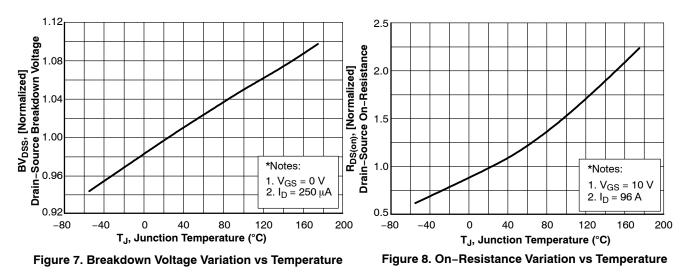
1. Repetitive Rating: Pulse-width limited by maximum junction temperature.

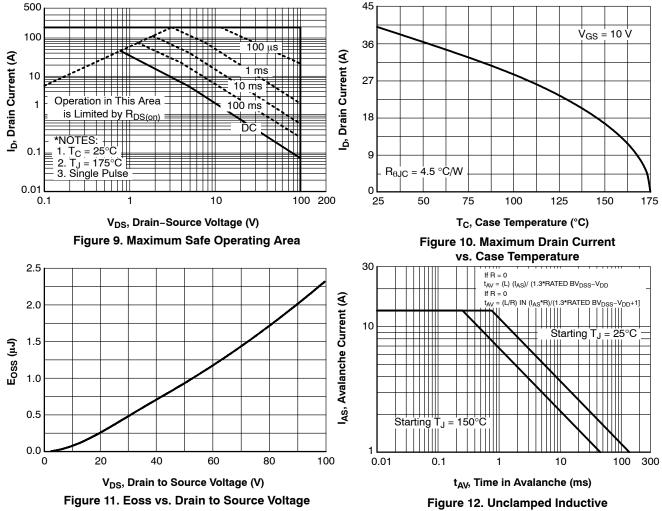
2. L = 3 mH, I<sub>AS</sub> = 13.4 A, R<sub>G</sub> = 25  $\Omega$  starting T<sub>J</sub> = 25°C. 3. I<sub>SD</sub> ≤ 40 A, di/dt ≤ 200 A/µs, V<sub>DD</sub> ≤ BV<sub>DSS</sub>, starting T<sub>J</sub> = 25°C. 4. Essentially independent of operating temperature.

#### **TYPICAL CHARACTERISTICS**



#### TYPICAL CHARACTERISTICS (CONTINUED)





### TYPICAL CHARACTERISTICS (CONTINUED)

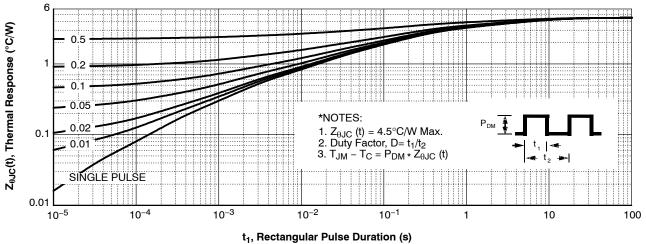
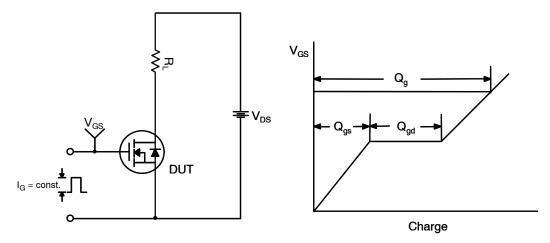


Figure 13. Transient Thermal Response Curve



### Figure 14. Gate Charge Test Circuit & Waveform

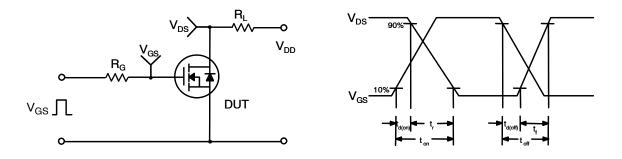


Figure 15. Resistive Switching Test Circuit & Waveforms

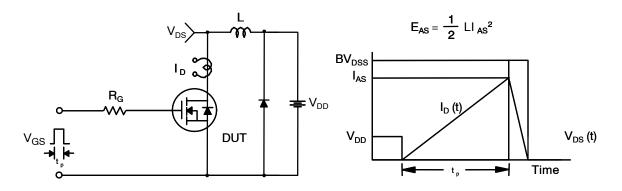


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

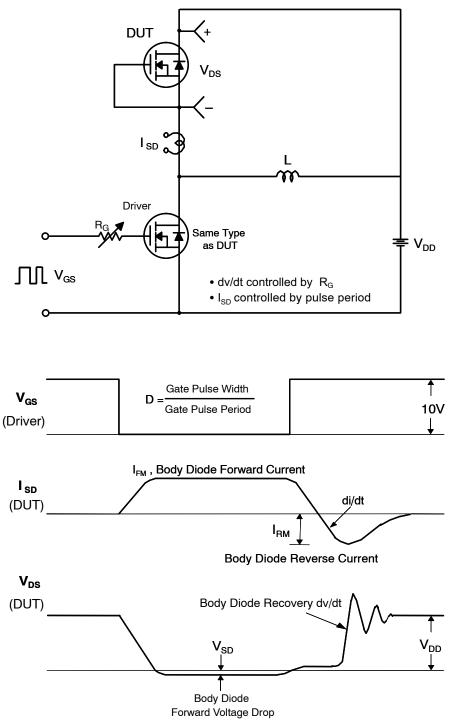
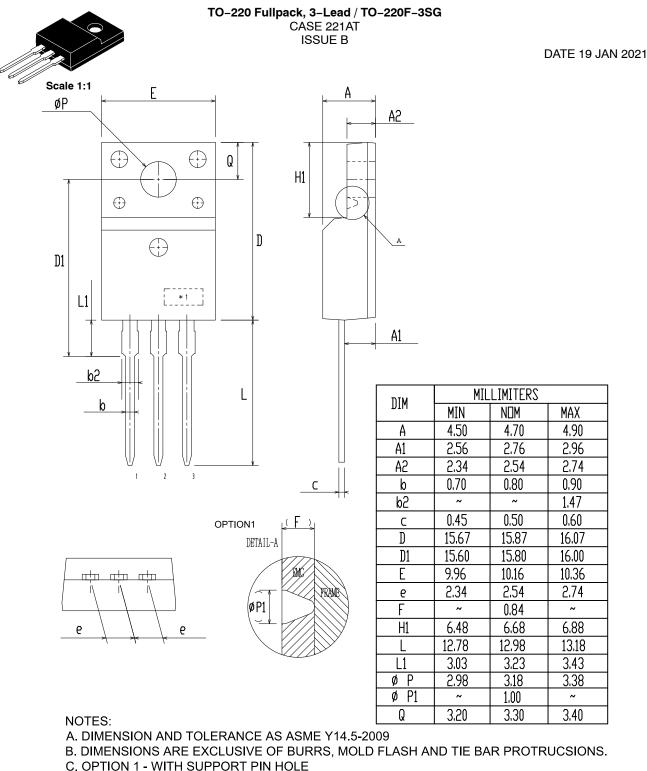


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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OPTION 2 - NO SUPPORT PIN HOLE

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