

MOSFET – Dual, N-Channel, Shielded Gate, POWER trench®

100 V, 2.7 A, 105 mΩ

FDS89161

General Description

This N-Channel MOSFET is produced using onsemi's advanced POWER trench process that incorporates Shielded Gate technology. This process has been optimized for $R_{DS(on)}$ switching performance and ruggedness.

Features

- Max $R_{DS(on)}$ = 105 mΩ at V_{GS} = 10 V, I_D = 2.7 A
- Max $R_{DS(on)}$ = 171 mΩ at V_{GS} = 6 V, I_D = 2.1 A
- High Performance Trench Technology for extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

- Synchronous Rectifier
- Primary Switch for Bridge Topology

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

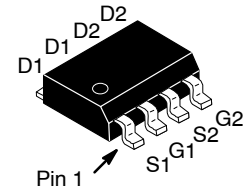
Symbol	Parameter		Value	Unit
V _{DS}	Drain to Source Voltage		100	V
V _{GS}	Gate to Source Voltage		±20	V
I _D	Drain Current	Continuous	2.7	A
		Pulsed	15	
E _{AS}	Single Pulse Avalanche Energy (Note 3)		13	mJ
P _D	Power Dissipation	T _C = 25°C	31	W
		T _A = 25°C (Note 1a)	1.6	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

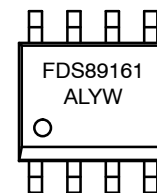
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	40	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	

V_{DS}	$R_{DS(on)}$ Max	I_D MAX
100 V	105 mΩ @ 10 V	2.7 A



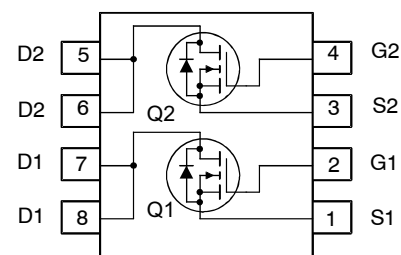
SOIC8
CASE 751EB

MARKING DIAGRAM



FDS89161 = Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping†
FDS89161	SOIC8	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	67	–	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
I_{GSS}	Gate to Body Leakage, Forward	$V_{GS} = \pm 20\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	–9	–	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 2.7\ \text{A}$	–	86	105	m Ω
		$V_{GS} = 6\ \text{V}$, $I_D = 2.1\ \text{A}$	–	120	171	
		$V_{GS} = 10\ \text{V}$, $I_D = 2.7\ \text{A}$, $T_J = 125^\circ\text{C}$	–	144	176	
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}$, $I_D = 2.7\ \text{A}$	–	5	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	158	210	pF
C_{oss}	Output Capacitance		–	43	58	pF
C_{rss}	Reverse Transfer Capacitance		–	3	5	pF
R_g	Gate Resistance		–	1	–	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}$, $I_D = 2.7\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	4.2	10	ns
t_r	Rise Time		–	1.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	7.3	15	ns
t_f	Fall Time		–	1.9	10	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{V}$ to $10\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 2.7\ \text{A}$	–	3	4.1	nC
		$V_{GS} = 0\ \text{V}$ to $5\ \text{V}$, $V_{DD} = 50\ \text{V}$, $I_D = 2.7\ \text{A}$	–	1.7	2.4	
Q_{gs}	Gate to Source Charge	$V_{DD} = 50\ \text{V}$, $I_D = 2.7\ \text{A}$	–	0.8	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	0.8	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 2.7\ \text{A}$ (Note 2)	–	0.85	1.3	V
		$V_{GS} = 0\ \text{V}$, $I_S = 2\ \text{A}$ (Note 2)	–	0.82	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 2.7\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	–	34	54	ns
Q_{rr}	Reverse Recovery Charge		–	21	34	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $78^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz. copper.



b) $135^\circ\text{C}/\text{W}$ when mounted on a minimum pad.

- Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%.
- Starting $T_J = 25^\circ\text{C}$, $L = 3\ \text{mH}$, $I_{AS} = 3\ \text{A}$, $V_{DD} = 100\ \text{V}$, $V_{GS} = 10\ \text{V}$.

TYPICAL CHARACTERISTICS (N-CHANNEL)

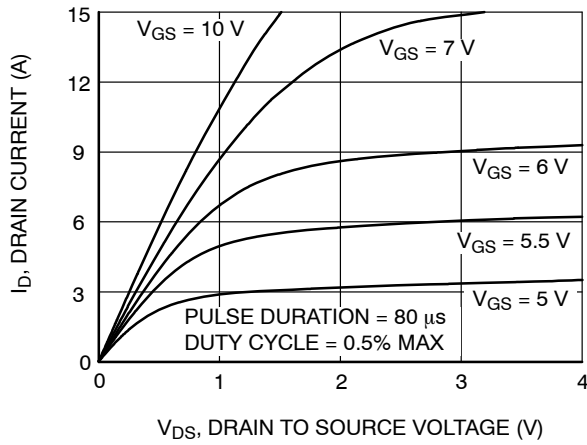
(T_J = 25°C unless otherwise noted)

Figure 1. On-Region Characteristics

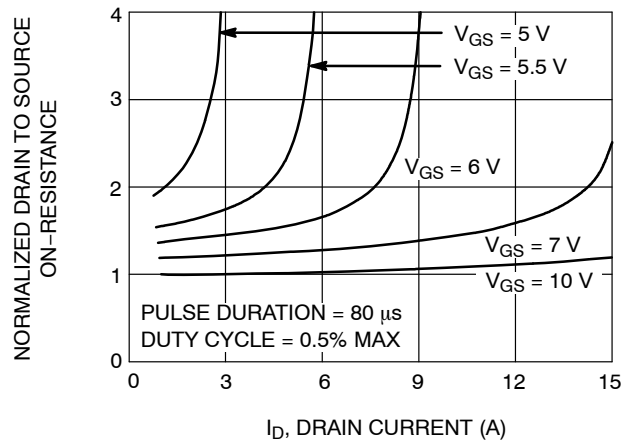


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

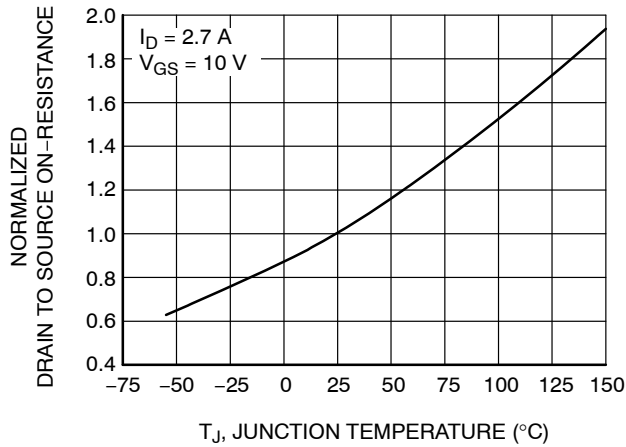


Figure 3. Normalized On-Resistance vs. Junction Temperature

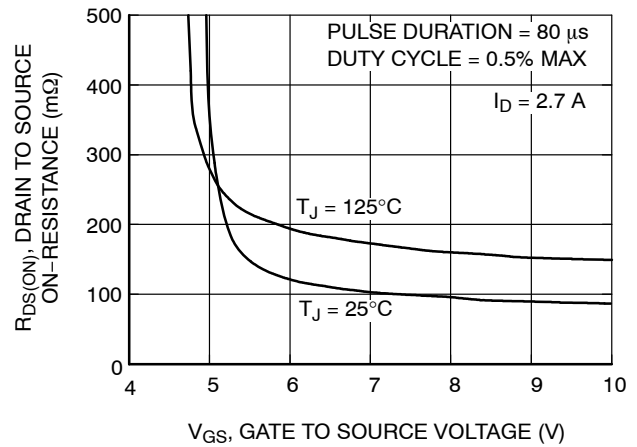


Figure 4. On-Resistance vs. Gate to Source Voltage

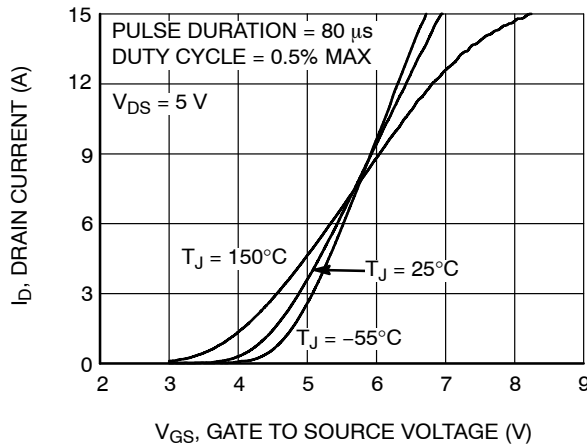


Figure 5. Transfer Characteristics

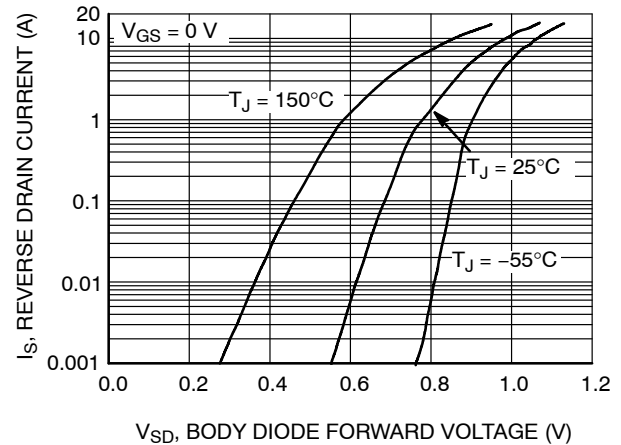


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (N-CHANNEL) (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

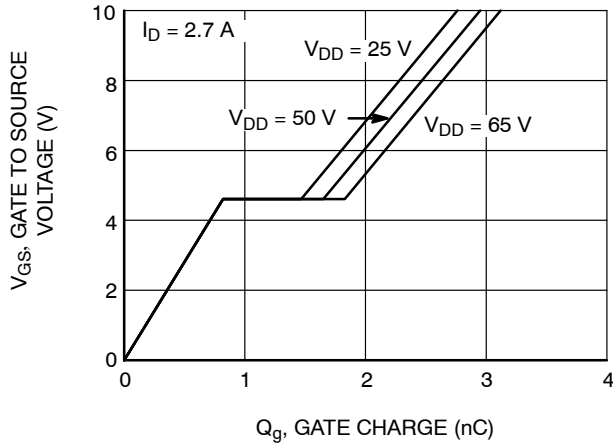


Figure 7. Gate Charge Characteristics

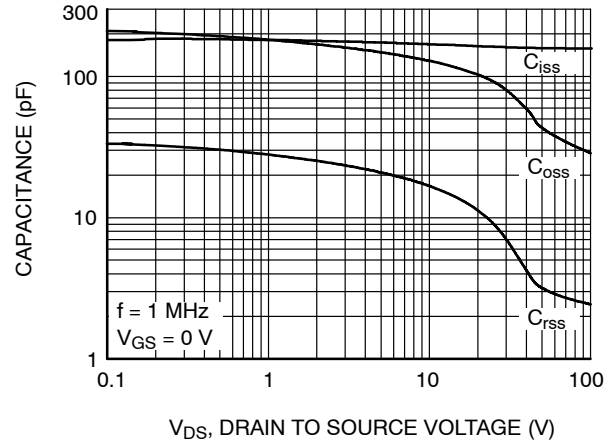


Figure 8. Capacitance vs. Drain to Source Voltage

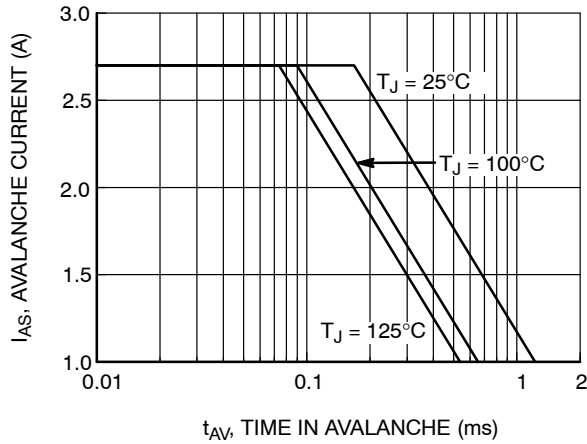


Figure 9. Unclamped Inductive Switching Capability

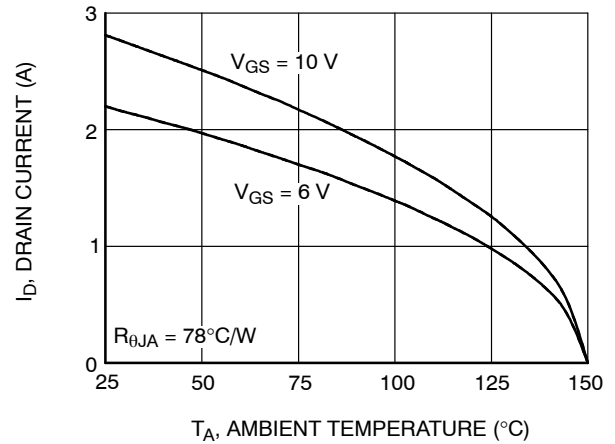


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

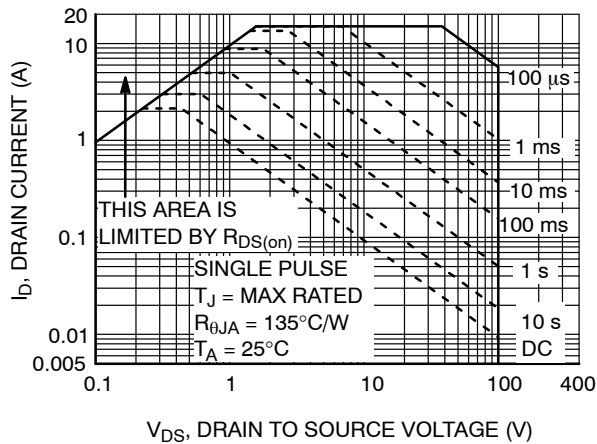


Figure 11. Forward Bias Safe Operating Area

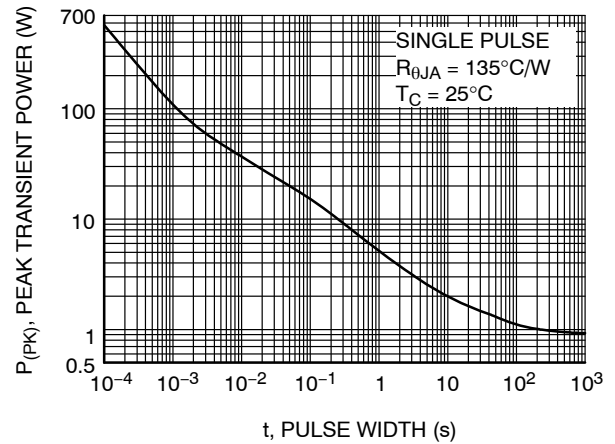


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (N-CHANNEL) (continued)

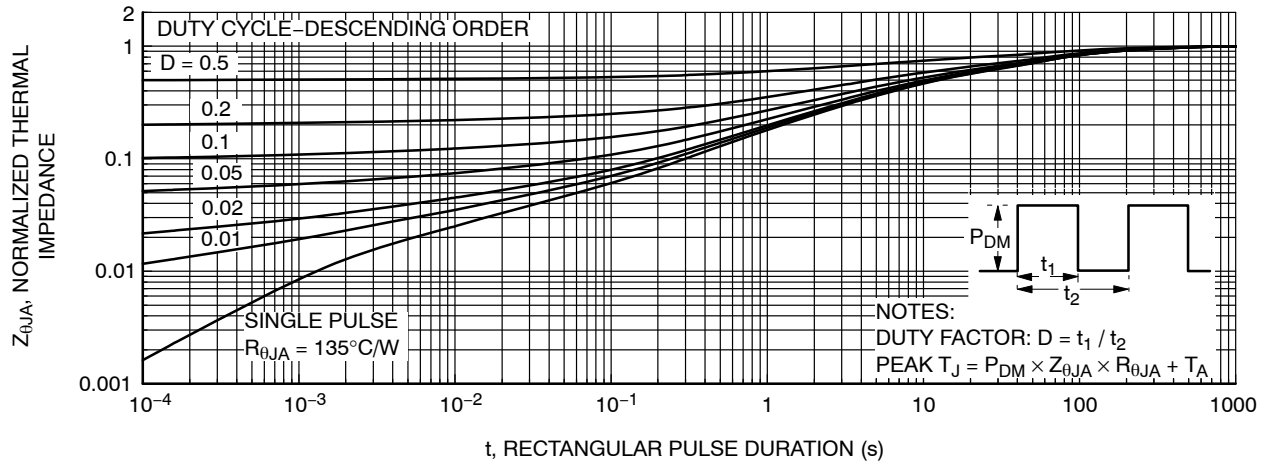
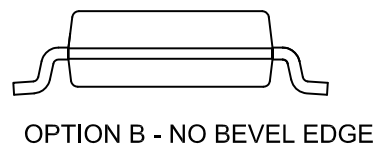
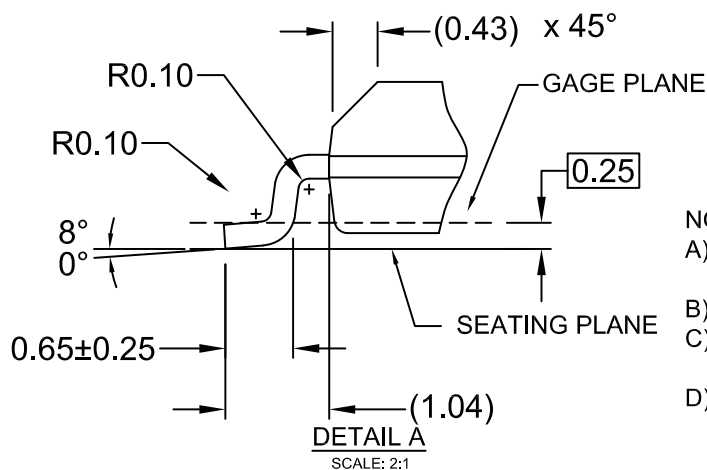
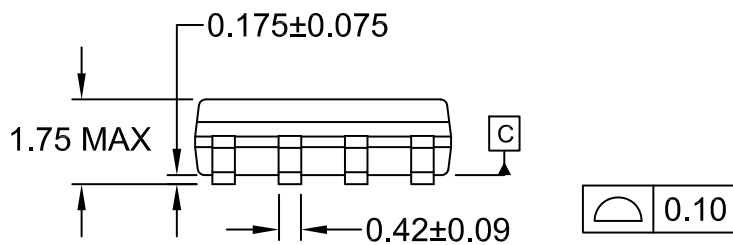
(T_J = 25°C unless otherwise noted)

Figure 13. Junction-to-Ambient Transient Thermal Response Curve

SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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