



Industrial eMMC 5.1 Specification

(XTRA III Series, Pseudo SLC, 153ball)

Version 1.7

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1. GENERAL DESCRIPTION



1.1. Introduction

FLEXXON's XTRA III eMMC is fully comply with JEDEC eMMC5.1 Standard. It is combined of an embedded flash controller and standard MLC NAND flash memory in one JEDEC standard package, 153Balls (11.5mm x 13mm).

FLEXXON eMMC provides high performance, good reliability and advanced power management. It is suitable for small, low power electronic devices.

1.2. Product Overview

FLEXXON XTRA III eMMC 5.1 includes the following features:

- Compliant with eMMC Specification Ver. 4.3, 4.4, 4.41, 4.5, 4.51, 5.0, 5.1
- Package of eMMC
 - 11.5 mm x 13 mm x 1.0 mm
- Temperature Range
 - Operation (Gold Grade): -25°C ~ 85°C
 - Operation (Diamond Grade): -40°C ~ 85°C
 - Storage: -40°C ~ 85°C
- Operating Voltage
 - VCC: 3.3V
 - VCCQ: 1.8V/3.3V
- Bus Mode
 - High-speed eMMC protocol
 - Clock frequency: 0 ~ 200MHz
- Supports three data bus widths: 1 bit (default), 4 bits, 8 bits
- Supports High Speed Mode HS400
- Supports Production State Awareness
- Supports Field Firmware Update
- RoHS compliant

1.3. Pseudo SLC (pSLC)

The default area of eMMC consist of a User Area to store data, two possible boot area partitions for booting and the Replay Protected Memory Block Area Partition to manage data in an authenticated and replay protected manner.

Each of the General Purpose Area Partitions can be configured as Pseudo SLC (enhanced or extended technological features) which offers better reliability, endurance and performance compared to MLC. For details, refer to JEDEC Standard Specification.

MLC Flash	
1 st bit (Fast)	2 nd bit (Slow)
1	1
1	0
0	1
0	0



Pseudo SLC	
1 st bit (Fast)	2 nd bit (Slow)
1	1
1	0
0	1
0	0

2. PRODUCT SPECIFICATIONS



2.1. Typical Sequential Performance

Table 2-1 eMMC Sequential Burst Performance (PSA Pseudo-SLC Burst Status)

Speed Mode & Operation			Capacity	
			4GB	8GB
HS400	Write Cache On	Read (MB/s)	225	225
		Write (MB/s)	105	140
	Write Cache Off	Read (MB/s)	225	225
		Write (MB/s)	100	125
HS200	Write Cache On	Read (MB/s)	160	160
		Write (MB/s)	105	125
	Write Cache Off	Read (MB/s)	160	160
		Write (MB/s)	95	115
DDR52	Write Cache On	Read (MB/s)	80	80
		Write (MB/s)	65	70
	Write Cache Off	Read (MB/s)	80	80
		Write (MB/s)	65	65
SDR52	Write Cache On	Read (MB/s)	45	45
		Write (MB/s)	40	40
	Write Cache Off	Read (MB/s)	45	45
		Write (MB/s)	35	40

Notes:

1. 8-bit bus width; HS400 mode; Vcc = 3.3V, VccQ = 1.8V
2. Performance is measured at VCC=3.3V, VCCQ=1.8V in HS400 & HS200 mode and at VCC=3.3V, VCCQ=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. Write Cache size is 512Kb.

Table 2-2 eMMC Sequential Sustained Performance (Normal Status)

Speed Mode & Operation			Capacity	
			4GB	8GB
HS400	Write Cache On	Read (MB/s)	225	225
		Write (MB/s)	105	135
	Write Cache Off	Read (MB/s)	225	225
		Write (MB/s)	95	125
HS200	Write Cache On	Read (MB/s)	160	160
		Write (MB/s)	105	125
	Write Cache Off	Read (MB/s)	160	160
		Write (MB/s)	95	115
DDR52	Write Cache On	Read (MB/s)	80	80
		Write (MB/s)	65	70
	Write Cache Off	Read (MB/s)	80	80
		Write (MB/s)	65	65
SDR52	Write Cache On	Read (MB/s)	45	45
		Write (MB/s)	40	40
	Write Cache Off	Read (MB/s)	45	45
		Write (MB/s)	35	40

Notes:

1. 8-bit bus width; HS400 mode; Vcc = 3.3V, Vccq = 1.8V
2. Performance is measured at VCC=3.3V, VCCQ=1.8V in HS400 & HS200 mode and at VCC=3.3V, VCCQ=3.3V in DDR52MHz & SDR52MHz mode.
3. Performance numbers might be subject to changes without notice.
4. Write Cache size is 512Kb.

2.2. Power Consumption

Table 2-3 eMMC Power Consumption RMS

Speed Mode & Operation			Capacity	
			4GB	8GB
HS400	Read (mA)	ICC	45	45
		ICCQ	170	170
	Write (mA)	ICC	45	75
		ICCQ	80	85
HS200	Read (mA)	ICC	40	40
		ICCQ	145	145
	Write (mA)	ICC	45	75
		ICCQ	80	85
DDR52	Read (mA)	ICC	25	25
		ICCQ	130	130
	Write (mA)	ICC	45	70
		ICCQ	70	75
SDR52	Read (mA)	ICC	20	20
		ICCQ	100	100
	Write (mA)	ICC	40	60
		ICCQ	75	75

Notes:

1. The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.
2. The RMS current is measured at TA=25°C, VCC=3.3V, VCCQ=1.8V in HS400 & HS200 mode and at VCC=3.3V, VCCQ=3.3V in DDR52MHz & SDR52MHz mode, 8-bit bus width without clock frequency.
3. Current numbers might be subject to changes without notice.

Table 2-4 Device Power Consumption Standby

Speed Mode & Operation		Capacity	
		4GB	8GB
HS400	Sleep (uA)	85	90
	Standby I _{CCQ} (uA)	130	140
	Standby I _{CC} (uA)	40	50
HS200	Sleep (uA)	85	90
	Standby I _{CCQ} (uA)	130	140
	Standby I _{CC} (uA)	40	50
DDR52	Sleep (uA)	90	95
	Standby I _{CCQ} (uA)	140	150
	Standby I _{CC} (uA)	40	55
SDR52	Sleep (uA)	90	95
	Standby I _{CCQ} (uA)	140	150
	Standby I _{CC} (uA)	40	55

Notes:

- Standby current is measured at T_A=25°C, VCC=3.3V, VCCQ=1.8V in HS400 & HS200 mode and at VCC=3.3V, VCCQ=3.3V in DDR52MHz & SDR52MHz mode, 8-bit bus width without clock frequency.
- Current numbers might be subject to changes without notice.

2.3. Partition Capacity

Table 2-5 eMMC Partition Capacity

Capacity	Boot Partition 1	Boot Partition 2	RPMB
4GB	4096 KB	4096 KB	4096 KB
8GB	4096 KB	4096 KB	4096 KB

2.4. User Density

Table 2-6 User Density

Capacity	User Density (Bytes)
4GB	3,917,479,936
8GB	7,834,959,872

3. INTERFACE DESCRIPTION



3.1. FLEXXON eMMC I/F Ball Array

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	
14	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	14
13	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	13
12	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	12
11	NC	NC	NC									NC	NC	NC	11
10	NC	NC	NC		NC	NC	NC	VSS	VCC	NC		NC	NC	NC	10
9	NC	NC	NC		NC					VCC		NC	NC	NC	9
8	NC	NC	NC		NC					VSS		NC	NC	NC	8
7	NC	NC	NC		VSS					NC		NC	NC	NC	7
6	VSS	DAT7	VCCQ		VCC					NC		CLK	NC	VSSQ	6
5	DAT2	DAT6	NC		NC	VCC	VSS	DS	VSS	RST_n		CMD	VSSQ	VCCQ	5
4	DAT1	DAT5	VSSQ	NC								VCCQ	VCCQ	VSSQ	4
3	DAT0	DAT4	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	VCCQ	3
2	NC	DAT3	VDDi	NC	NC	NC	NC	NC	NC	NC	NC	NC	VSSQ	NC	2
1	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	

Figure 3-1 eMMC interface in 153Balls Array (Top View)

3.2. Pins and Signal Description

Table 3-1 Function Pin Assignment, 153 balls

eMMC Interface			
Ball No.	Ball Signal	Type	Description
A3	DAT0	I/O/PP	Data I/O: Bidirectional channel used for data transfer
A4	DAT1		
A5	DAT2		
B2	DAT3		
B3	DAT4		
B4	DAT5		
B5	DAT6		
B6	DAT7		
M5	CMD	I/O/PP	Command: A bidirectional channel used for device initialization and command transfers.
M6	CLK	Input	Clock: Each cycle directs a 1-bit transfer on the command and DAT lines
K5	RST_n	Input	Hardware Reset
E6	VCC	Supply	Supply Voltage for Core
F5	VCC		
J10	VCC		
K9	VCC		
C6	VCCQ	Supply	Supply Voltage for I/O
M4	VCCQ		
N4	VCCQ		
P3	VCCQ		
P5	VCCQ		
A6	VSS	Supply	Supply Voltage ground for Core
E7	VSS		
G5	VSS		
H10	VSS		
J5	VSS		
K8	VSS		
C4	VSSQ	Supply	Supply Voltage ground for I/O
N2	VSSQ		
N5	VSSQ		
P4	VSSQ		
P6	VSSQ		
H5	DS	O/PP	Data strobe
C2	VDDi		Connect capacitor from VDDi to GND for stabilize internal power.

Note:

NC: No connect in eMMC. Left it floating.

4. EMMC REGISTERS



4.1. OCR Register

The 32-bit Operation Conditions Register (OCR) stores the VDD voltage profile of the Device and the access mode indication. The OCR register should be implemented by all Device.

Table 4-1 OCR Register Table

OCR slice	Description	Value	Width
[31]	Card power up status bit (busy) ¹		
[30:29]	Access mode	00b (byte mode) 10b (sector mode)	2
[28:24]	Reserved	0 0000b	5
[23:15]	2.7 - 3.6V	1 1111 1111b	9
[14:8]	2.0 - 2.6V	000 0000b	7
[7]	1.7 - 1.95V	1b	1
[6:0]	Reserved	000 0000b	7
Note ¹ : This bit is set to Low if the Device has not finished the power up routine			

4.2. CID Register

The Card Identification (CID) register is 128 bits wide. It contains the Device identification information used during the Device identification phase. For details, refer to JEDEC Standard Specification No. JESD84-B51.

Table 4-2 CID Register Table

Name	Field	CID Slice	Value	Width
Manufacturer ID	MID	[127:120]	EBh	8
Reserved	-	[119:114]	0h	6
Device/BGA	CBX	[113:112]	1h	2
OEM/ Application ID	OID	[111:104]	0Dh	8
Product Name	PNM	[103:56]	eMMC	48
Product Revision	PRV	[55:48]	51h	8
Product Serial Number	PSN	[47:16]	Random by Production	32
Manufacturing Date	MDT	[15:8]	Month, Year	8
CRC7 Checksum	CRC	[7:1]	-	7
Not used, always "1"	-	[0:0]	1h	1

4.3. CSD Register

The Device-Specific Data (CSD) register provides information on how to access the contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, etc. For details, refer to JEDEC Standard Specification No. JESD84-B51.

Table 4-3 CSD Register Table

Name	Field	Width	Type	CSD Slice	Value
CSD structure	CSD_STRUCTURE	2	R	[127:126]	3h
System specification version	SPEC_VERS	4	R	[125:122]	4h
Reserved	-	2	R	[121:120]	0h
Data read access-time 1	TAAC	8	R	[119:112]	4Fh
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	1h
Max. bus clock frequency	TRAN_SPEED	8	R	[103:96]	32h
Device command classes	CCC	12	R	[95:84]	8F5h
Max. read data block length	READ_BL_LEN	4	R	[83:80]	9h
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	0h
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	0h
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	0h
DSR implemented	DSR_IMP	1	R	[76:76]	0h
Reserved	-	2	R	[75:74]	0h
Device size	C_SIZE	12	R	[73:62]	FFFh
Max. read current @ VDD min	VDD_R_CURR_MIN	3	R	[61:59]	7h
Max. read current @ VDD max	VDD_R_CURR_MAX	3	R	[58:56]	7h
Max. write current @ VDD min	VDD_W_CURR_MIN	3	R	[55:53]	7h
Max. write current @ VDD max	VDD_W_CURR_MAX	3	R	[52:50]	7h
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	7h
Erase group size	ERASE_GRP_SIZE	5	R	[46:42]	4GB- 0Fh 8GB-1Fh
Erase group size multiplier	ERASE_GRP_MULT	5	R	[41:37]	1Fh
Write protect group size	WP_GRP_SIZE	5	R	[36:32]	0Fh
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	1h
Manufacturer default ECC	DEFAULT_ECC	2	R	[30:29]	0h
Write speed factor	R2W_FACTOR	3	R	[28:26]	2h
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	9h
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	0h
Reserved	-	4	R	[20:17]	0h
Content protection application	CONTENT_PROT_APP	1	R	[16:16]	0h
File format group	FILE_FORMAT_GRP	1	R/W	[15:15]	0h
Copy flag (OTP)	COPY	1	R/W	[14:14]	0h
Permanent write protection	PERM_WRITE_PROTECT	1	R/W	[13:13]	0h
Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	[12:12]	0h
File format	FILE_FORMAT	2	R/W	[11:10]	0h
ECC code	ECC	2	R/W/E	[9:8]	0h

CRC	CRC	7	R/W/E	[7:1]	4GB-64h 8GB-2Eh
Not used, always '1'	-	1	-	[0:0]	1h

4.4. Extended CSD Register

The Extended CSD register defines the Device properties and selected modes. It is 512 bytes long. The most significant 320 bytes are the Properties segment, which defines the Device capabilities and cannot be modified by the host. The lower 192 bytes are the Modes segment, which defines the configuration the Device is working in. These modes can be changed by the host by means of the SWITCH command. For details, refer to JEDEC Standard Specification No. JESD84-B51

Name	Field	Size (Byte)	CSD-slice	Value
Properties Segment				
Reserved1	–	6	[511:506]	0h
Extended Security Commands Error	EXT_SECURITY_ERR	1	[505]	0h
Supported Command Sets	S_CMD_SET	1	[504]	1h
HPI features	HPI_FEATURES	1	[503]	1h
Background operations support	BKOPS_SUPPORT	1	[502]	1h
Max packed read commands	MAX_PACKED_READS	1	[501]	3Ch
Max packed write commands	MAX_PACKED_WRITES	1	[500]	3Ch
Data Tag Support	DATA_TAG_SUPPORT	1	[499]	1h
Tag Unit Size	TAG_UNIT_SIZE	1	[498]	3h
Tag Resources Size	TAG_RES_SIZE	1	[497]	0h
Context management capabilities	CONTEXT_CAPABILITIES	1	[496]	5h
Large Unit size	LARGE_UNIT_SIZE_M1	1	[495]	17h
Extended partitions attribute support	EXT_SUPPORT	1	[494]	3h
Supported modes	SUPPORTED_MODES	1	[493]	1h
FFU features	FFU_FEATURES	1	[492]	0h
Operation codes timeout	OPERATION_CODE_TIME_OUT	1	[491]	0h
FFU Argument	FFU_ARG	4	[490:487]	65535h
Barrier support	BARRIER_SUPPORT	1	[486:486]	1h
Reserved	Reserved	177	[485:309]	-
CMD Queuing Support	CMQ_SUPPORT	1	[308:308]	0h
CMD Queuing Depth	CMQ_DEPTH	1	[307:307]	0h
Reserved	Reserved	1	[306:306]	-

Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	[305:302]	0h
Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	[301:270]	-
Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	[269]	1h
Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	[268]	1h
Pre EOL information	PRE_EOL_INFO	1	[267]	1h
Optimal read size	OPTIMAL_READ_SIZE	1	[266]	1h
Optimal write size	OPTIMAL_WRITE_SIZE	1	[265]	1h
Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	[264]	8h
Device version	DEVICE_VERSION	2	[263:262]	1h
Firmware version	FIRMWARE_VERSION	8	[261:254]	0h*
Power class for 200MHz, DDR at VCC=3.6V	PWR_CL_DDR_200_360	1	[253]	0h
Cache size	CACHE_SIZE	4	[252:249]	512
Generic CMD6 timeout	GENERIC_CMD6_TIME	1	[248]	32h
Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	[247]	FFh
Background operations status	BKOPS_STATUS	1	[246]	0h
Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	[245:242]	0h
1 st initialization time after partitioning	INI_TIMEOUT_AP	1	[241]	64h
Cache Flushing Policy	CACHE_FLUSH_POLICY	1	[240]	1h
Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	[239]	0h
Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	[238]	0h
Power class for 200MHz at 3.6V	PWR_CL_200_360	1	[237]	0h
Power class for 200MHz, at 1.95V	PWR_CL_200_195	1	[236]	0h
Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	[235]	0h
Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	[234]	0h
Reserved1	-	1	[233]	-
TRIM Multiplier	TRIM_MULT	1	[232]	11h
Secure Feature support	SEC_FEATURE_SUPPORT	1	[231]	55h

Secure Erase Multiplier	SEC_ERASE_MULT	1	[230]	F7h
Secure TRIM Multiplier	SEC_TRIM_MULT	1	[229]	F7h
Boot information	BOOT_INFO	1	[228]	7h
Reserved1	–	1	[227]	–
Boot partition size	BOOT_SIZE_MULT	1	[226]	20h
Access size	ACC_SIZE	1	[225]	4GB – 7h 8GB – 8h
High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	[224]	1h
High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	[223]	11h
Reliable write sector count	REL_WR_SEC_C	1	[222]	1h
High-capacity write protect group size	HC_WP_GRP_SIZE	1	[221]	10h
Sleep current (VCC)	S_C_VCC	1	[220]	Ah
Sleep current (VCCQ)	S_C_VCCQ	1	[219]	Bh
Production state awareness Timeout	PRODUCTION_STATE_AW ARENESS_TIMEOUT	1	[218]	14h
Sleep/awake timeout	S_A_TIMEOUT	1	[217]	15h
Sleep Notification time out	SLEEP_NOTIFICATION_TI ME	1	[216]	Fh
Sector Count	SEC_COUNT	4	[215:212]	4GB – 7651328 8GB - 15302656
Reserved (note1)	–	1	[211]	1h
Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	[210]	8h
Minimum Read Performance for 8bit at 52MHz	MIN_PERF_R_8_52	1	[209]	8h
Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_5 2	1	[208]	8h
Minimum Read Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	[207]	8h
Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	[206]	8h
Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	[205]	8h
Reserved1	–	1	[204]	0h
Power class for 26MHz at 3.6V 1 R	PWR_CL_26_360	1	[203]	0h
Power class for 52MHz at 3.6V 1 R	PWR_CL_52_360	1	[202]	0h
Power class for 26MHz at 1.95V 1 R	PWR_CL_26_195	1	[201]	0h

Power class for 52MHz at 1.95V 1 R	PWR_CL_52_195	1	[200]	0h
Partition switching timing	PARTITION_SWITCH_TIME	1	[199]	3h
Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	[198]	FFh
I/O Driver Strength	DRIVER_STRENGTH	1	[197]	1Fh
Device type	CARD_TYPE	1	[196]	57h
Reserved (note1)	–	1	[195]	0h
CSD structure version			[194]	2h
Reserved (note1)	–	1	[193]	0h
Extended CSD revision	EXT_CSD_REV	1	[192]	8h
Modes Segment				
Command set	CMD_SET	1	[191]	0h
Reserved (note1)	–	1	[190]	–
Command set revision	CMD_SET_REV	1	[189]	0h
Reserved (note1)	–	1	[188]	–
Power class	POWER_CLASS	1	[187]	0h
Reserved (note1)	–	1	[186]	–
High-speed interface timing	HS_TIMING	1	[185]	1h (note 3)
Strobe Support	STROBE_SUPPORT	1	[184]	1h
Bus width mode	BUS_WIDTH	1	[183]	2h (note 4)
Reserved (note1)	–	1	[182]	–
Erased memory content	ERASED_MEM_CONT	1	[181]	0h
Reserved (note1)	–	1	[180]	–
Partition configuration	PARTITION_CONFIG	1	[179]	0h
Boot config protection	BOOT_CONFIG_PROT	1	[178]	0h
Boot bus Conditions	BOOT_BUS_CONDITIONS	1	[177]	0h
Reserved (note1)	–	1	[176]	–
High-density erase group definition	ERASE_GROUP_DEF	1	[175]	0h
Boot write protection status registers	BOOT_WP_STATUS	1	[174]	0h
Boot area write protection register	BOOT_WP	1	[173]	0h
Reserved (note1)	–	1	[172]	–
User area write protection register	USER_WP	1	[171]	0h
Reserved (note1)	–	1	[170]	0h
FW configuration	FW_CONFIG	1	[169]	0h
RPMB Size	RPMB_SIZE_MULT	1	[168]	20h
Write reliability setting register	WR_REL_SET	1	[167]	1Fh
Write reliability parameter register	WR_REL_PARAM	1	[166]	14h
Start Sanitize operation	SANITIZE_START	1	[165]	0h
Manually start background operations	BKOPS_START	1	[164]	0h

Enable background operations handshake	BKOPS_EN	1	[163]	0h
H/W reset function	RST_n_FUNCTION	1	[162]	0h
HPI management	HPI_MGMT	1	[161]	0h
Partitioning Support	PARTITIONING_SUPPORT	1	[160]	7h
Max Enhanced Area Size	MAX_ENH_SIZE_MULT	3	[159:157]	4GB – 467 8GB - 934
Partitions attribute	PARTITIONS_ATTRIBUTE	1	[156]	1h
Partitioning Setting	PARTITION_SETTING_	1	[155]	1h
General Purpose Partition Size	GP_SIZE_MULT 4	3	[154:152]	0h
General Purpose Partition Size	GP_SIZE_MULT3	3	[151:149]	0h
General Purpose Partition Size	GP_SIZE_MULT2	3	[148:146]	0h
General Purpose Partition Size	GP_SIZE_MULT1	3	[145:143]	0h
Enhanced User Data Area Size	ENH_SIZE_MULT	3	[142:140]	934h
Enhanced User Data Start Address	ENH_START_ADDR	4	[139:136]	0h
Reserved (note1)	–	1	[135]	–
Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	[134]	0h
Reserved (note1)	–	1	[133]	–
Package Case Temperature is	TCASE_SUPPORT	1	[132]	0h
Periodic Wake-up	PERIODIC_WAKEUP	1	[131]	0h
Program CID/CSD in DDR mode	PROGRAM_CID_CSD_DD	1	[130]	1h
Reserved (note1)	–	2	[129:128]	–
Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	[127:64]	–
Native sector size	NATIVE_SECTOR_SIZE	1	[63]	0h
Sector size emulation	USE_NATIVE_SECTOR	1	[62]	0h
Sector size	DATA_SECTOR_SIZE	1	[61]	0h
1 st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	[60]	0h
Class 6 commands control	CLASS_6_CTRL	1	[59]	0h
Number of addressed group to be	DYNCAP_NEEDED	1	[58]	0h
Exception events control	EXCEPTION_EVENTS_CTR	2	[57:56]	0h
Exception events status	EXCEPTION_EVENTS_STA	2	[55:54]	0h
Extended Partitions Attribute	EXT_PARTITIONS_ATTRIB	2	[53:52]	0h
Context configuration	CONTEXT_CONF	15	[51:37]	0h
Packed command status	PACKED_COMMAND_STATUS	1	[36]	0h
Packed command failure index	PACKED_FAILURE_INDEX	1	[35]	0h
Power Off Notification	POWER_OFF_NOTIFICATION	1	[34]	0h

Control to turn the Cache ON/OFF	CACHE_CTRL	1	[33]	0h
Flushing of the cache	FLUSH_CACHE	1	[32]	0h
Reserved (note1)	Reserved	1	[31]	0h
Mode config	MODE_CONFIG	1	[30:30]	0h
Mode operation codes	MODE_OPERATION_COD	1	[29:29]	0h
Reserved (note1)	Reserved	2	[28:27]	–
FFU status	FFU_STATUS	1	[26:26]	0h
Per loading data size	PRE_LOADING_DATA_SIZE	4	[25:22]	0h
Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	[21:18]	4GB – 7651328 8GB - 15302656
Product state awareness enablement	PRODUCT_STATE_AWAR	1	[17:17]	1h
Secure removal type	SECURE_REMOVAL_TYPE	1	[16:16]	1h
Command Queue Mode enable	CMQ_MODE_EN	1	[15:15]	0h
Reserved	Reserved	15	[14:0]	-

Note1 : Reserved bits should read as “0.”

Note2 : Obsolete values should be don't care.

Note3 : This field is 0 after power-on, H/W reset or software reset, thus selecting the backwards compatibility interface timing for the Device. If the host sets 1 to this field, the Device changes its timing to high speed interface timing (see Section 10.6.1 of JESD84-B51). If the host sets value 2 the Device changes its timing to HS200 interface timing (see Section 10.8.1 of JESD84-B51), If the host sets HS_TIMING[3:0] to 0x3, the device changes its timing to HS400 interface timing (see 10.10).

Note4 : It is set to '0' (1 bit data bus) after power up and can be changed by a SWITCH command.

Note5: * Changed by Firmware release note

4.5. RCA Register

The writable 16-bit Relative Device Address (RCA) register carries the Device address assigned by the host during the Device identification. This address is used for the addressed host-Device communication after the Device identification procedure. The default value of the RCA register is 0x0001. The value 0x0000 is reserved to set all Devices into the *Stand-by State* with CMD7.

4.6. DSR Register

The 16-bit driver stage register (DSR) is described in detail in JEDEC Standard Specification, JESD84-B51 Section 7.6. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of Devices). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

5. ELECTRICAL CHARACTERISTICS



5.1. Power Supply

Table 5-1 eMMC power supply

Parameter	Symbol	Min	Max	Unit
Supply voltage (NAND)	Vcc	2.7	3.6	V
Supply voltage (I/O)	Vccq	2.7	3.6	V
		1.7	1.95	V
Supply Power-Up for 1.8V	tPRUL		25	ms
Supply Power-Up for 3.3V	tPRUH		35	Ms

5.2. Bus Signal Levels

Figure 5-1 Bus Signal Levels

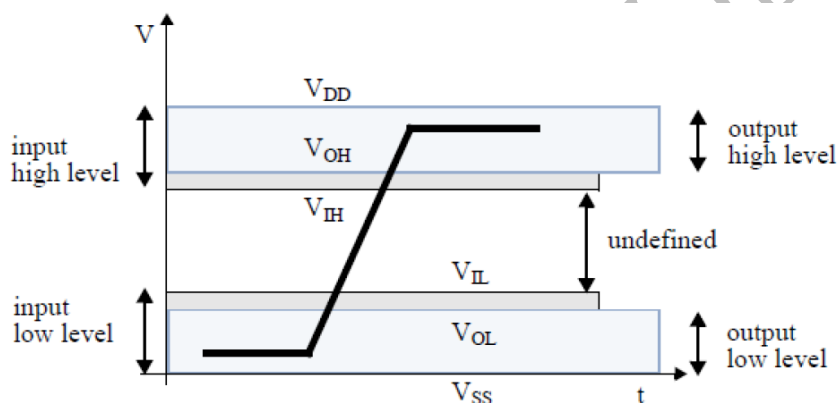
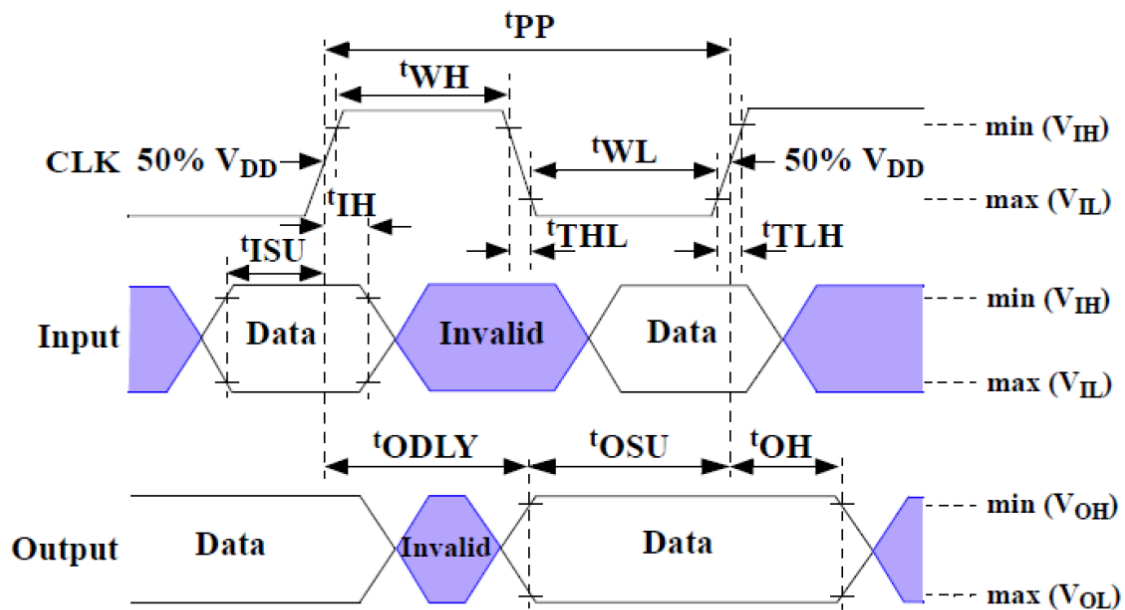


Table 5-2 Bus Signals Levels

Parameter	Symbol	Min	Max	Unit	Remark
Open-Drain Bus Signal Level					
Output High Voltage	VOH	VDD - 0.2	-	V	IOH = -100 uA
Output Low Voltage	VOL	-	0.3	V	IOL = 2 mA
Push-pull bus signal level (2.7V~3.6V)					
Output High Voltage	VOH	0.75 * VCCQ	-	V	IOH = -100 uA @ Vccq min
Output Low Voltage	VOL	-	0.125 * VCCQ	V	IOL = 100 uA @ Vccq min
Input High Voltage	VIH	0.625 * VCCQ	VCCQ + 0.3	V	
Input Low Voltage	VIL	VSS - 0.3	0.25 * VCCQ	V	
Push-pull bus signal level (1.7V~1.95V)					
Output High Voltage	VOH	VCCQ - 0.45V	-	V	IOH = -2 mA
Output Low Voltage	VOL	-	0.45V	V	IOL = 2 mA
Input High Voltage	VIH	0.65 * VCCQ	VCCQ + 0.3	V	
Input Low Voltage	VIL	VSS - 0.3	0.35 * VDD	V	

5.3. Bus Timing

Figure 5-2 Bus Timing in Single Data Rate Mode



Data must always be sampled on the rising edge of the clock.

Table 5-3 Backward Compatible Device Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark ¹
Clock CLK²					
Clock Frequency Data Transfer Mode (PP) ³	fPP	0	26	MHz	CL ≤ 30 pF
Clock Frequency Identification Mode (OD)	fOD	0	400	kHz	
Clock high time	tWH	10	-	ns	CL ≤ 30 pF
Clock low time	tWL	10	-	ns	CL ≤ 30 pF
Clock rise time ⁴	tTLH	-	10	ns	CL ≤ 30 pF
Clock fall time	tTHL	-	10	ns	CL ≤ 30 pF
Inputs/Outputs CMD, DAT (Referenced to CLK)					
Input set-up time	tISU	3	-	ns	CL ≤ 30 pF
Input hold time	tIH	3	-	ns	CL ≤ 30 pF
Output set-up time ⁵	tOSU	11.7	-	ns	CL ≤ 30 pF
Output hold time ⁵	tOH	8.3	-	ns	CL ≤ 30 pF

Note ¹: The Device must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

Note ²: CLK timing is measured at 50% of VDD.

Note ³: For compatibility with Devices that support the v4.2 standard or earlier, host should not use > 26 MHz before switching to high-speed interface timing.

Note ⁴: CLK rise and fall times are measured by min (VIH) and max (VIL).

Note ⁵: tOSU and tOH are defined as values from clock rising edge. However, there may be Devices or devices which utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to settWL value as long as possible within the range which will not go over tCK-tOH(min) in the system or to use slow clock frequency, so that host could have data set up margin for those devices. In this case, each device which utilizes clock falling edge might show the correlation either between tWL and tOSU or between tCK and tOSU for the device in its own datasheet as a note or its' application notes.

Table 5-4 High Speed Device Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK¹					
Clock Frequency Data Transfer Mode (PP) ²	f _{PP}	0	52 ³	MHz	CL ≤30 pF Tolerance: +100 KHz
Clock Frequency Identification Mode (OD)	f _{OD}	0	400	kHz	Tolerance: +20 KHz
Clock high time	t _{WH}	6.5	-	ns	CL ≤30 pF
Clock low time	t _{WL}	6.5	-	ns	CL ≤30 pF
Clock rise time ⁴	t _{TLH}	-	3	ns	CL ≤30 pF
Clock fall time	t _{THL}	-	3	ns	CL ≤30 pF
Inputs /Outputs CMD, DAT (Referenced to CLK)					
Input set-up time	t _{ISU}	3	-	ns	CL ≤30 pF
Input hold time	t _{IH}	3	-	ns	CL ≤30 pF
Output delay time during data transfer	t _{ODLY}	-	13.7	ns	CL ≤30 pF
Output hold time	t _{OH}	2.5	-	ns	CL ≤30 pF
Signal rise time ⁵	t _{RISE}	-	3	ns	CL ≤30 pF
Signal fall time	t _{FALL}	-	3	ns	CL ≤30 pF

Note ¹: CLK timing is measured at 50% of VDD.
Note ²: eMMC shall support the full frequency range from 0-26MHz, or 0-52MHz
Note ³: Device can operate as high-speed Device interface timing at 26 MHz clock frequency.
Note ⁴: CLK rise and fall times are measured by min (VIH) and max (VIL).
Note ⁵: Inputs CMD, DAT rise and fall times are measured by min (VIH) and max (VIL), and output CMD, DAT rise and fall times are measured by min (VOH) and max (VOL).

Figure 5-3 Bus Timing in Dual Data Rate Mode

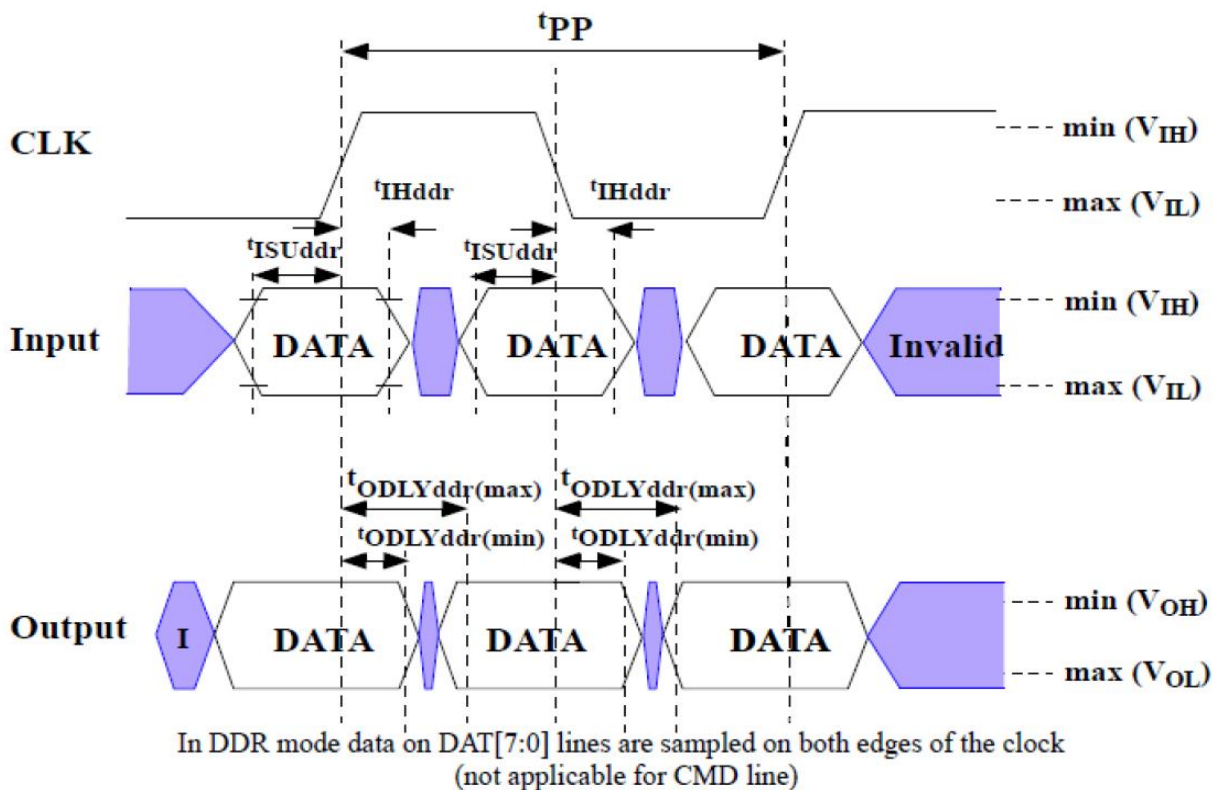
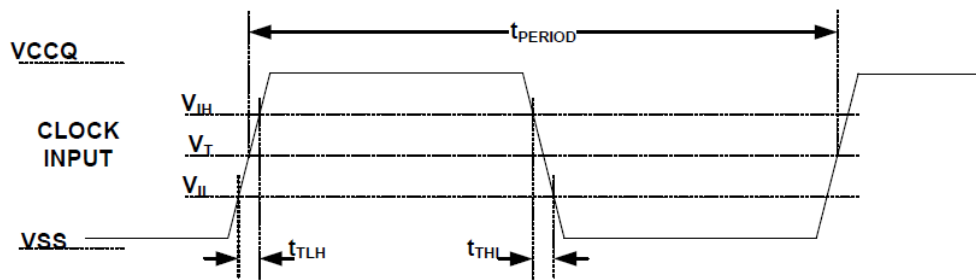


Table 5-5 Dual Data Rate Interface Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK¹					
Clock Duty Cycle	-	45	55	%	Include jitter, phase noise
Input/Output DAT (Referenced to CLK-DDR Mode)					
Input set-up time	t_{ISUddr}	2.5	-	ns	$CL \leq 20$ pF
Input hold time	t_{IHddr}	2.5	-	ns	$CL \leq 20$ pF
Output delay time	$t_{ODLYddr}$	1.5	7	ns	$CL \leq 20$ pF
Signal rise time (DAT0-7) ²	t_{RISE}	-	2	ns	$CL \leq 20$ pF
Signal fall time (DAT0-7)	t_{FALL}	-	2	ns	$CL \leq 20$ pF

Note ¹: CLK timing is measured at 50% of VDD.
Note ²: Inputs DAT rise and fall times are measured by min (VIH) and max (VIL), and outputs DAT rise and fall times are measured by min (VOH) and max (VOL).

Figure 5-4 HS200 Clock Signal Timing



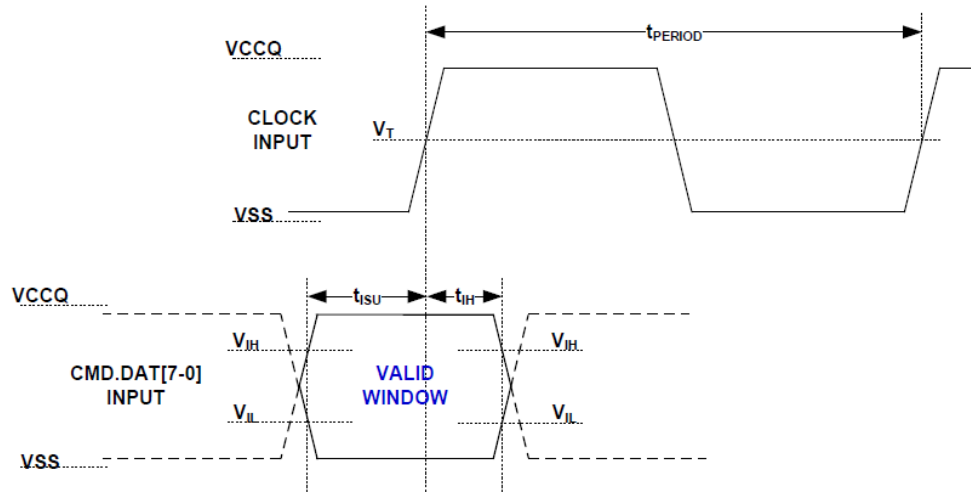
Notes:

1. V_{IH} denote $V_{IH}(\min.)$ and V_{IL} denotes $V_{IL}(\max.)$.
2. $V_T=0.975V$ – Clock Threshold, indicates clock reference point for timing measurements.

Table 5-6 HS200 Clock Signal Timing

Symbol	Min	Max	Unit	Remark
t_{PERIOD}	5	-	ns	200MHz (Max.), between rising edges
t_{TLH}, t_{THL}	-	$0.2 * t_{PERIOD}$	ns	$t_{TLH}, t_{THL} < 1ns$ (max.) at 200MHz, $C_{DEVICE}=6pF$, The absolute maximum value of t_{TLH}, t_{THL} is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

Figure 5-5 HS200 Device Input Timing



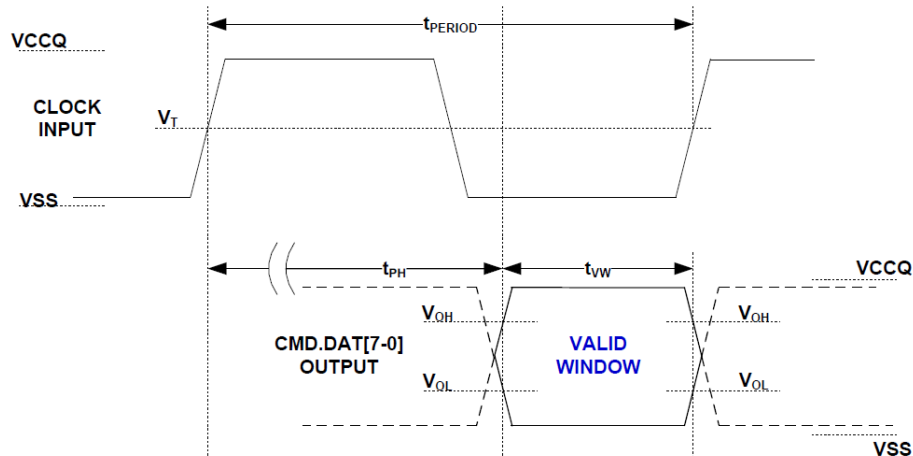
Note 1: t_{ISU} and t_{IH} are measured at V_{IL} (max) and V_{IH} (min).

Note 2: V_{IH} denote V_{IH} (min) and V_{IL} (max) denotes V_{IL} (max).

Table 5-7 HS200 Device Input Timing

Symbol	Min	Max	Unit	Remark
t_{ISU}	1.40	-	ns	$C_{DEVICE} \leq 6pF$
t_{IH}	0.8	-	ns	$C_{DEVICE} \leq 6pF$

Figure 5-6 HS200 Device Output Timing



NOTE V_{OH} denotes $V_{OH(min)}$ and V_{OL} denotes $V_{OL(max)}$.

Table 5-8 HS200 Device Output Timing

Symbol	Min	Max	Unit	Remark
t_{PH}	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
Δ_{TPH}	-350 ($\Delta T = -20^\circ C$)	+1550 ($\Delta T = 90^\circ C$)	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window (TVW) from last system Tuning procedure Δ_{TPH} is 2600ps for ΔT from $-25^\circ C$ to $125^\circ C$ during operation.
t_{vw}	0.575	-	UI	$t_{vw} = 2.88ns$ at 200MHz Using test circuit including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected TVW at Host input is larger than 0.475UI.

Note: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200MHz.

Figure 5-7 Δ_{TPH} consideration

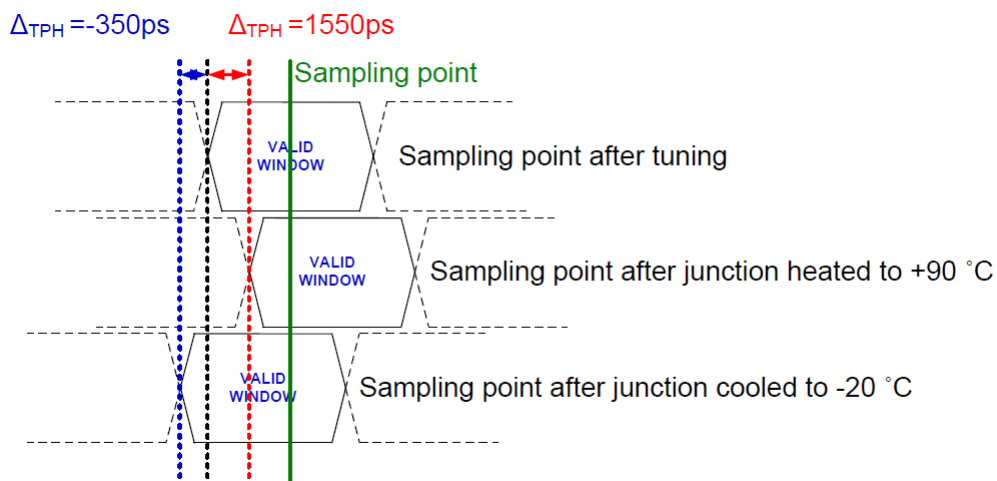


Figure 5-8 HS400 Device Input Timing

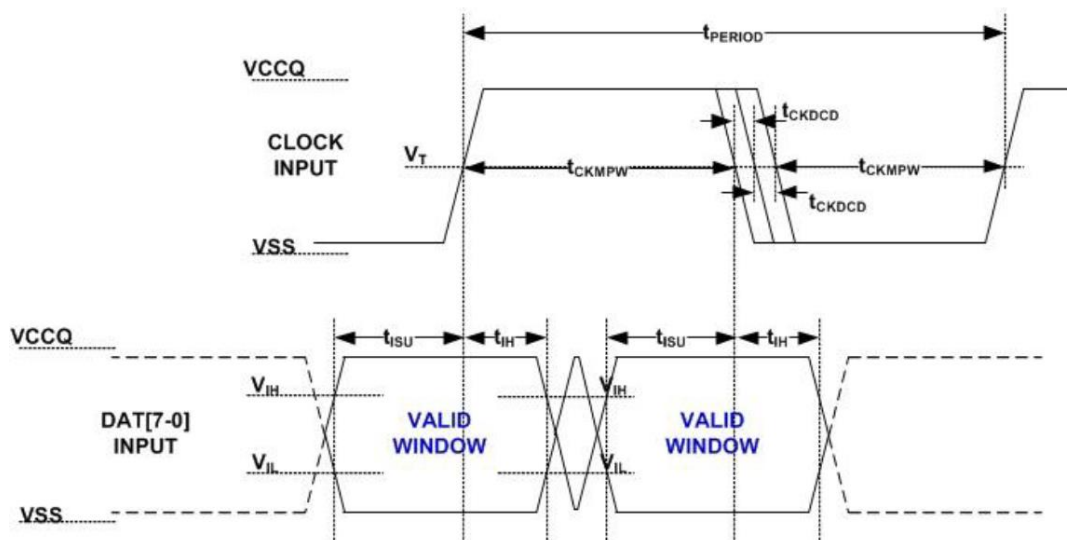


Table 5-9 HS400 Device Input Timing

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	t_{PERIOD}	5			200MHz (Max), between rising edges with respect to V_T .
Slew rate	SR	1.125		V/ns	With respect to V_{IH}/V_{IL} .
Duty cycle distortion	t_{CKDCD}	0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to V_T . Includes jitter, phase noise.
Minimum pulse width	t_{CKMPW}	2.2		ns	With respect to V_T .
Input DAT (referenced to CLK)					
Input set-up time	t_{ISUddr}	0.4	-	ns	$C_{Device} \leq 6pF$ with respect to V_{IH}/V_{IL} .
Input hold time	t_{IHddr}	0.4	-	ns	$C_{Device} \leq 6pF$ with respect to V_{IH}/V_{IL} .
Slew rate	SR	1.125		V/ns	with respect to V_{IH}/V_{IL} .

Figure 5-9 HS400 Device Output Timing

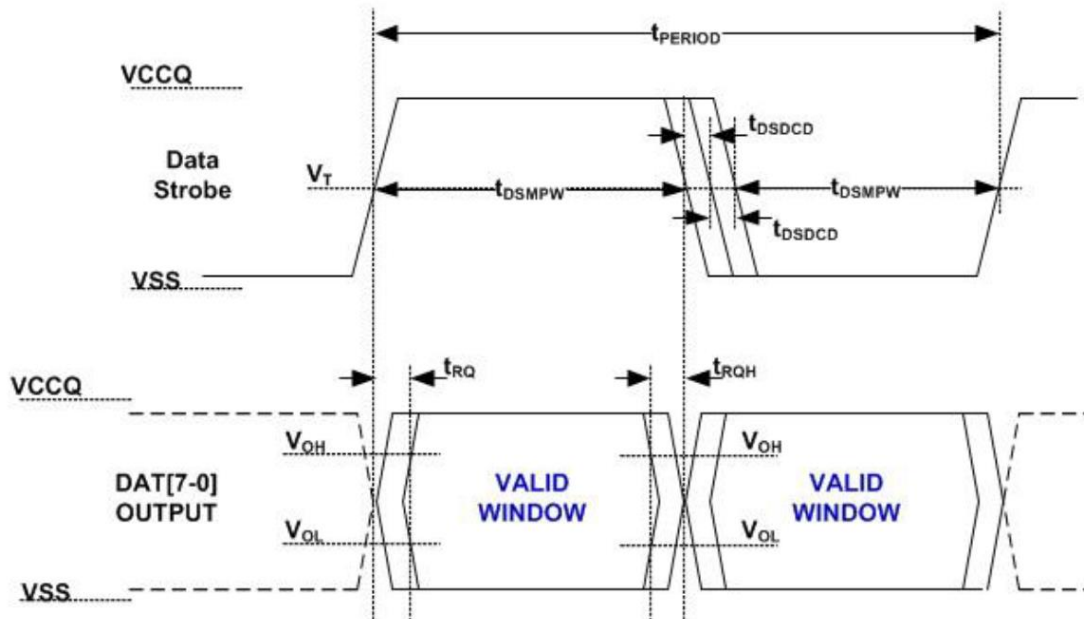


Table 5-10 HS400 Device Output Timing

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	t_{PERIOD}	5			200MHz(Max), between rising edges with respect to V_T .
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load
Duty cycle distortion	t_{DSDCD}	0	0.2	ns	Allowable deviation from an input CLK duty cycle distortion (t_{CKDCD}). With respect to V_T . Includes jitter, phase noise
Minimum pulse width	t_{DSMPW}	2		ns	With respect to V_T .
Read pre-amble	t_{RPRE}	0.4		t_{PERIOD}	Max value is specified by manufacture. Value up to infinite is valid
Read post-amble	t_{RPST}	0.4		t_{PERIOD}	Max value is specified by manufacture. Value up to infinite is valid
Output DAT (Referenced to Data Strobe)					
Output skew	t_{RQ}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load.
Output hold skew	t_{RQH}		0.4	ns	With respect to V_{OH}/V_{OL} and HS400 reference load.
Slew rate	SR	1.125		V/ns	With respect to V_{OH}/V_{OL} and HS400 reference load.

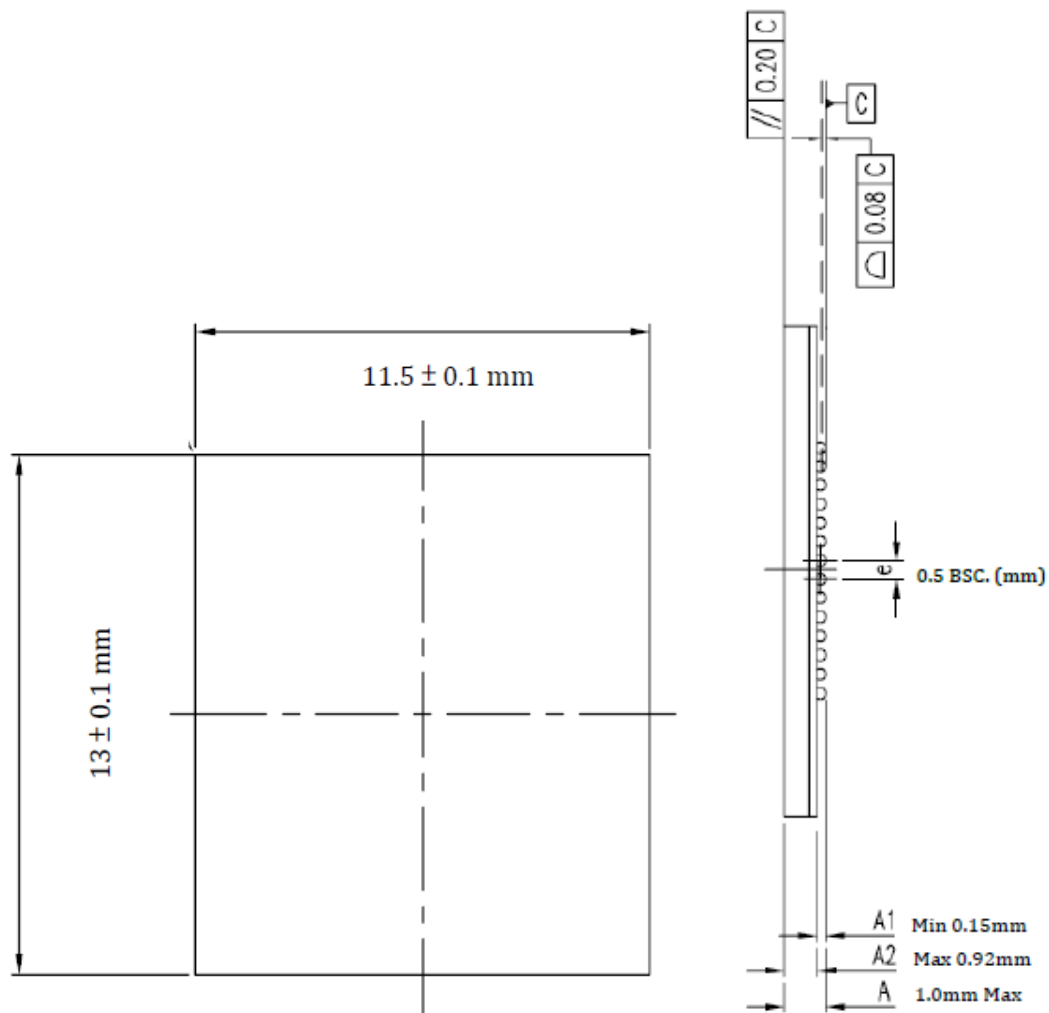
Table 5-11 HS400 Capacitance

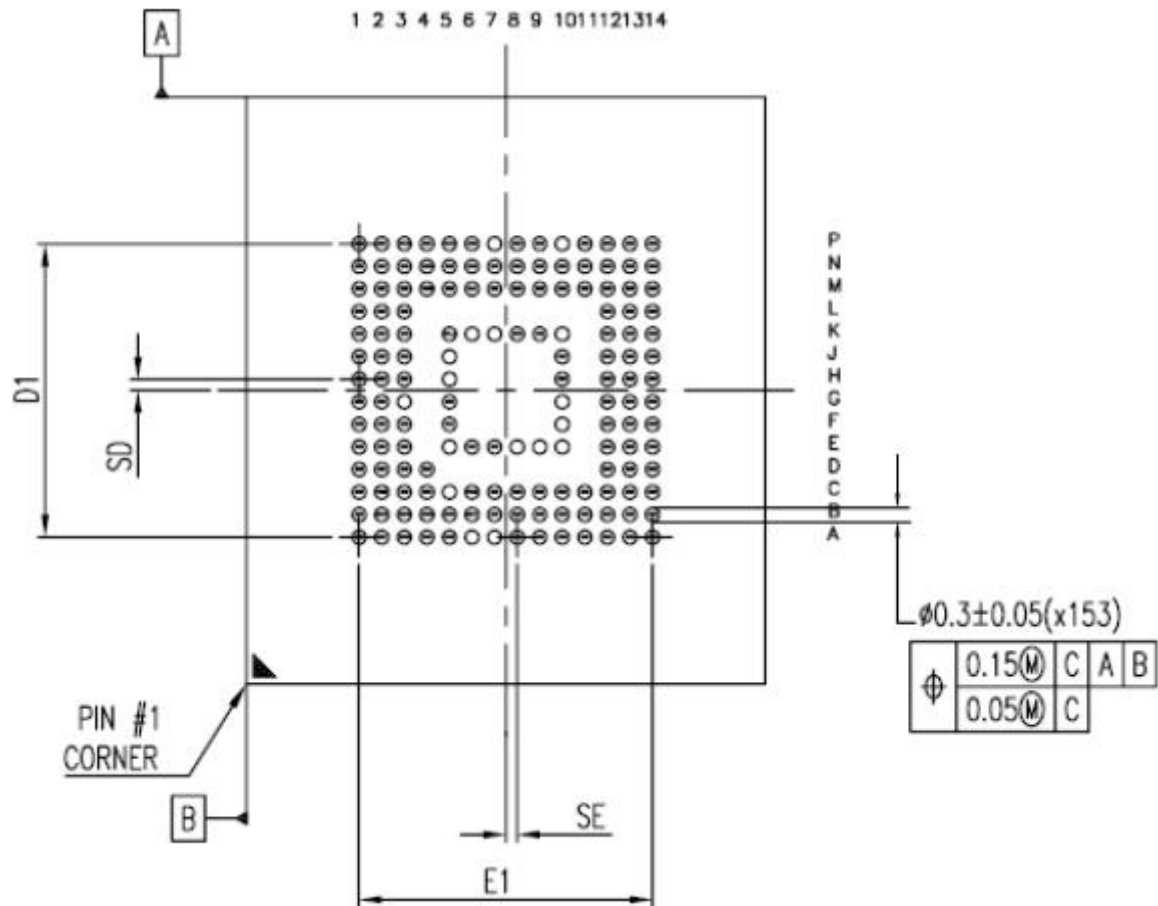
Parameter	Symbol	Min	Type	Max	Unit
Pull-up resistance for CMD	RCMD	4.7		100(1)	Kohm
Pull-up resistance for DAT0-7	R _{DAT}	10		100(1)	Kohm
Pull-down resistance for Data Strobe	R _{DS}	10		100(1)	Kohm
Internal pull up resistance DAT1-DAT7	R _{int}	10		150	Kohm
Bus signal line capacitance	CL			13	pF
Single Device capacitance	C _{Device}			6	pF

6. PACKAGE



Package Size: 11.5 x 13.0 x 1.0mm





Bottom View:

N	SE (MM)	SD (MM)	E1 (MM)	D1 (MM)	JEDEC (REF)
153	0.25 BSC.	0.25 BSC.	6.50 BSC.	6.50 BSC.	MO-276 BA

7. ORDERING INFORMATION



Capacity	MPN (Diamond Grade)	MPN (Gold Grade)	Power System	Pin Configuration	Package Size
4GB	FEMC004GSTE9-T14-17	FEMC004GSTG9-T14-17	VCCQ: 1.8V/3.3V	153 FBGA	11.5x13x1.0 (mm)
8GB	FEMC008GSTE9-T14-27	FEMC008GSTG9-T14-27	VCC: 3.3V		

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Revision History

Revision	Release Date	History
1.0	2016/06	First release
1.1	2016/07	Add "Bus Signal Line Load"
1.2	2017/02	Update Template and add 2GB
1.3	2017/06	Update Ordering Information
1.4	2018/07	Update Ordering Information
1.5	2019/05	Update Ordering Information
1.6	2023/07	Update Product Overview, Product Specification and ordering information.
1.7	2024/04	Update Product Specification