fast SiC semiconductor

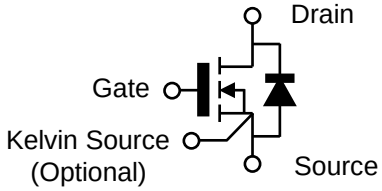
FF06060A

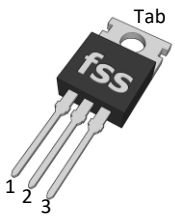
Product Datasheet

Silicon Carbide MOSFET

650V, 65mΩ SiC MOSFET – Falcon Series

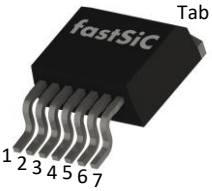
Product Information:





TO-220-3L

TOLL



TO-263-7L

Features

- Optimized $R_{DS(on)}$ with Rapid Switching Behavior
- Compatible with Standard Gate Drivers
- Clean Kelvin-Source Switching Pin-out
- High Avalanche Endurance Capability
- Optimized for High Power Density Applications
- RoHS Compliant and Halogen Free
- Validated Based on AEC-Q101 Automotive Qualified

Terminal	Packaging Type		
	TO-220-3L	TOLL	TO-263-7L
Gate	1	1	1
Drain	2, Tab	Tab	Tab
Source	3	3,4,5,6,7,8	3,4,5,6,7
Kelvin Source	--	2	2

Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Enable High Temperature Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems
- High Reliability

Potential Applications

- Switching Mode Power Supply
- PFC & DC/DC Converter
- EV Charging Station
- UPS
- Renewable Energy
- Power Inverter & Motor Driver

Key Performance Parameters

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS} @$T_{j(max)}$	700	V
Recommended Gate-Source Turn-On Voltage	V_{GS}	15~18	
Drain-Source On-State Resistance	$R_{DS(on)}$	65	mΩ
Continuous Drain Current	I_D	44	A
Pulse Drain Current	$I_{D,\ pulse}$	120	
Power Dissipation	P_{tot}	214	W
Avalanche Energy	E_{AS}	500	mJ
Gate Charge	Q_G	69	nC
Output Capacitive Charge	Q_{oss}	66	
Junction & Storage Temperature	T_j, T_{stg}	-55 to 175	°C

Part Number	Package	Marking
FF06060CA	TO-220-3L	FF06060A
FF06060FA	TOLL	FF06060A
FF06060J-7A	TO-263-7L	FF06060A

For further information about comparable products, please contact (www.fastsic.com).

Maximum Ratings: (T_j = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Voltage	V_{DSS}	650	--	--	V	V_{GS}=0V, I_D=100μA
Continuous Drain Current	I_D	--	--	44 32	A	V_{GS}=18V, T_C=25°C V_{GS}=18V, T_C=100°C
Pulse Drain Current	$I_{D,\ pulse}$	--	--	120		Per Fig. 13
Continuous Body Diode Current	I_S	--	--	30		V_{GS}=0V, T_C=25°C
Avalanche Energy, Single Pulse	E_{AS}	--	--	500	mJ	L=25mH
Operate Gate Source Voltage	$V_{GS,\ op}$	-8~0	--	15~18	V	Recommended operating values
Transient Gate Source Voltage	$V_{GS,\ tran.}$	-10	--	22		Transient operating limit (AC f > 1Hz, pulse width < 100ns)
Power Dissipation	P_{tot}	--	--	214	W	T_c=25°C
Junction Temperature	T_j	-55	--	175	°C	--
Storage Temperature	T_{stg}	-55	--	175		
Soldering Temperature	T_L	--	--	260		

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
DC Characteristics (at T_j = 25°C, unless otherwise specified)						
Drain-source Breakdown Voltage	$V_{(BR)DSS}$	650 --	-- 700	-- --	V	V_{GS}=0V, I_D=100μA, T_j=25°C V_{GS}=0V, I_D=100μA, T_j=175°C
Drain-Source On-State Resistance	$R_{DS(on)}$	-- --	65 84	80 --	mΩ	V_{GS}=18V, I_D=15A, T_j=25°C V_{GS}=18V, I_D=15A, T_j=175°C
Gate-Source Threshold Voltage	V_{th}	--	2.5	--	V	V_{GS}=V_{DS}, I_D=20mA
Zero Gate Voltage Drain Current	I_{DSS}	--	<1	60	μA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
Gate-Source Leakage Current	I_{GSS}	--	--	100	nA	V_{GS}=18V, V_{DS}=0V
Body Diode Forward Voltage	V_{SD}	-- --	3.4 2.9	-- --	V	V_{GS}=0V, I_S=7A, T_j=25°C V_{GS}=0V, I_S=7A, T_j=175°C
AC Characteristics (at T_j = 25°C, unless otherwise specified)						
Input Capacitance	C_{iss}	--	1499	--	pF	V_{DS}=400V, V_{GS}=0V, f=250kHz, V_{AC}=25mV
Output Capacitance	C_{oss}	--	113	--		
Reverse Capacitance	C_{rss}	--	17	--		
Effective Output Capacitance, energy related	$C_{o(er)}$[1]	--	124	--		
Effective Output Capacitance, time related	$C_{o(tr)}$[2]	--	164	--		
C_{oss} Stored Energy	E_{oss}	--	10	--	μJ	
Output Capacitive Charge	Q_{oss}	--	66	--	nC	
Internal Gate Resistance	$R_{G,\ int.}$	--	2.2	--	Ω	f=1MHz, V_{AC}=25mV

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V.

Switching Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate Characteristics						
Gate to Source Charge	Q_{GS}	--	11	--	nC	V_{DS}=400V, V_{GS}=0V/15V, I_D=15A
Gate to Drain Charge	Q_{GD}	--	34	--		
Total Gate Charge	Q_G	--	69	--		
Inductive Load						
Turn On Delay Time	$t_{d(on)}$	--	33	--	ns	V_{DS}=400V, I_D=13A, V_{GS}=-3/+15V, $R_{G(ext.)}$= 2.7Ω External SiC Diode as an FWD
Rise Time	t_r	--	28	--		
Turn Off Delay Time	$t_{d(off)}$	--	21	--		
Fall Time	t_f	--	11	--		
Turn On Switching Energy	E_{on}	--	87	--	µJ	
Turn Off Switching Energy	E_{off}	--	11	--		
Resistive Load						
Turn On Delay Time	$t_{d(on)}$	--	18	--	ns	V_{DS}=400V, I_D=13.3A, V_{GS}=-3/+15V, R_G=2.7Ω, R_L=30Ω
Rise Time	t_r	--	11	--		
Turn Off Delay Time	$t_{d(off)}$	--	23	--		
Fall Time	t_f	--	24	--		
Body Diode Characteristics						
Reverse Recovery Charge	Q_{rr}	--	42	--	nC	V_{GS}=0V, I_S=13A, V_{DS}=400V, di/dt=476A/µs *Q_{rr} herein excluded the Q_{oss} value.
Reverse Recovery Time	t_{rr}	--	15	--	ns	
Peak Reverse Recovery Current	I_{rrm}	--	4.3	--	A	

Thermal Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal Impedance, junction-case	$R_{th\text{-}jc}$	--	0.7	--	K/W	--
Thermal Impedance, junction-ambient	$R_{th\text{-}ja}$	--	40	--		Device on PCB, with 6 cm² of cooling area

Electrical Characteristics Diagrams

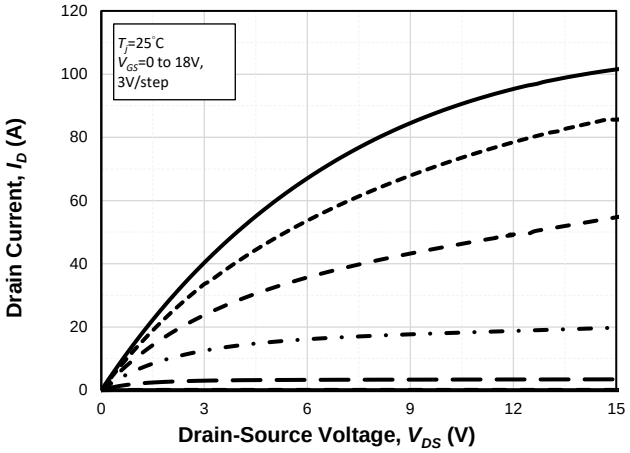


Fig. 1 Typical Output Characteristics at T_j=25˚C

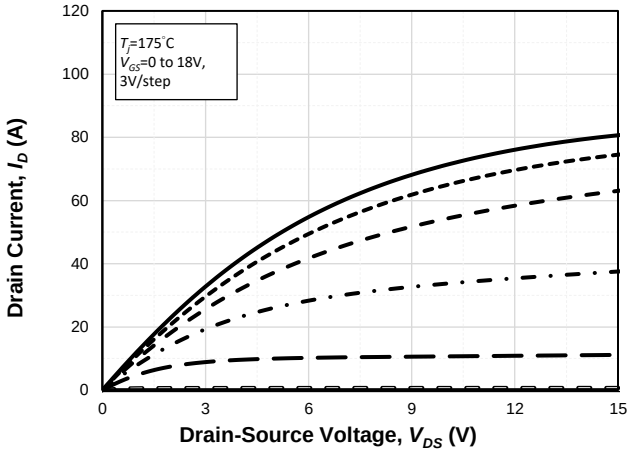


Fig. 2 Typical Output Characteristics at T_j=175˚C

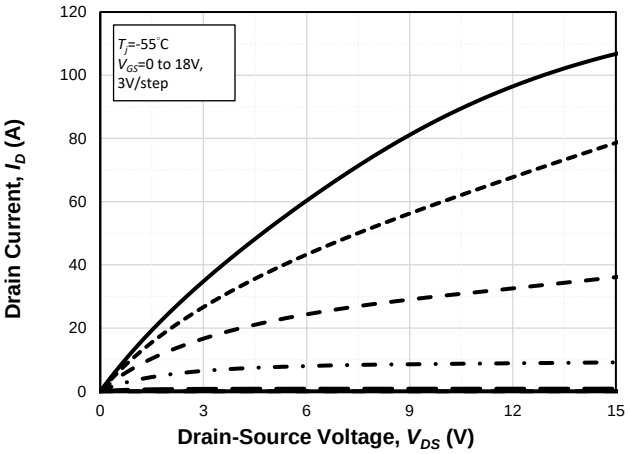


Fig. 3 Typical Output Characteristics at T_j=-55˚C

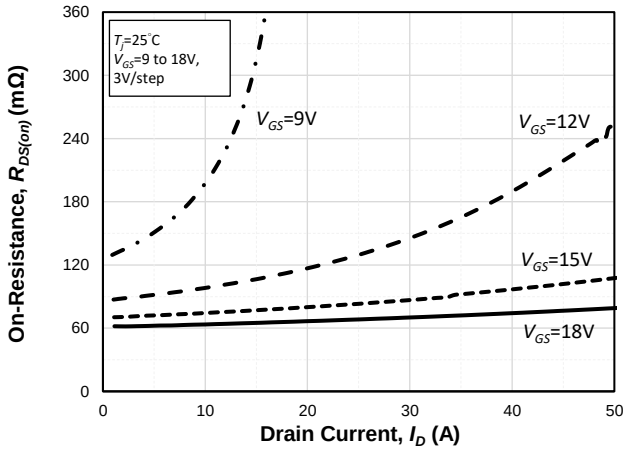


Fig. 4 Typ. $R_{DS(on)}$ vs. I_D with Various V_{GS}

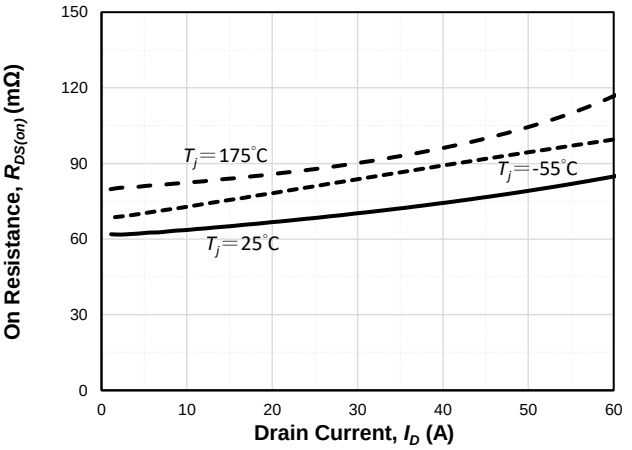


Fig. 5 Typ. $R_{DS(on)}$ vs. I_D with Various T_j, V_{GS}=18V

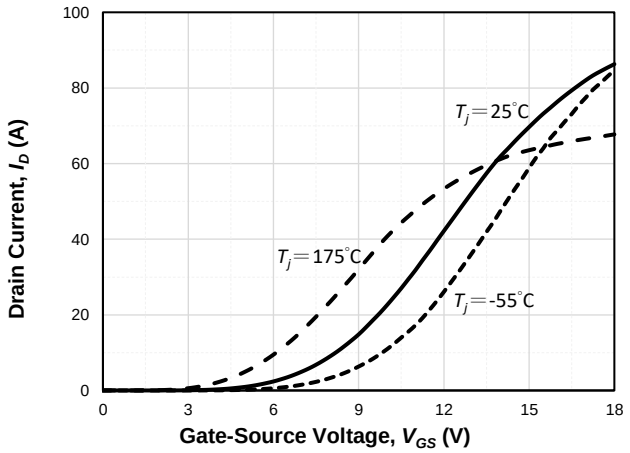


Fig. 6 Typ. I_D vs. V_{GS} with Various T_j, V_{DS}=10V

Electrical Characteristics Diagrams

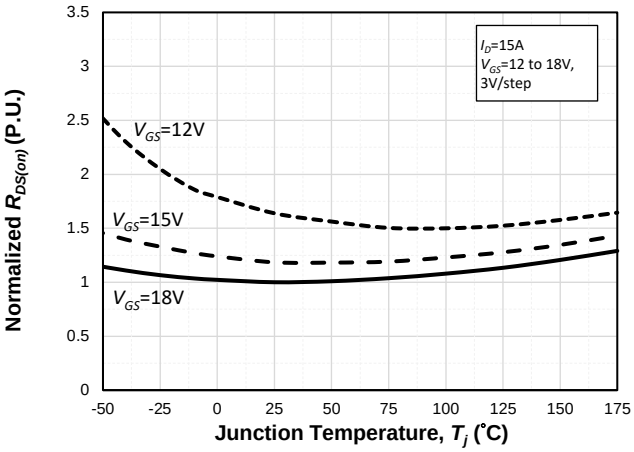


Fig. 7 Normalized $R_{DS(on)}$ vs. T_j with Various V_{GS}

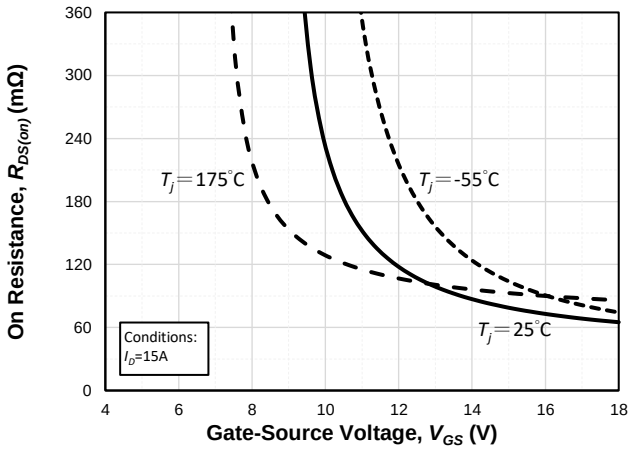


Fig. 8 Typ. $R_{DS(on)}$ vs. V_{GS} with Various T_j

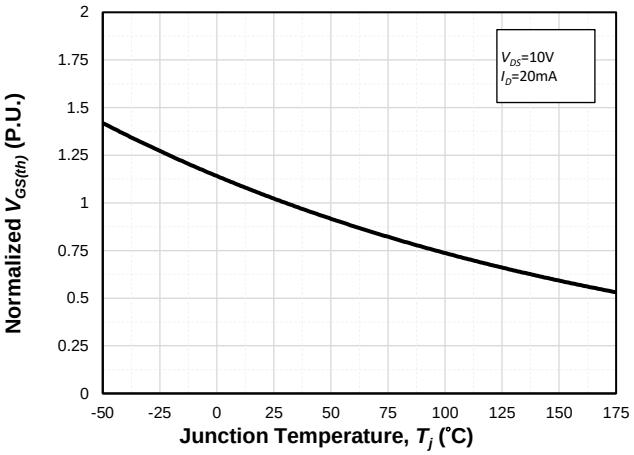


Fig. 9 Normalized V_{th} vs. T_j

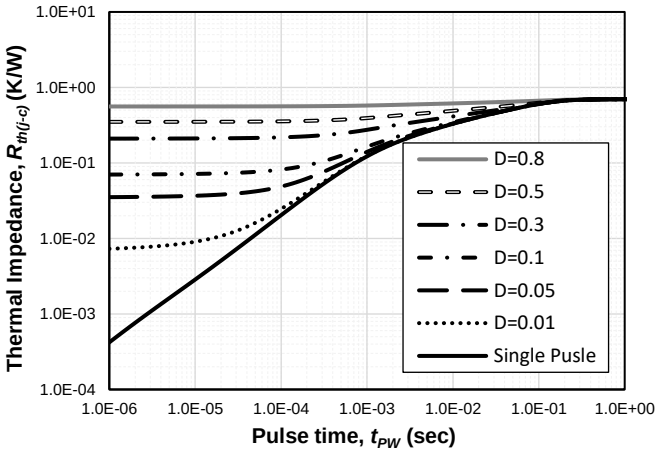


Fig. 10 Typ. Transient Thermal Impedance $R_{th\text{-}jc}$

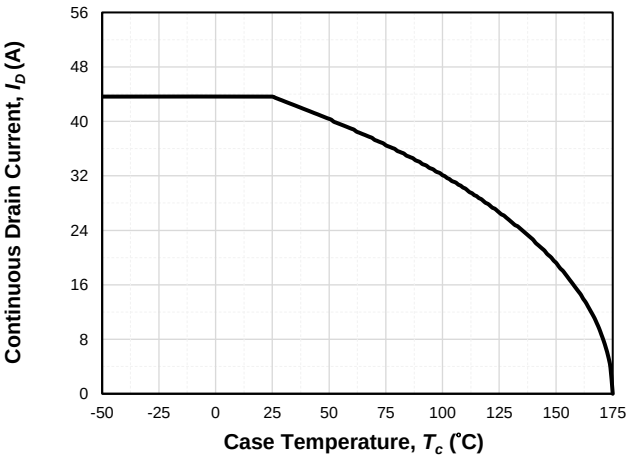


Fig. 11 Continuous I_D De-rating at V_{GS}=18V, T_j≤175˚C

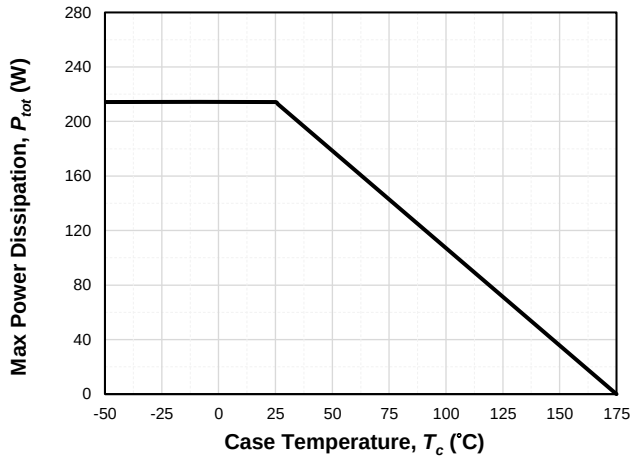


Fig. 12 Power Dissipation at V_{GS}=18V, T_j≤175˚C

Electrical Characteristics Diagrams

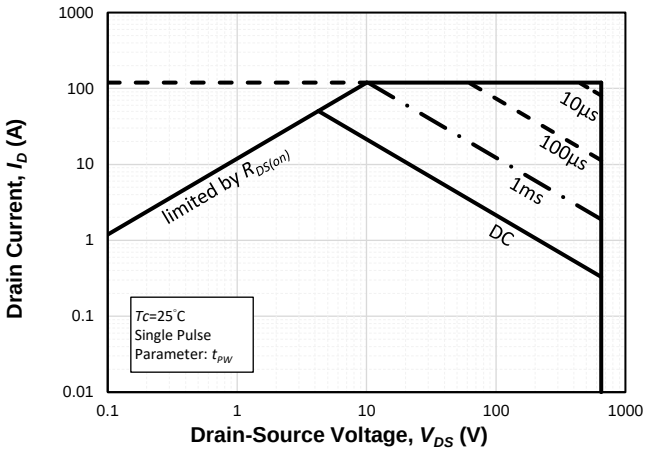


Fig. 13 Safe Operating Area at T_c=25˚C

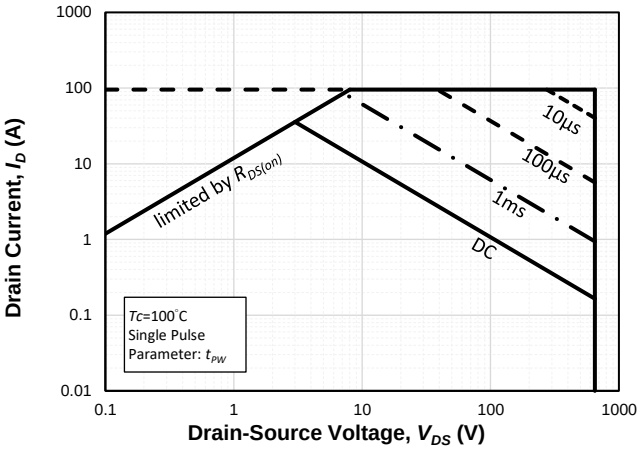


Fig. 14 Safe Operating Area at T_c=100˚C

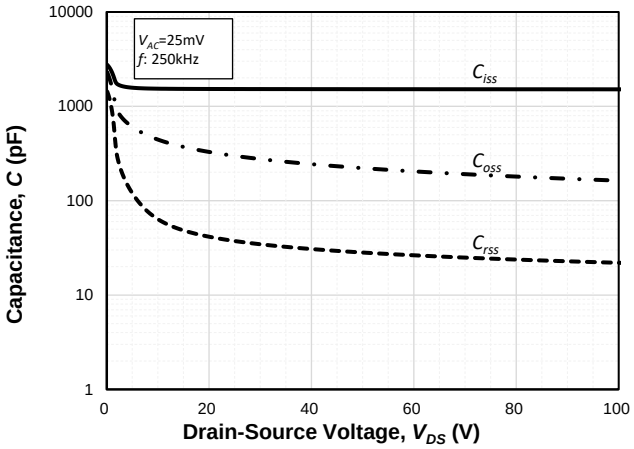


Fig. 15 Typ. Capacitance vs. V_{DS} at f_{sw}=250kHz, V_{DS}≤100V

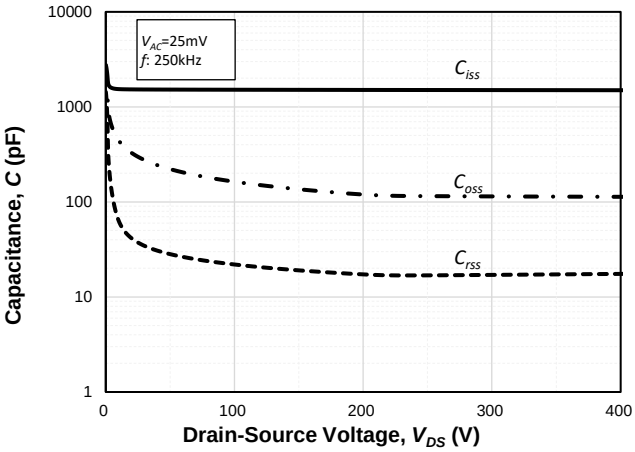


Fig. 16 Typ. Capacitance vs. V_{DS} at f_{sw}=250kHz, V_{DS}≤400V

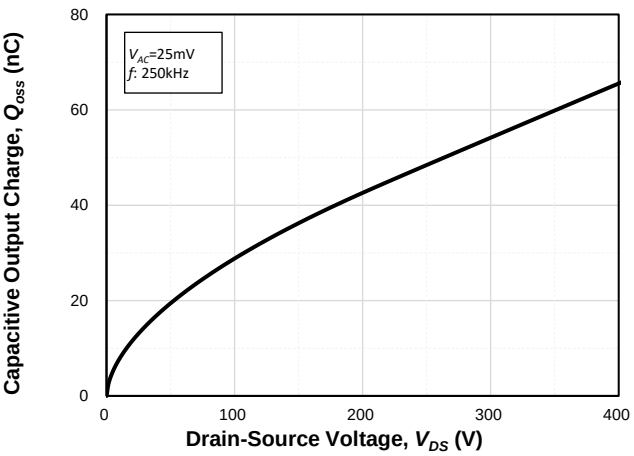


Fig. 17 Typ. Capacitive Output Charge at f_{sw}=250kHz

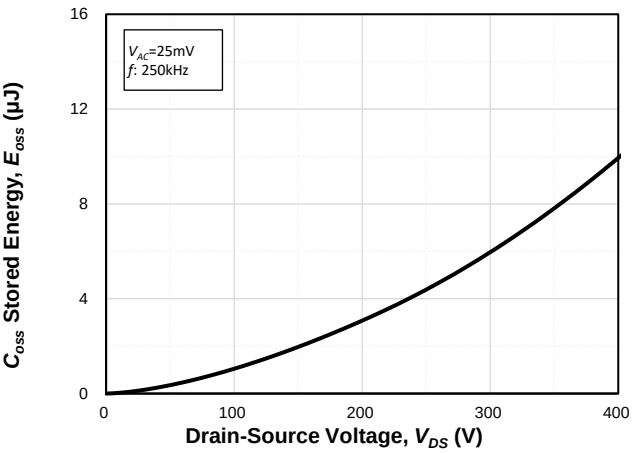


Fig. 18 Typ. C_{oss} Stored Energy at f_{sw}=250kHz

Electrical Characteristics Diagrams

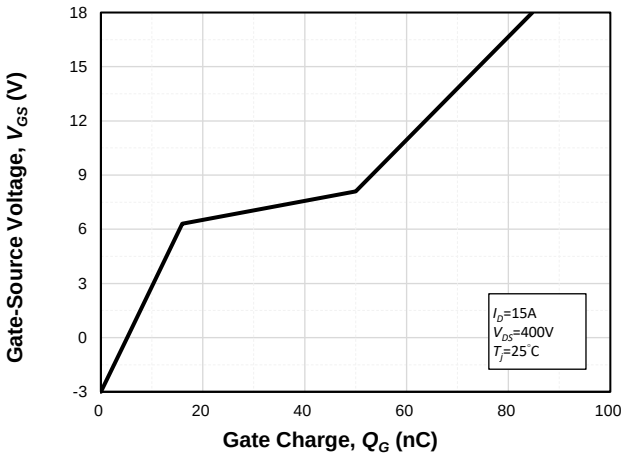


Fig. 19 Typ. Gate Charge at V_{DS}=400V, I_D=15A

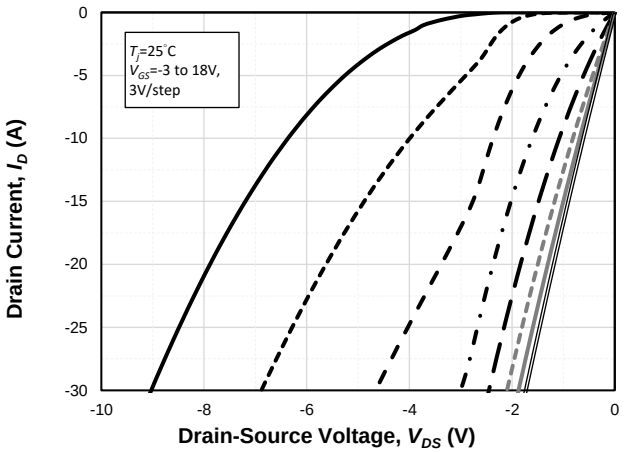


Fig. 20 Typical Forward Characteristics of Reverse Conduction at T_j=25˚C

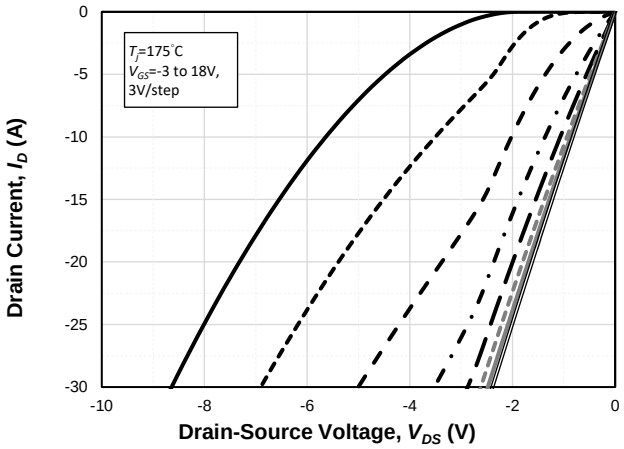


Fig. 21 Typical Forward Characteristics of Reverse Conduction at T_j=175˚C

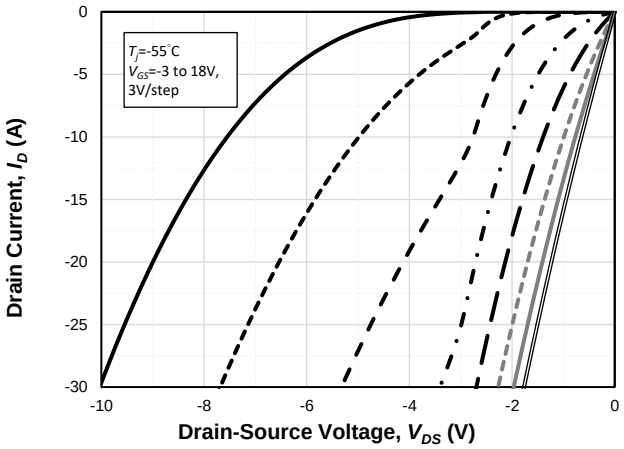


Fig. 22 Typical Forward Characteristics of Reverse Conduction at T_j=-55˚C

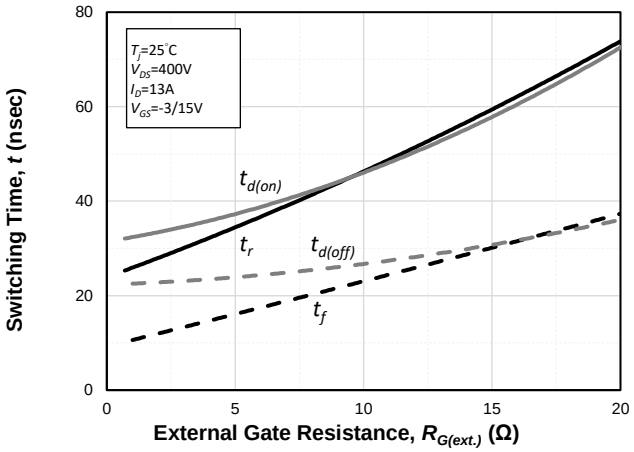


Fig. 23 Typ. Switching Time vs. $R_{G(ext.)}$

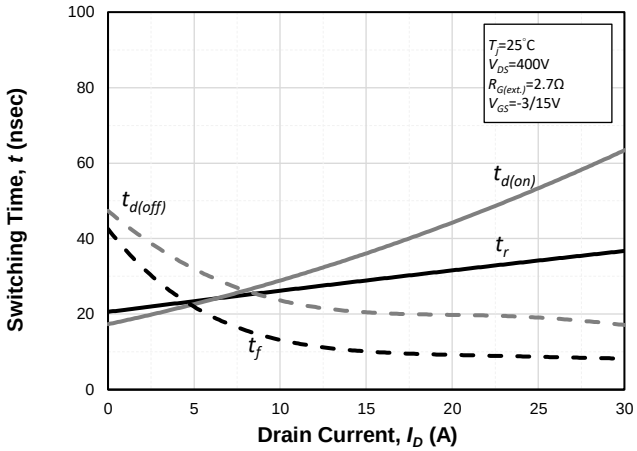


Fig. 24 Typ. Switching Time vs. I_D

Electrical Characteristics Diagrams

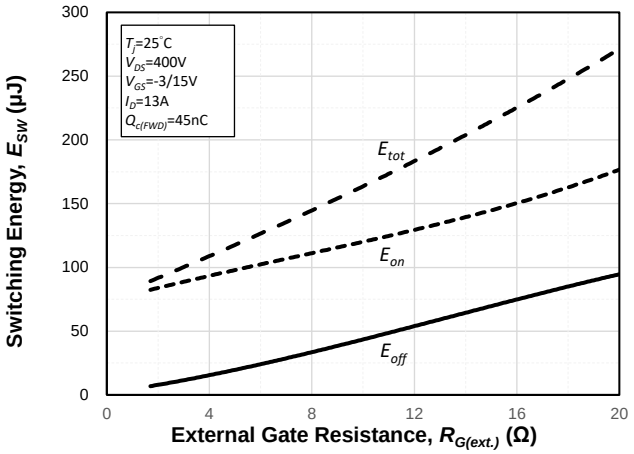


Fig. 25 Typ. Switching Energy vs. $R_{G(ext.)}$

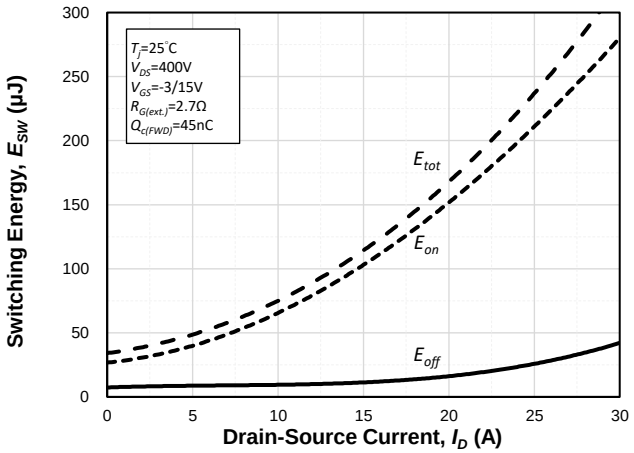
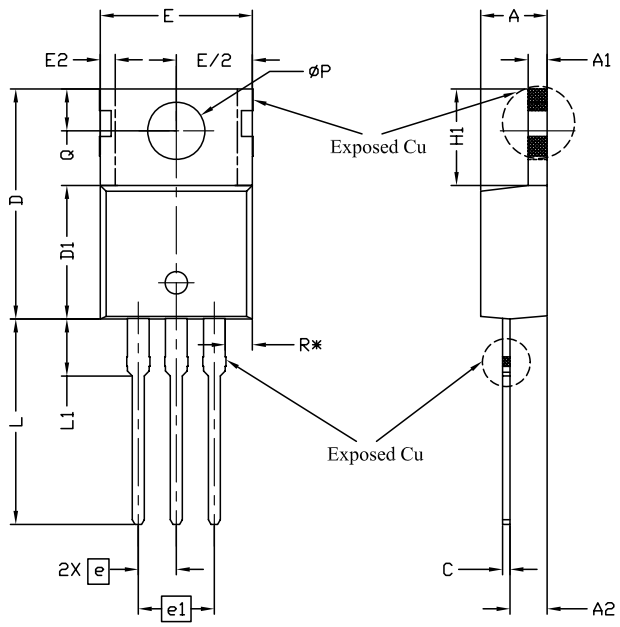
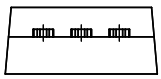
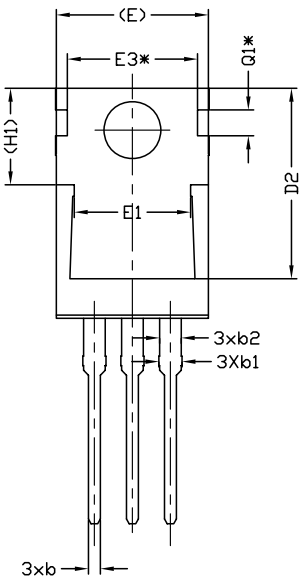


Fig. 26 Typ. Switching Energy vs. I_D

Package Outline (TO-220-3L)





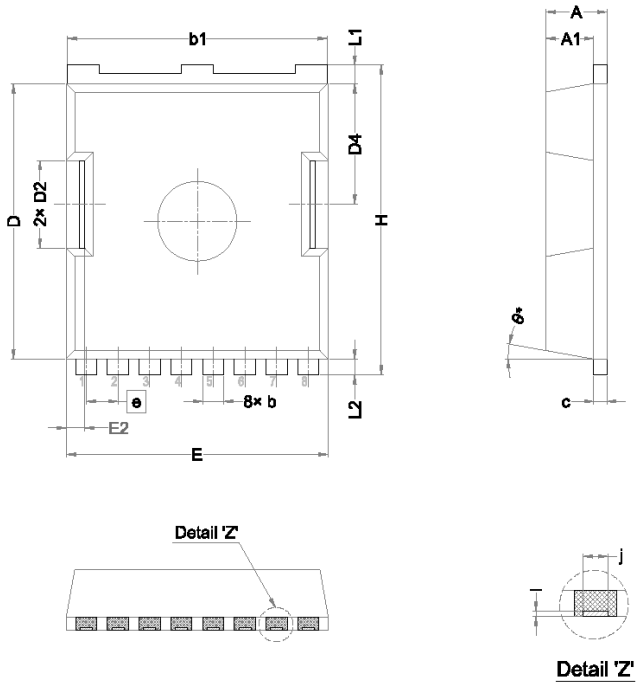


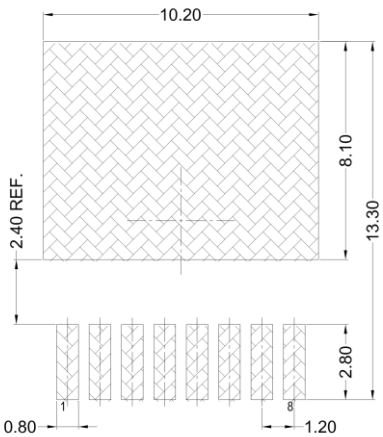
Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
A	4.24	4.44	4.64
A1	1.15	1.27	1.40
A2	2.30	2.48	2.70
b	0.70	0.80	0.90
b1	1.20	1.55	1.75
b2	1.20	1.45	1.70
c	0.40	0.50	0.60
D(2)	14.70	15.37	16.00
D1	8.82	8.92	9.02
D2(3)	12.43	12.73	12.83
E(2), (3)	9.96	10.16	10.36
E1(3)	6.86	7.77	8.89
E2(4)	--	--	0.76
E3*	8.70 REF.		
e	2.54 BSC.		
e1	5.08 BSC.		
H1(3), (4)	6.30	6.45	6.60
L	13.47	13.72	13.97
L1	3.60	3.80	4.00
ΦP	3.75	3.84	3.93
Q	2.60	2.80	3.00
Q1*	1.73 REF.		
R*	1.82 REF.		

Note:

1. Slot required; notch may be rounded.
2. Dimension D & E do not include mold flash. Mold flash shall not exceed 0.127mm pre side. These dimensions are measure at the outermost extreme of the plastic body.
3. Thermal pad contour optional within dimensions E, H1, D2 & E1.
4. Dimension E2 & H1 define a zone where stamping and singulation irregularities are allowed.
5. "*" is for reference.

Package Outline (TOLL, MO-299B)





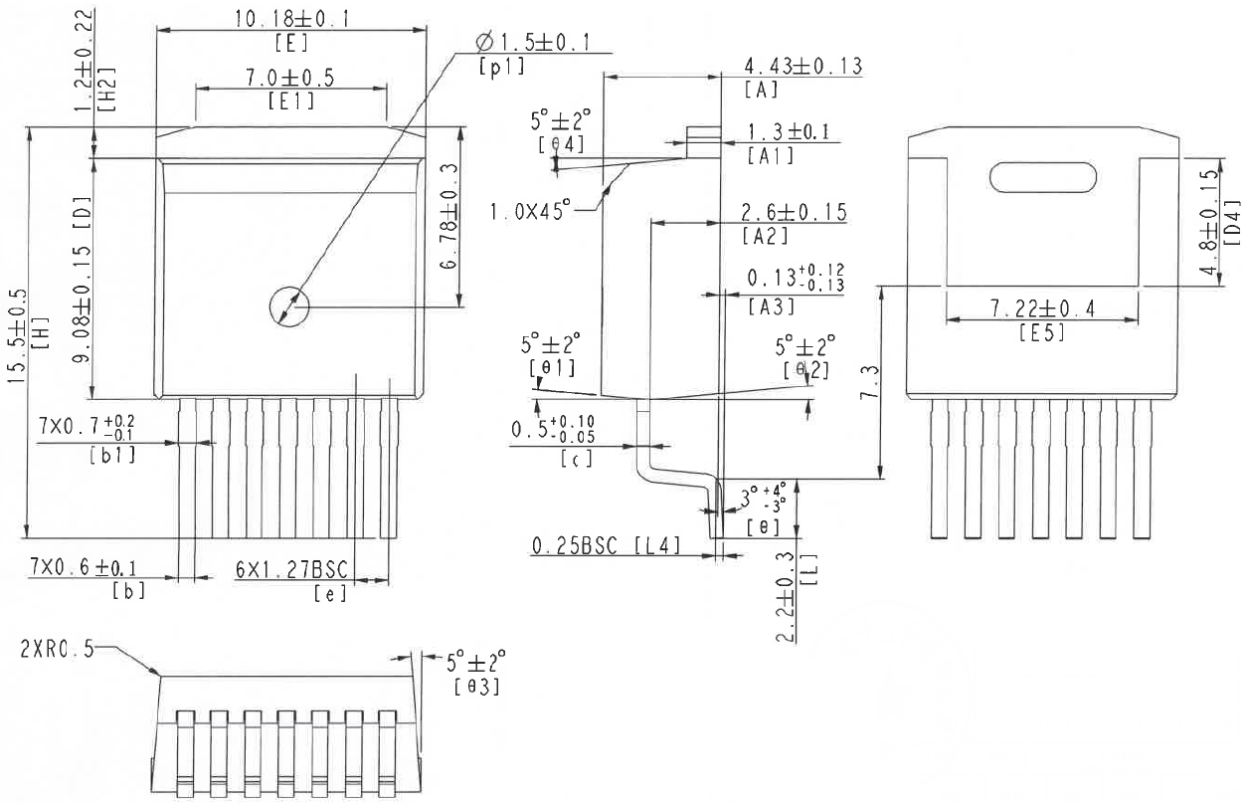
Land Pattern (Only for reference)

Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b3	1.10	1.20	1.30
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D4	4.45	4.55	4.65
E	9.80	9.90	10.00
E1	8.00	8.10	8.20
E2	0.60	0.70	0.80
e		1.20 BSC.	
H	11.58	11.68	11.78
H1		6.95 BSC.	
H2		5.89 BSC.	
i		0.10 REF.	
j		0.46REF.	
K		2.80 REF.	
L	1.40	1.90	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.30	0.70	0.80
N		8	
Q		6.80 REF.	
R	3.00	3.10	3.20
θ		10° REF.	

Note:

1. Dimensions do not inclusive burrs and mold flash.
2. "*" is for reference.

Package Outline (TO-263-7L)



Revision History

Date	Revision	Changes
23.04	Preliminary	1st issue
23.04	Preliminary	Update dynamic characteristics
23.05	Preliminary	Revise P/N
24.04	Preliminary	Minor change
24.11	Preliminary	Update pad layout

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