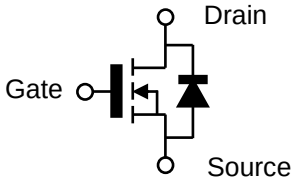
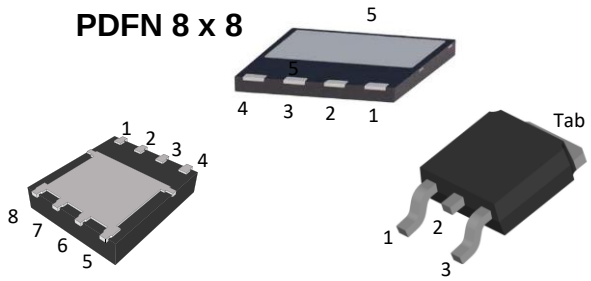
Silicon Carbide MOSFET

650V, 150mΩ SiC MOSFET – Falcon Series

Product Information:





PQFN 5 x 6 TO-252, DPAK

Features

- Optimized $R_{DS(on)}$ with Rapid Switching Behavior
- Low Profile & Low Parasitic Inductance Packaging
- Compatible with Standard 12V Gate Drivers
- High Avalanche Endurance Capability
- Optimized for High Power Density Applications
- Compact MSL-1 SMT Package
- RoHS Compliant and Halogen Free

Terminal	Packaging Type		
	TO-252	PQFN 5x6	PDFN 8x8
Gate	1	4	1
Drain	2, Tab	5, 6, 7, 8	5
Kelvin Source	--	--	2
Source	3	1, 2, 3	3, 4

Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Enable High Temperature Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems
- High Reliability

Potential Applications

- Switching Mode Power Supply
- Power Factor Correction
- Portable Adaptor
- Telecom Power
- Renewable Energy
- Class D amplifier

Key Performance Parameters

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS} @$T_{j(max)}$	700	V
Recommended Gate-Source Turn-On Voltage	V_{GS}	12~15	V
Drain-Source On-State Resistance	$R_{DS(on)}$	150	mΩ
Continuous Drain Current (DPAK, PDFN 8x8)	I_D	15	A
Continuous Drain Current (PQFN 5x6)	I_D	12.6	A
Pulse Drain Current	$I_{D,\ pulse}$	30	A
Power Dissipation (DPAK, PDFN 8x8)	P_{tot}	68	W
Power Dissipation (PQFN 5x6)	P_{tot}	44	W
Avalanche Energy	E_{AS}	113	mJ
Gate Charge	Q_G	29.5	nC
Output Capacitive Charge	Q_{oss}	24.4	nC
Junction & Storage Temperature	T_j, T_{stg}	-55 to 175	°C

Part Number	Package	Marking
FL06150A	TO-252, DPAK	FL06150
FL06150B	PQFN 5 x 6	FL06150
FL06150G	PDFN 8 x 8	FL06150

For further information about comparable products, please contact (www.fastsic.com).

Maximum Ratings: (T_j = 25°C, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Voltage	V_{DSS}	650	--	--	V	V_{GS}=0V, I_D=100μA
Continuous Drain Current	I_D	--	--	15 11	A	V_{GS}=15V, T_C=25°C V_{GS}=15V, T_C=100°C (DPAK, PDFN 8x8)
		--	--	12.6 9		V_{GS}=15V, T_C=25°C V_{GS}=15V, T_C=100°C (PQFN 5x6)
Pulse Drain Current	$I_{D,\ pulse}$	--	--	30		Per Fig. 13 and Fig. 15
Continuous Body Diode Current	I_S	--	--	12		V_{GS}=0V, T_C=25°C (DPAK, PDFN 8x8)
		--	--	9		V_{GS}=0V, T_C=25°C (PQFN 5x6)
Avalanche Energy, Single Pulse	E_{AS}	--	--	113	mJ	L=25mH
Operate Gate Source Voltage	$V_{GS,\ op}$	-6~0	--	12~15	V	Recommended operating values
Transient Gate Source Voltage	$V_{GS,\ tran.}$	-8	--	18		Transient operating limit (AC f > 1Hz, pulse width < 100ns)
Power Dissipation	P_{tot}	--	--	68	W	T_c =25°C (DPAK, PDFN 8x8)
		--	--	44		T_c =25°C (PQFN 5x6)
Junction Temperature	T_j	-55	--	175	°C	--
Storage Temperature	T_{stg}	-55	--	175		
Soldering Temperature	T_L	--	--	260		

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
DC Characteristics (at T_j = 25°C, unless otherwise specified)						
Drain-source Breakdown Voltage	$V_{(BR)DSS}$	650 --	-- 750	-- --	V	V_{GS}=0V, I_D=100μA, T_j=25°C V_{GS}=0V, I_D=100μA, T_j=175°C
Drain-Source On-State Resistance	$R_{DS(on)}$	--	150 185	--	mΩ	V_{GS}=15V, I_D=5A, T_j=25°C V_{GS}=15V, I_D=5A, T_j=100°C
Gate-Source Threshold Voltage	V_{th}	--	2.0	--	V	V_{GS}=V_{DS} ,I_D=8mA
Zero Gate Voltage Drain Current	I_{DSS}	--	<1	--	μA	V_{DS}=650V, V_{GS}=0V, T_j=25°C
Gate-Source Leakage Current	I_{GSS}	--	--	100	nA	V_{GS}=15V, V_{DS}=0V
Body Diode Forward Voltage	V_{SD}	--	2.5 2.2	--	V	V_{GS}=0V, I_S=2.5A, T_j=25°C V_{GS}=0V, I_S=2.5A, T_j=175°C
AC Characteristics (at T_j = 25°C, unless otherwise specified)						
Input Capacitance	C_{iss}	--	672	--	pF	V_{DS}=400V, V_{GS}=0V, f=250kHz, V_{AC}=25mV
Output Capacitance	C_{oss}	--	43	--		
Reverse Capacitance	C_{rss}	--	6.5	--		
Effective Output Capacitance, energy related	$C_{o(er)}$[1]	--	46	--		
Effective Output Capacitance, time related	$C_{o(tr)}$[2]	--	61	--		
C_{oss} Stored Energy	E_{oss}	--	3.7	--	μJ	
Output Capacitive Charge	Q_{oss}	--	24.4	--	nC	
Internal Gate Resistance	$R_{G,\ int.}$	--	9	--	Ω	f=1MHz, V_{AC}=25mV

[1] $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400V.
[2] $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400V.

Switching Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate Characteristics						
Gate to Source Charge	Q_{GS}	--	4.6	--	nC	V_{DS}=400V, V_{GS}=0V/12V, I_D=5A
Gate to Drain Charge	Q_{GD}	--	15	--		
Total Gate Charge	Q_G	--	29.5	--		
Inductive Load						
Turn On Delay Time	$t_{d(on)}$	--	21	--	ns	V_{DS}=400V, I_D=5A, V_{GS}=-3/+15V, $R_{G(ext.)}$= 2.7Ω External SiC Diode as an FWD
Rise Time	t_r	--	23	--		
Turn Off Delay Time	$t_{d(off)}$	--	40	--		
Fall Time	t_f	--	23	--		
Turn On Switching Energy	E_{on}	--	39	--	µJ	
Turn Off Switching Energy	E_{off}	--	6.7	--		
Resistive Load						
Turn On Delay Time	$t_{d(on)}$	--	9.8	--	ns	V_{DS}=400V, I_D=5A, V_{GS}=-3/+15V, $R_{G(ext.)}$= 2.7Ω R_L=80Ω
Rise Time	t_r	--	12.8	--		
Turn Off Delay Time	$t_{d(off)}$	--	28.5	--		
Fall Time	t_f	--	14.5	--		
Body Diode Characteristics						
Reverse Recovery Charge	Q_{rr}	--	27	--	nC	V_{GS}=0V, I_S=5A, V_{DS}=400V, di/dt=300A/µs *Q_{rr} herein excluded the Q_{oss} value.
Reverse Recovery Time	t_{rr}	--	42	--	ns	
Peak Reverse Recovery Current	I_{rrm}	--	1.2	--	A	

Thermal Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal Impedance, junction-case (DPAK, PDFN 8x8)	$R_{th\text{-}jc}$	--	2.2	--	K/W	--
Thermal Impedance, junction-case (PQFN 5x6)	$R_{th\text{-}jc}$	--	3.4	--		
Thermal Impedance, junction-ambient	$R_{th\text{-}ja}$	--	--	--		Device on PCB, with 6 cm² of cooling area

Electrical Characteristics Diagrams

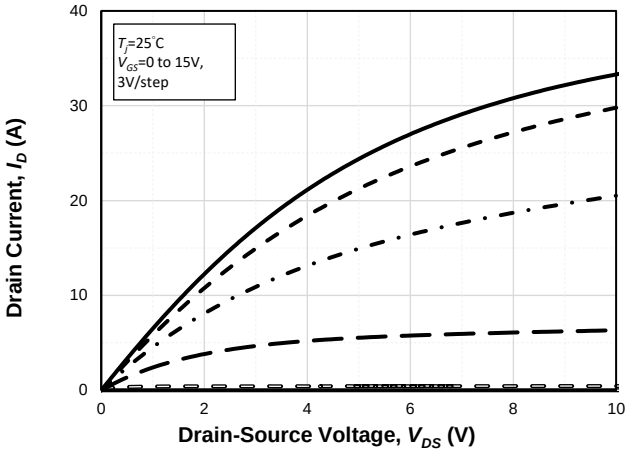


Fig. 1 Typical Output Characteristics at T_j=25˚C

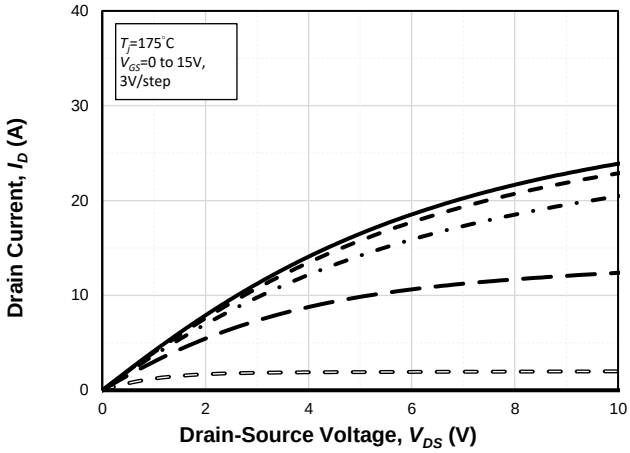


Fig. 2 Typical Output Characteristics at T_j=175˚C

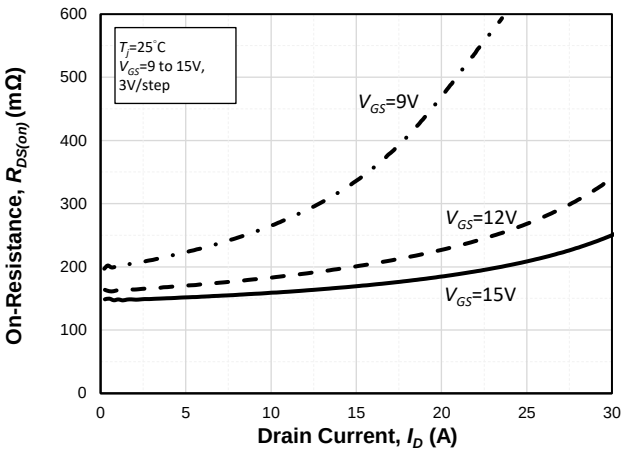


Fig. 3 Typ. $R_{DS(on)}$ vs. I_D with Various V_{GS}

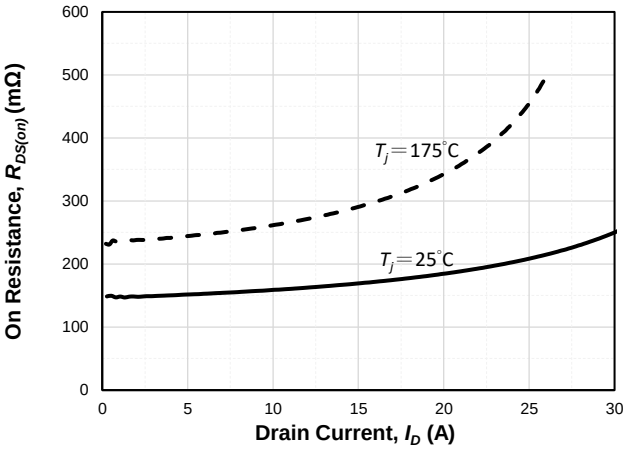


Fig. 4 Typ. $R_{DS(on)}$ vs. I_D with Various T_j, V_{GS}=15V

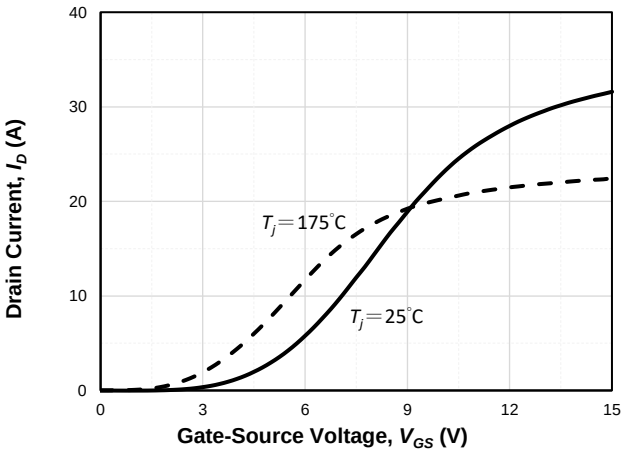


Fig. 5 Typ. I_D vs. V_{GS} with Various T_j, V_{DS}=10V

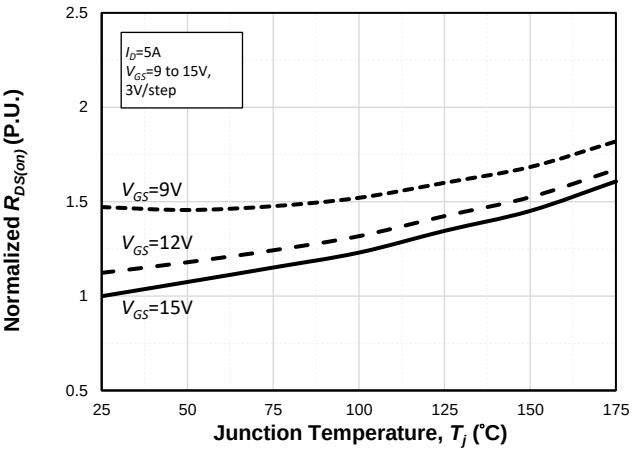


Fig. 6 Normalized $R_{DS(on)}$ vs. T_j with Various V_{GS}

Electrical Characteristics Diagrams

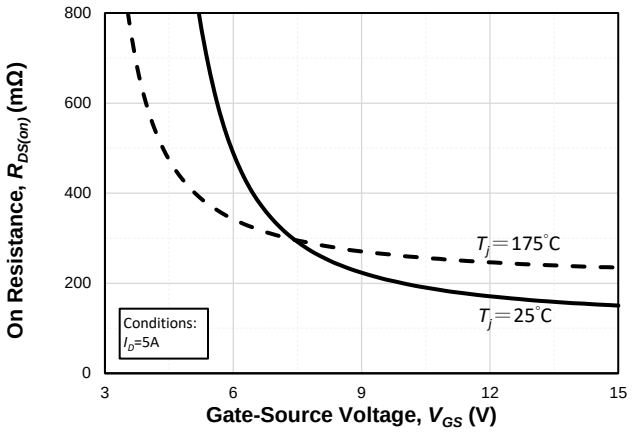


Fig. 7 Typ. $R_{DS(on)}$ vs. V_{GS} with Various T_j

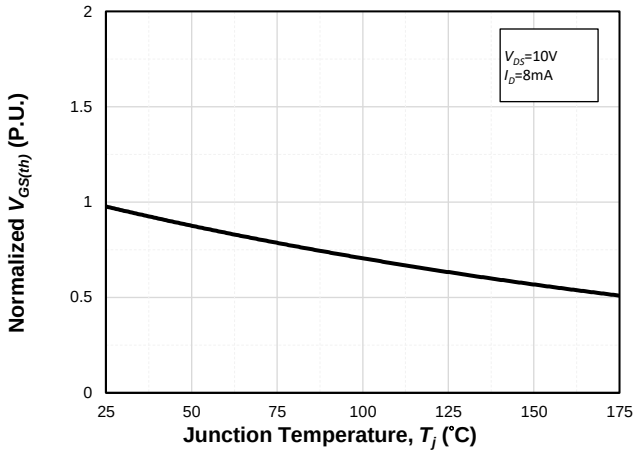


Fig. 8 Normalized V_{th} vs. T_j

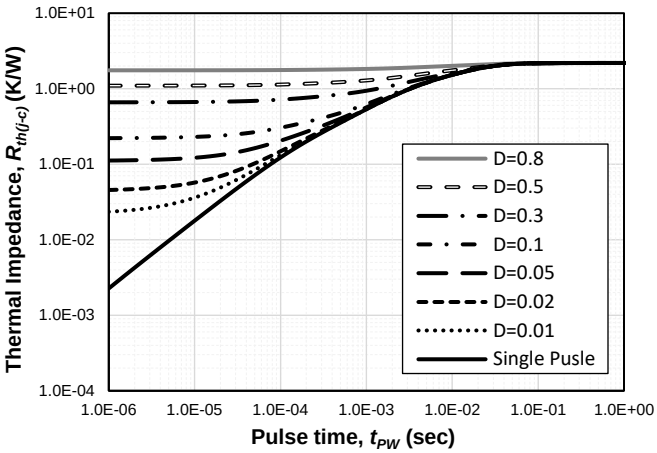


Fig. 9 Typ. Transient Thermal Impedance R_{th-jc} (DPAK, PDFN 8x8)

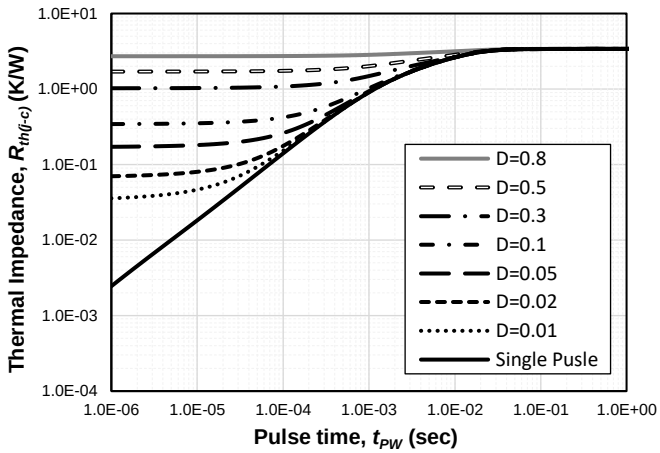


Fig. 10 Typ. Transient Thermal Impedance R_{th-jc} (PQFN 5x6)

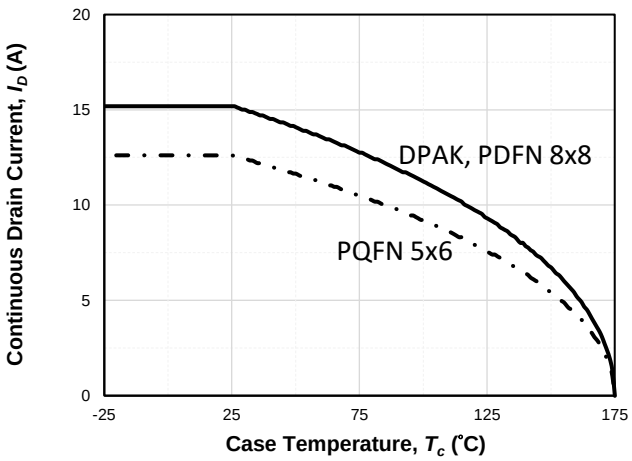


Fig. 11 Continuous I_D De-rating at V_{GS}=15V, T_j≤175˚C

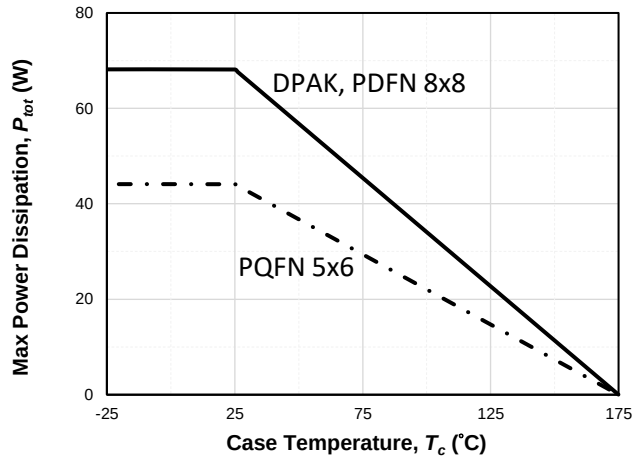


Fig. 12 Power Dissipation at V_{GS}=15V, T_j≤175˚C

Electrical Characteristics Diagrams

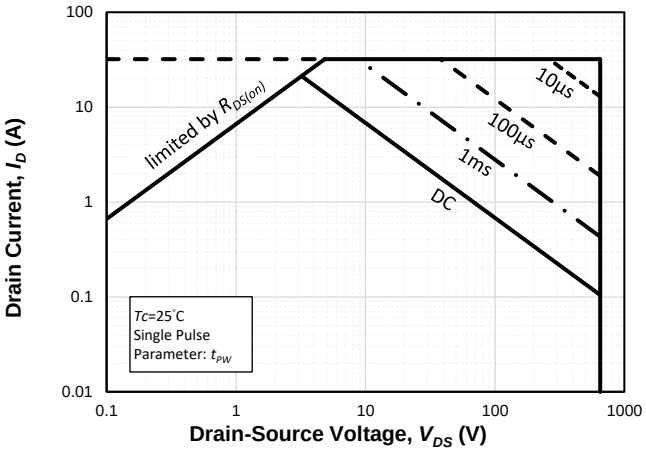


Fig. 13 Safe Operating Area at T_c=25˚C (DPAK, PDFN 8x8)

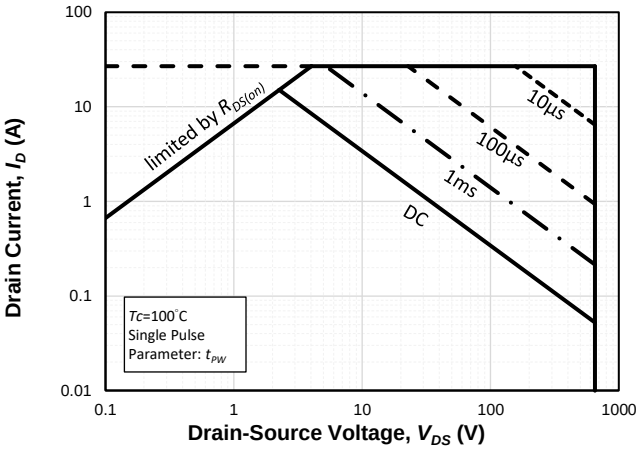


Fig. 14 Safe Operating Area at T_c=100˚C (DPAK, PDFN 8x8)

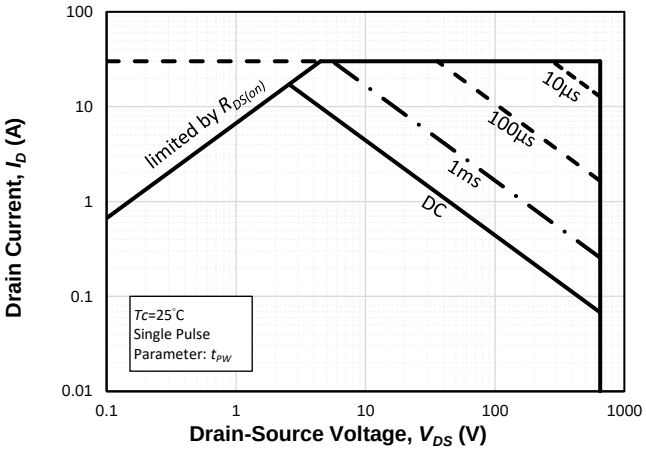


Fig. 15 Safe Operating Area at T_c=25˚C (PQFN 5x6)

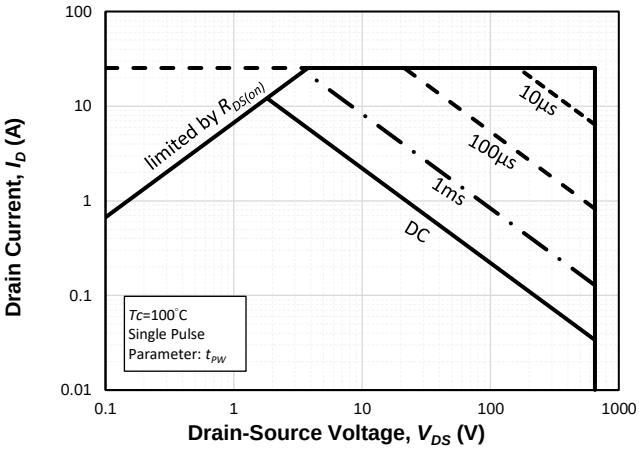


Fig. 16 Safe Operating Area at T_c=100˚C (PQFN 5x6)

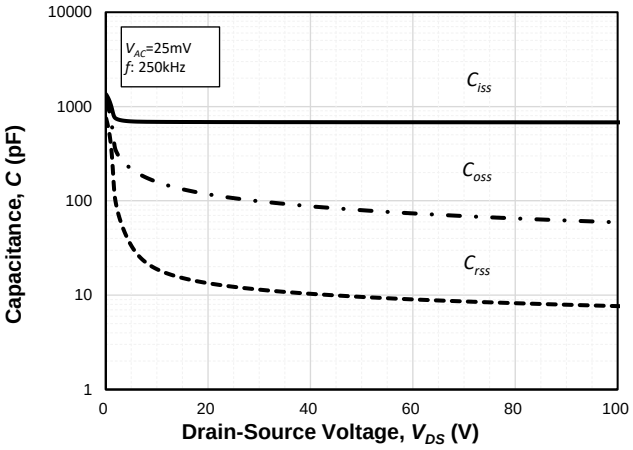


Fig. 17 Typ. Capacitance vs. V_{DS} at f_{sw}=250kHz, V_{DS}≤100V

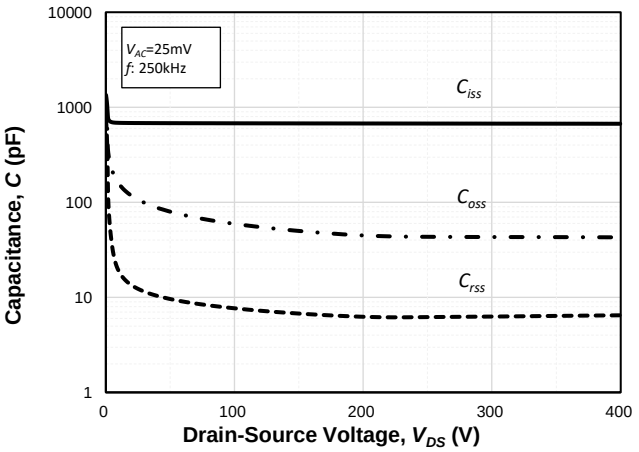


Fig. 18 Typ. Capacitance vs. V_{DS} at f_{sw}=250kHz, V_{DS}≤400V

Electrical Characteristics Diagrams

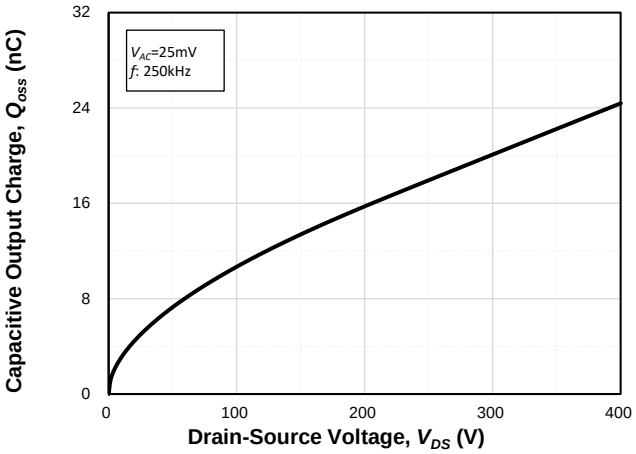


Fig. 19 Typ. Capacitive Output Charge at f_{sw}=250kHz

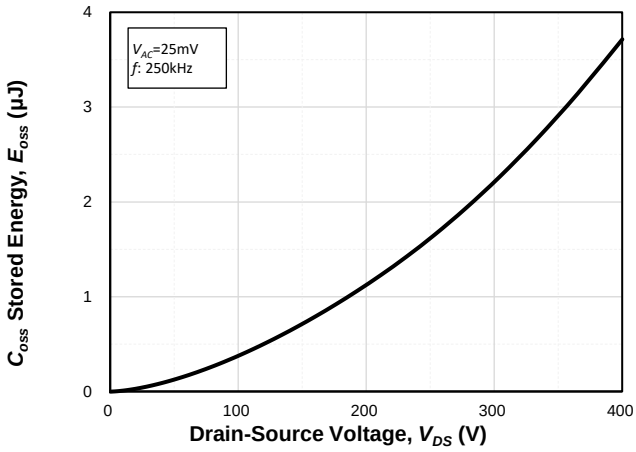


Fig. 20 Typ. C_{oss} Stored Energy at f_{sw}=250kHz

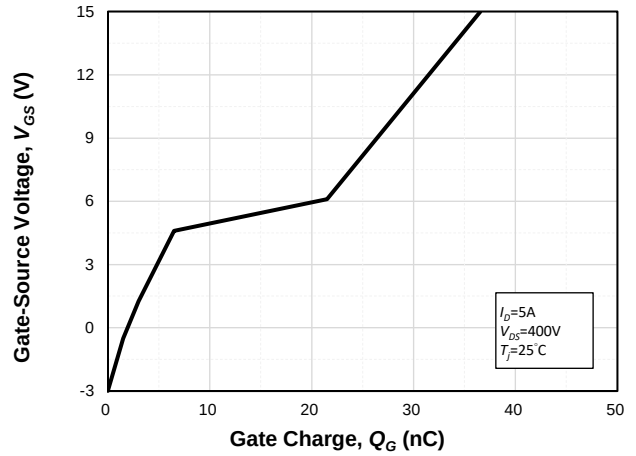


Fig. 21 Typ. Gate Charge at V_{DS}=400V, I_D=5A

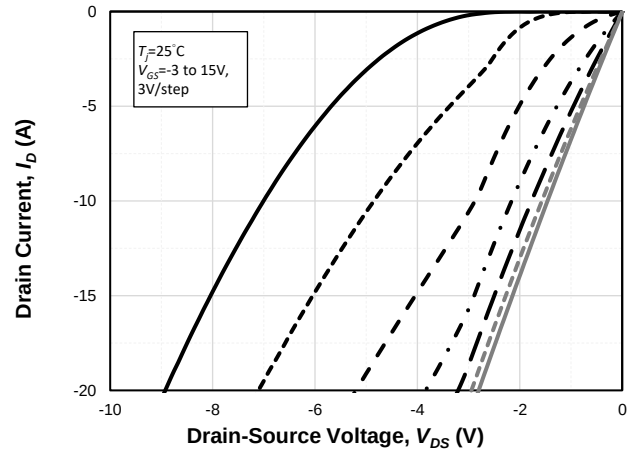


Fig. 22 Typical Forward Characteristics of Reverse Conduction at T_j=25˚C

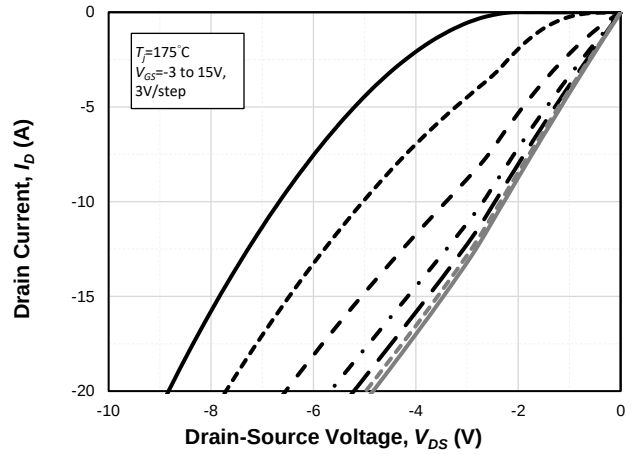


Fig. 23 Typical Forward Characteristics of Reverse Conduction at T_j=175˚C

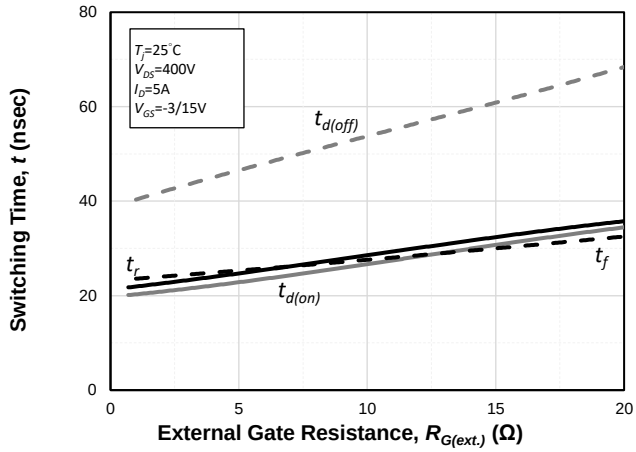


Fig. 24 Typ. Switching Time vs. $R_{G(ext.)}$

Electrical Characteristics Diagrams

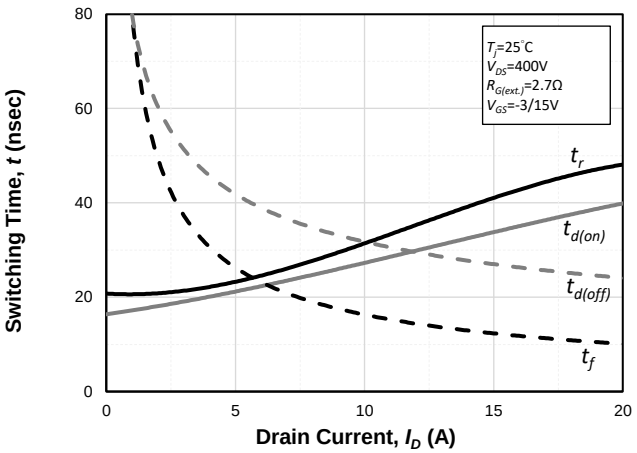


Fig. 25 Typ. Switching Time vs. I_D

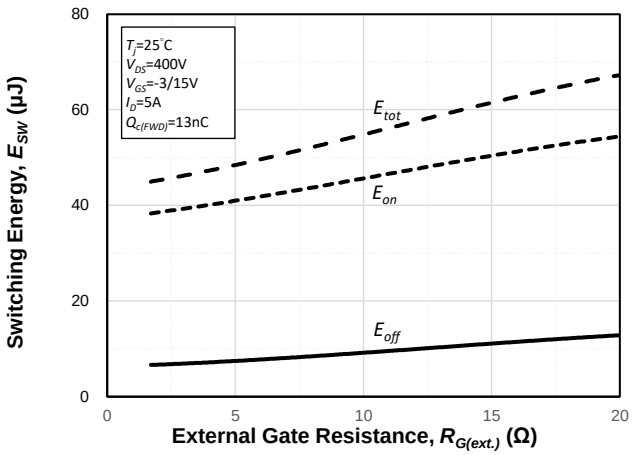


Fig. 26 Typ. Switching Energy vs. $R_{G(ext.)}$

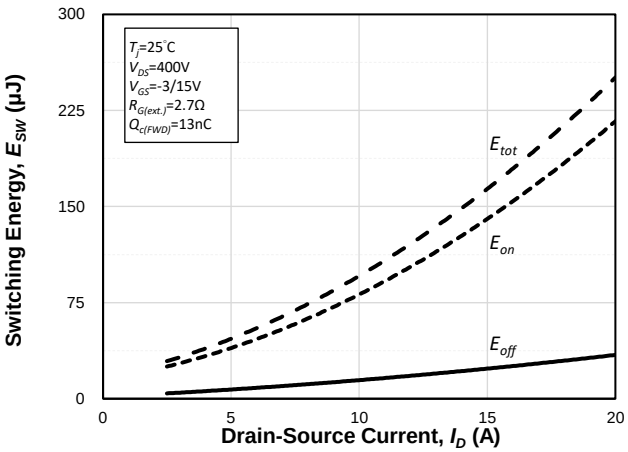
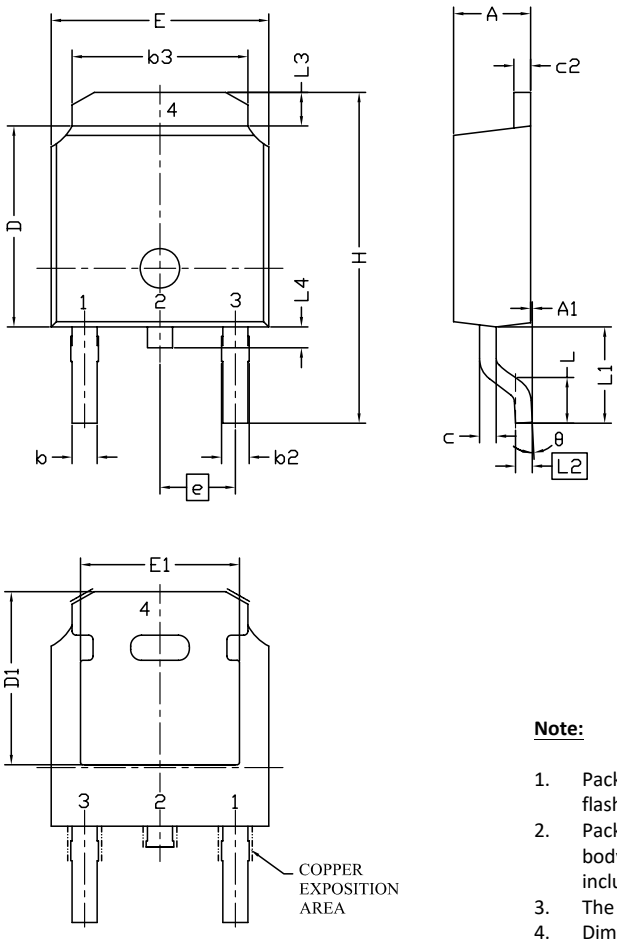


Fig. 27 Typ. Switching Energy vs. I_D

Package Outline (TO-252, DPAK)

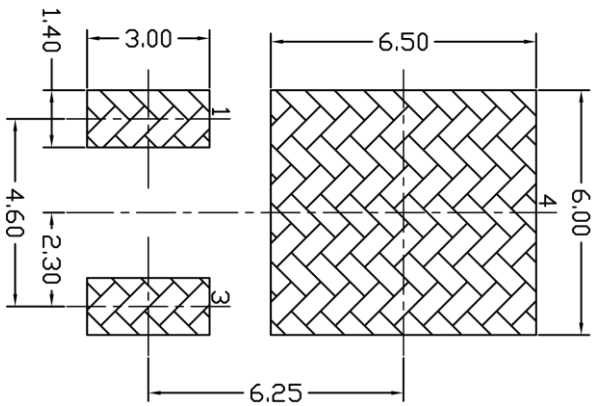


Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
E	6.40	6.60	6.73
L	1.40	1.52	1.77
L1		2.743 REF.	
L2		0.508 BSC.	
L3	0.89	--	1.27
L4	0.64	--	1.01
D	6.00	6.10	6.22
H	9.40	10.00	10.40
b	0.64	0.76	0.88
b2	0.77	0.84	1.14
b3	5.21	5.34	5.46
e		2.286 BSC.	
A	2.20	2.30	2.38
A1	0.00	--	0.127
c	0.46	0.50	0.60
c2	0.46	0.50	0.58
D1	5.21	--	--
E1	4.40	--	--
θ	0°	--	10°

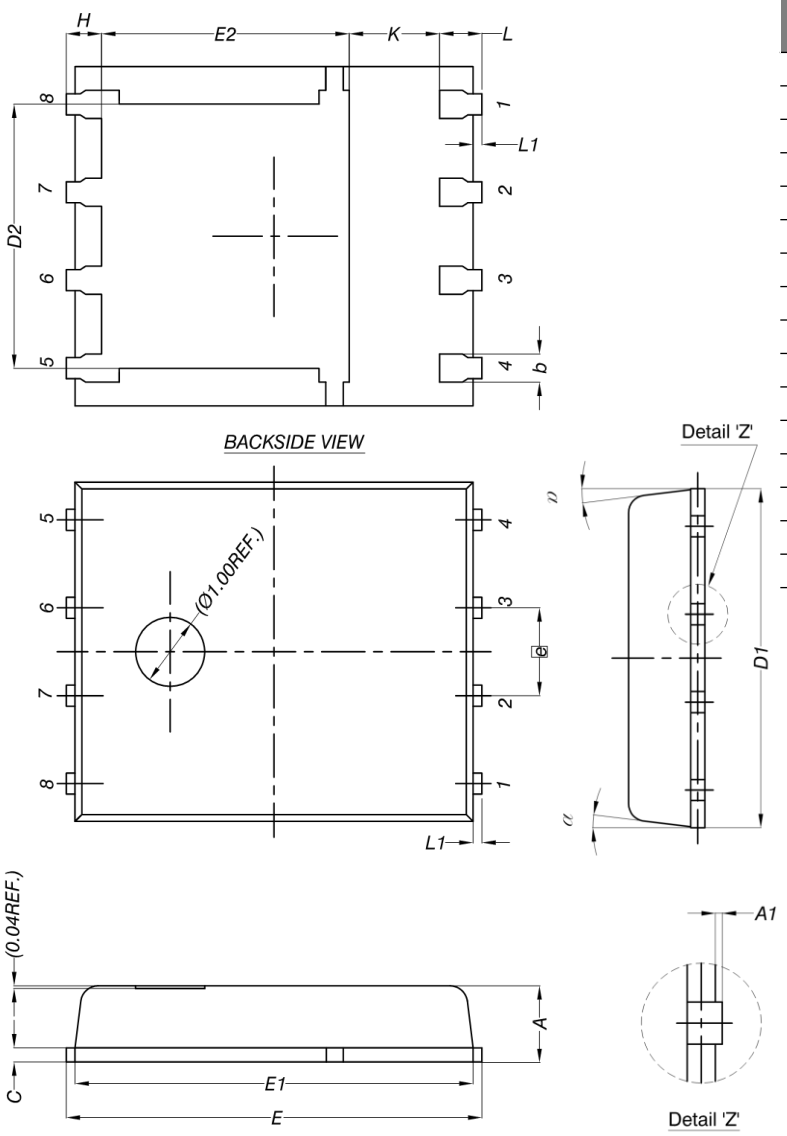
Note:

1. Package body sizes exclude mold flash, protrusion, or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side.
2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body.
3. The package top may be smaller than the package bottom.
4. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10 mm total in excess of “b” dimension at the maximum material condition. The dambar cannot be located on the lower radius of the foot.

Land Pattern (Only for Reference)



Package Outline (PQFN 5 x 6)

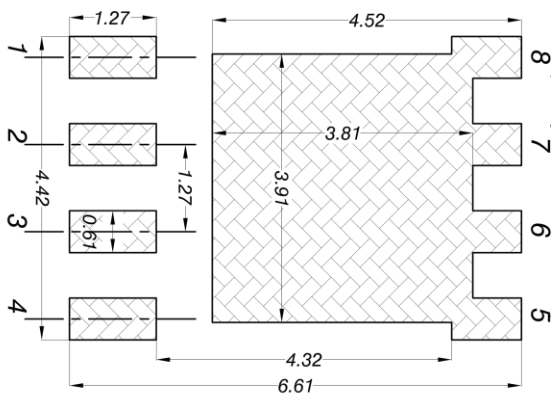


Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
A	0.90	1.00	1.10
A1	0	--	0.05
b	0.33	0.41	0.51
C	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
E	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
e		1.27 BSC.	
H	0.41	0.51	0.61
K	1.10	--	--
L	0.51	0.61	0.71
L1	0.06	0.13	020
α	0°	--	12°

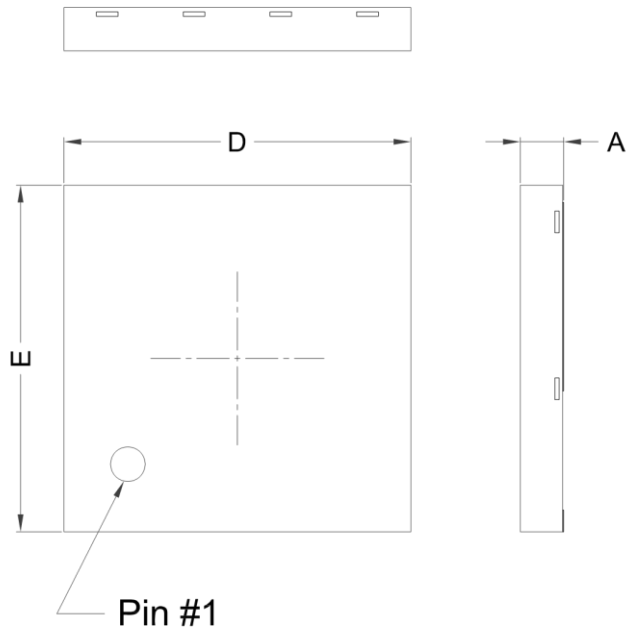
Note:

1. Package body sizes exclude mold flash, protrusion, or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 0.10 mm per side
2. Package body sizes determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar, tie bar burrs, gate burrs, and inter-lead flash, but including any mismatch between the top and bottom of the plastic body.
3. The package top may be smaller than the package bottom.

Land Pattern (Only for Reference)



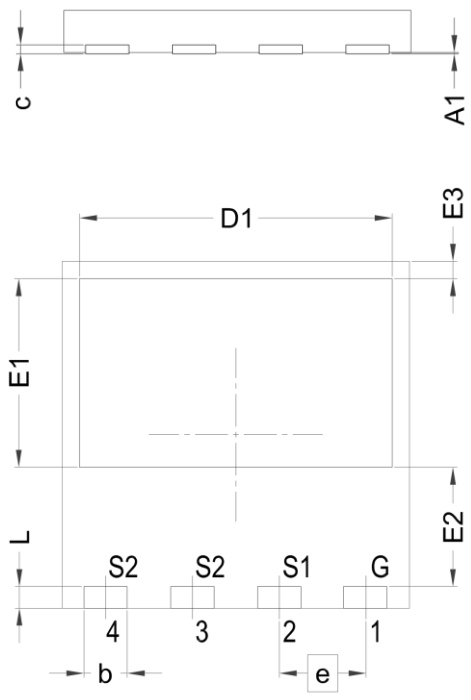
Package Outline (PDFN 8 x 8)

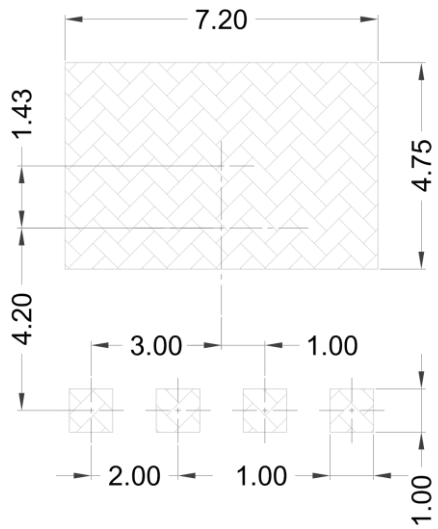


Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.90	1.00	1.10
c	0.10	0.20	0.30
D	7.90	8.00	8.10
D1	7.10	7.20	7.30
E	7.90	8.00	8.10
E1	4.25	4.35	4.45
E2	2.65	2.75	2.85
E3	0.30	0.40	0.50
e		2.00 BSC.	
L	0.40	0.50	0.60

Note:

1. All dimensions are in mm.
2. Dimensions are not inclusive burrs and mold flash.





Land Pattern (Only for reference)

Revision History

Date	Revision	Changes
22.01	Tentative	1st issue
23.01	Preliminary	Update parameters and characteristics
23.08	Preliminary	Update package type
24.07	1.0	Update to version 1.0

Important Note (Disclaimer)

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