

Dual P-Channel Enhancement Mode Power MOSFET

Description

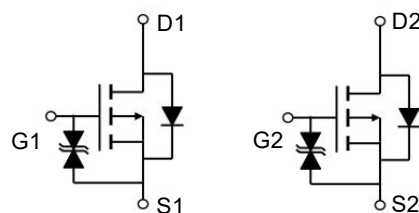
The G2K2P10S2E uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

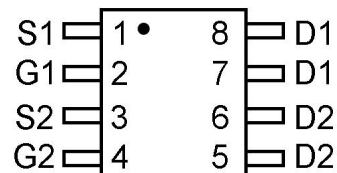
- V_{DS} -100V
- I_D (at $V_{GS} = -10V$) -3.5A
- $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 200m Ω
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 220m Ω
- 100% Avalanche Tested
- RoHS Compliant
- ESD (HBM) : 7KV

Application

- Power switch
- DC/DC converters



Schematic diagram



pin assignment



SOP-8 Dual

Ordering Information

Device	Package	Marking	Packaging
G2K2P10S2E	SOP-8 Dual	G2K2P10S2	4000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-100	V
Continuous Drain Current	I_D	-3.5	A
Pulsed Drain Current (note1)	I_{DM}	-14	A
Gate-Source Voltage	V_{GS}	± 20	V
Power Dissipation	P_D	3.1	W
Single pulse avalanche energy (note2)	E_{AS}	25	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	$^\circ\text{C}$

Thermal Resistance

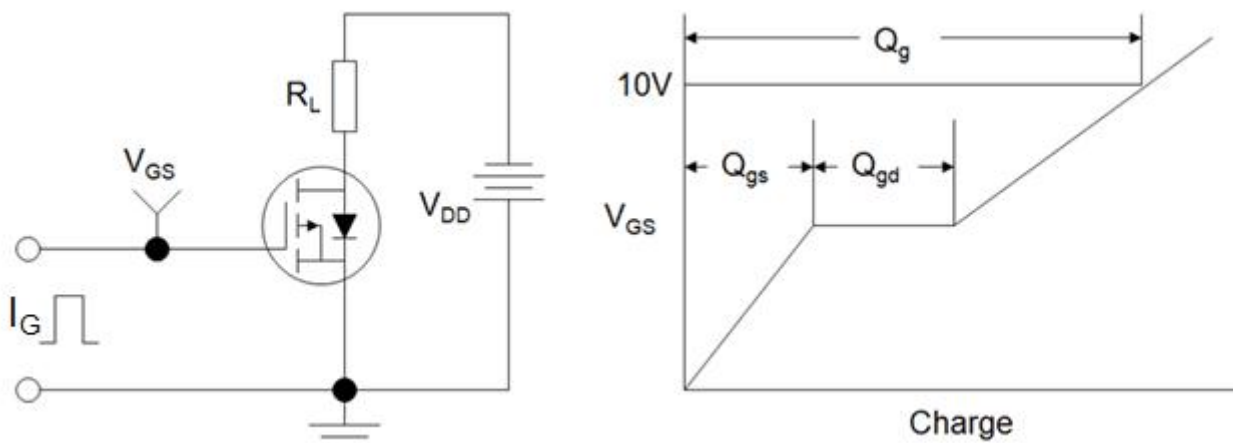
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	40	$^\circ\text{C/W}$

Specifications T _J = 25°C, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = -250μA	-100	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -100V, V _{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±10	uA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250μA	-1.0	-1.6	-2.5	V
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} = -10V, I _D = -3A	--	170	200	mΩ
		V _{GS} = -4.5V, I _D = -2A	--	180	220	
Forward Transconductance	g _{FS}	V _{DS} = -5V, I _D = -3A	--	10	--	S
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = -50V, f = 1.0MHz	--	1623	--	pF
Output Capacitance	C _{oss}		--	43	--	
Reverse Transfer Capacitance	C _{rss}		--	42	--	
Total Gate Charge	Q _g	V _{DD} = -50V, I _D = -3A, V _{GS} = -10V	--	23	--	nC
Gate-Source Charge	Q _{gs}		--	4.2	--	
Gate-Drain Charge	Q _{gd}		--	5.2	--	
Turn-on Delay Time	t _{d(on)}	V _{DD} = -50V, I _D = -3A, R _G = 3Ω	--	24	--	ns
Turn-on Rise Time	t _r		--	5	--	
Turn-off Delay Time	t _{d(off)}		--	19	--	
Turn-off Fall Time	t _f		--	11	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I _S	T _C = 25°C	--	--	-3.5	A
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = -3A, V _{GS} = 0V	--	--	-1.2	V
Reverse Recovery Charge	Q _{rr}	I _F = -3A, V _{GS} = 0V di/dt=-100A/us	--	22	--	nC
Reverse Recovery Time	T _{rr}		--	29	--	ns

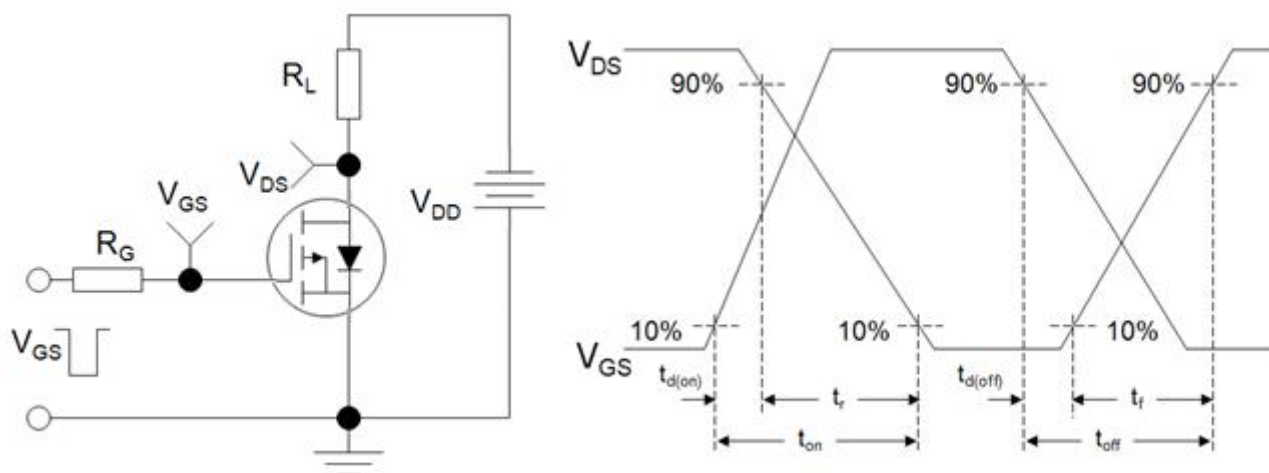
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : $T_J = 25^{\circ}\text{C}$, $V_{DD} = -50V$, $V_{GS} = -10V$, $L = 0.5mH$, $R_G = 25\Omega$
3. Identical low side and high side switch with identical R_G

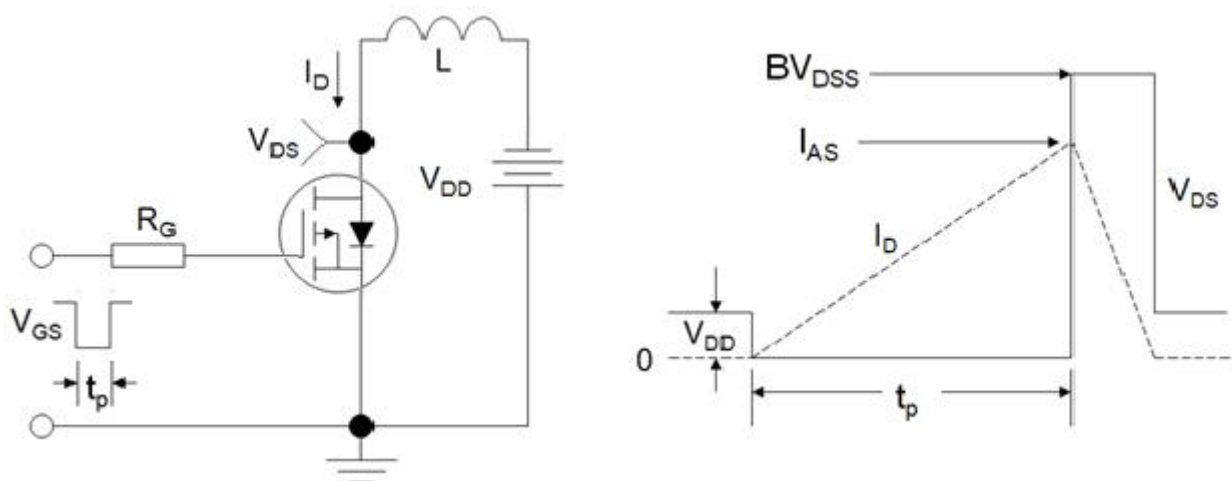
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

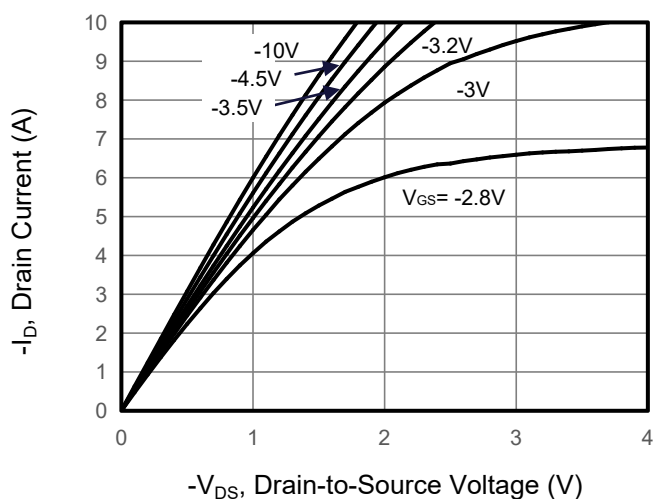


Figure 2. Transfer Characteristics

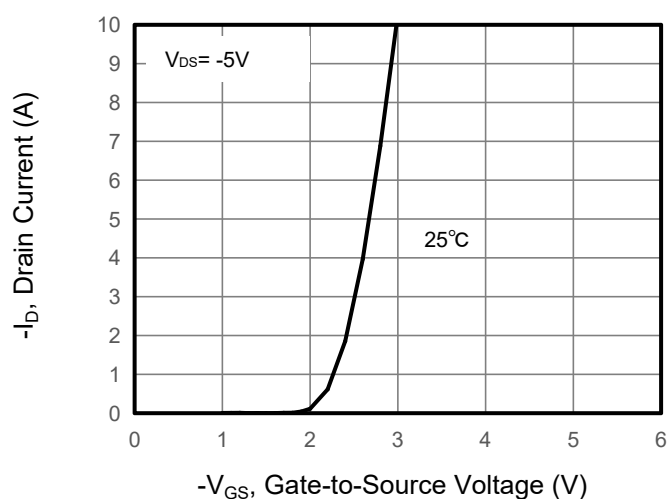


Figure 3. Drain Source On Resistance

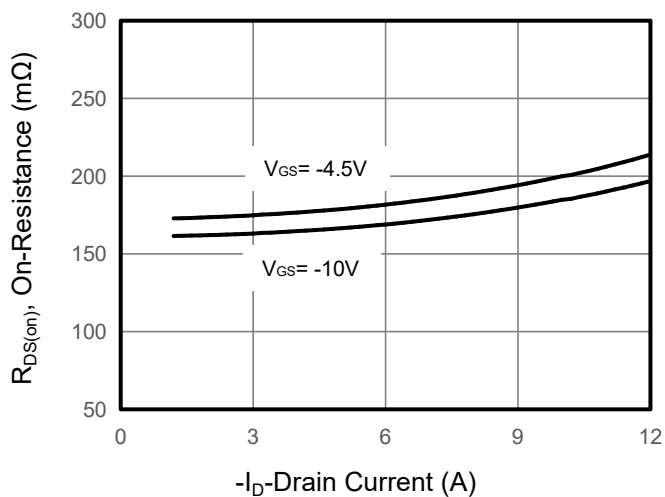


Figure 4. Gate Charge

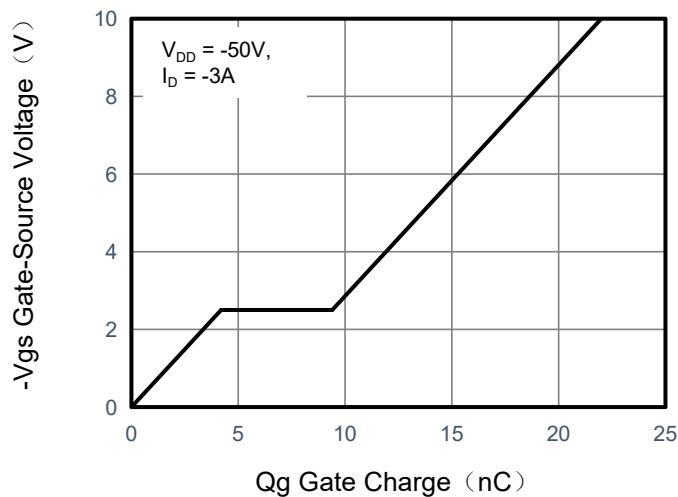


Figure 5. Capacitance

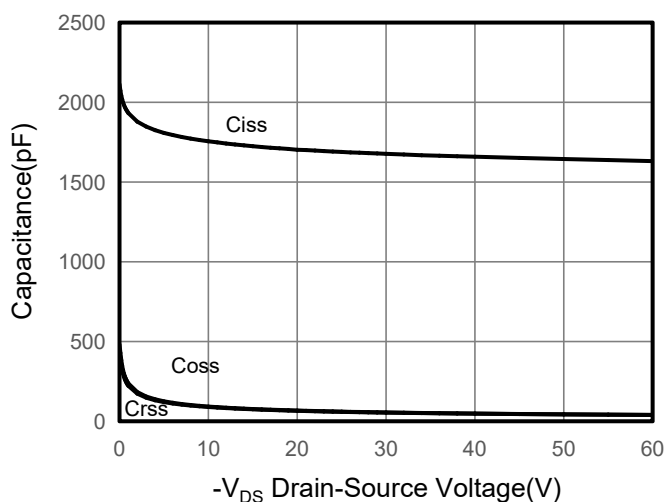
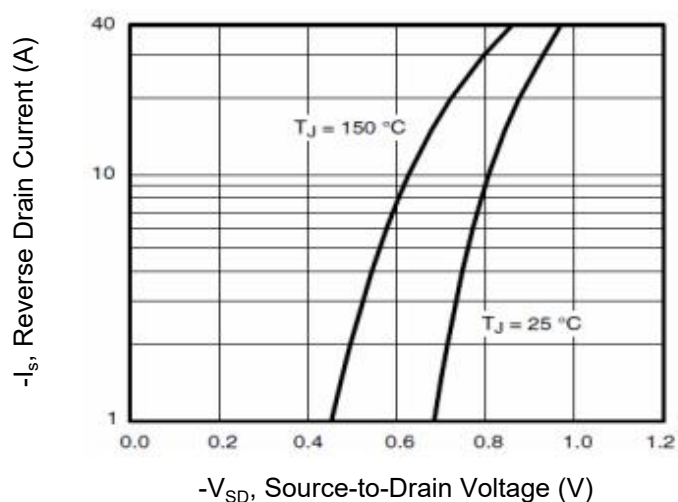


Figure 6. Source-Drain Diode Forward



Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

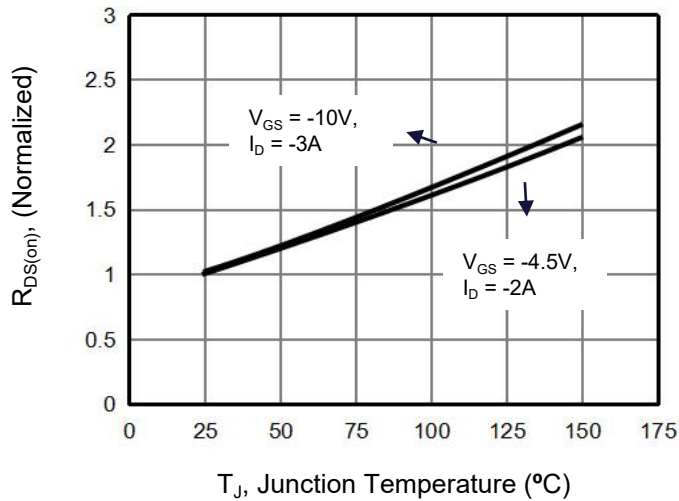


Figure 10. Safe Operation Area

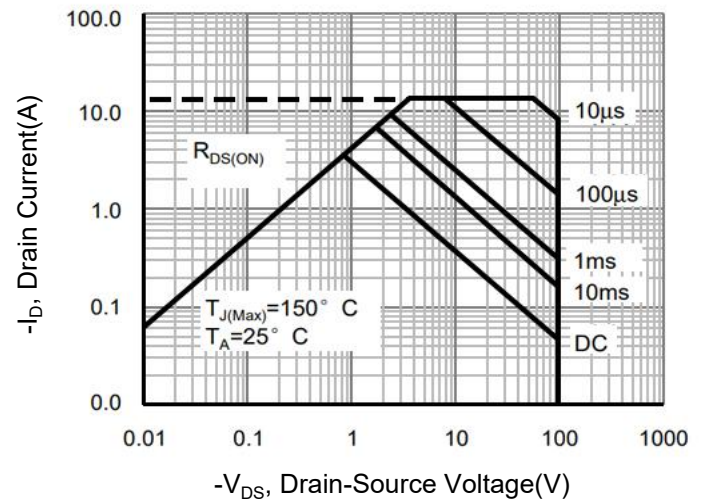
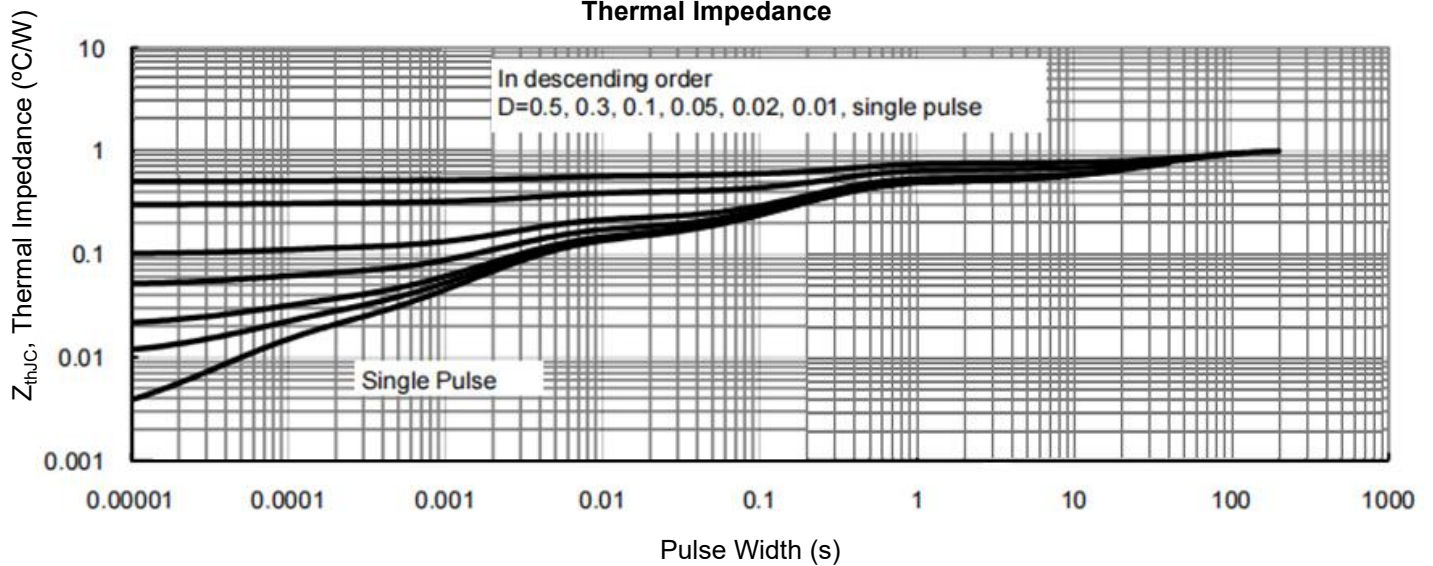
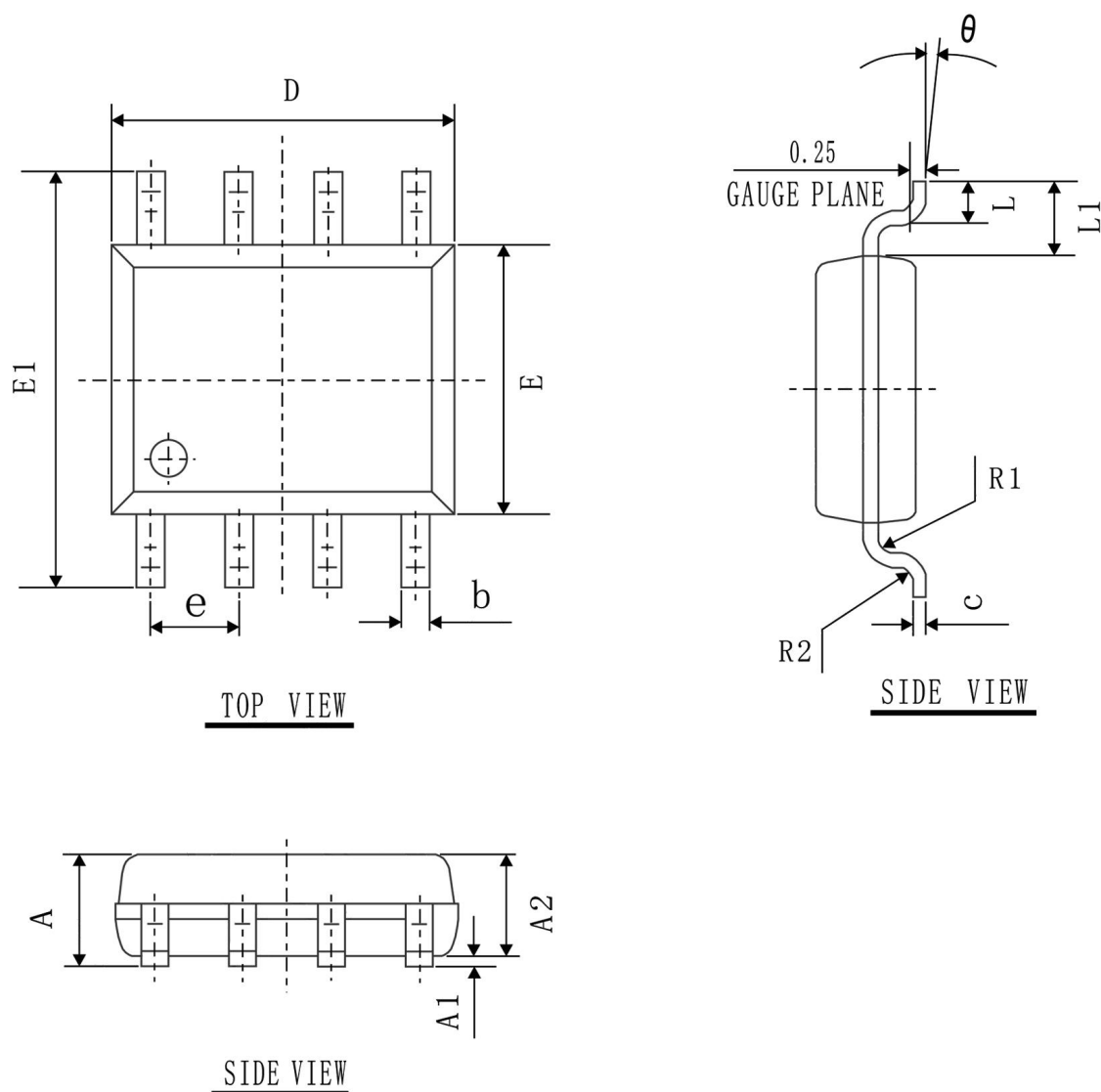


Figure 9. Normalized Maximum Transient Thermal Impedance



SOP-8 Dual Package Information



SYMBOL	MIN	NOM	MAX
A	1.40	1.60	1.80
A1	0.05	0.15	0.25
A2	1.35	1.45	1.55
b	0.30	0.40	0.50
c	0.153	0.203	0.253
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
L	0.45	0.70	1.00
θ	2°	4°	6°
L 1	1.04 REF		
e	1.27 BSC		
R1	0.07 TYP		
R2	0.07 TYP		