Dual P-Channel Enhancement Mode Power MOSFET

Description

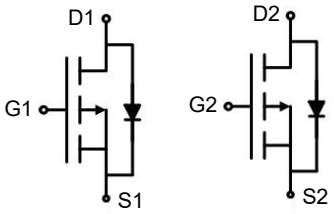
The G4953S uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

General Features

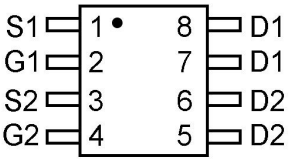
- V_{DS} -30V
- I_D (at V_{GS} = -10V) -5A
- $R_{DS(ON)}$ (at V_{GS} = -10V) < 45mΩ
- $R_{DS(ON)}$ (at V_{GS} = -4.5V) < 65mΩ
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



pin assignment

SOP-8 Dual

Ordering Information

Device	Package	Marking	Packaging
G4953S	SOP-8 Dual	G4953	4000pcs/Reel

Absolute Maximum Ratings T_C = 25ºC, unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	V
Continuous Drain Current	I_D	-5	A
Pulsed Drain Current (note1)	I_{DM}	-20	A
Gate-Source Voltage	V_{GS}	±20	V
Power Dissipation	P_D	1.6	W
Single pulse avalanche energy （note2）	E_{AS}	12	mJ
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	ºC

Thermal Resistance

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	78	ºC/W

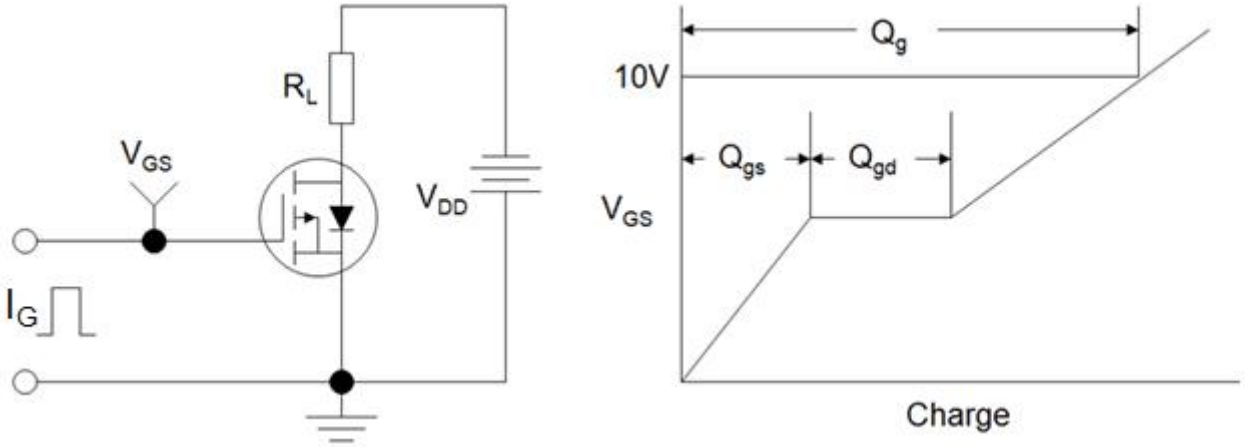
Specifications T_J = 25ºC, unless otherwise noted

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0V, I_D = -250μA	-30	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -30V, V_{GS} = 0V	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	V_{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250μA	-1	-1.4	-3	V
Drain-Source On-Resistance	$R_{DS(on)}$	V_{GS} = -10V, I_D = -5A	--	37	45	mΩ
		V_{GS} = -4.5V, I_D = -4A	--	52	65	
Forward Transconductance	g_{FS}	V_{DS} = -5V,I_D = -5A	--	6.2	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{GS} = 0V, V_{DS} = -15V, f = 1.0MHz	--	592	--	pF
Output Capacitance	C_{oss}		--	76	--	
Reverse Transfer Capacitance	C_{rss}		--	66	--	
Total Gate Charge	Q_g	V_{DD} = -15V, I_D = -5A, V_{GS} = -10V	--	11	--	nC
Gate-Source Charge	Q_{gs}		--	2	--	
Gate-Drain Charge	Q_{gd}		--	3	--	
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = -15V, I_D = -5A, R_G = 3Ω	--	13	--	ns
Turn-on Rise Time	t_r		--	7	--	
Turn-off Delay Time	$t_{d(off)}$		--	14	--	
Turn-off Fall Time	t_f		--	9	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	T_C = 25ºC	--	--	-5	A
Body Diode Voltage	V_{SD}	T_J = 25ºC, I_{SD} = -5A, V_{GS} = 0V	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	I_F = -5A, V_{GS} = 0V di/dt=-100A/us	--	5.3	--	nC
Reverse Recovery Time	T_{rr}		--	11	--	ns

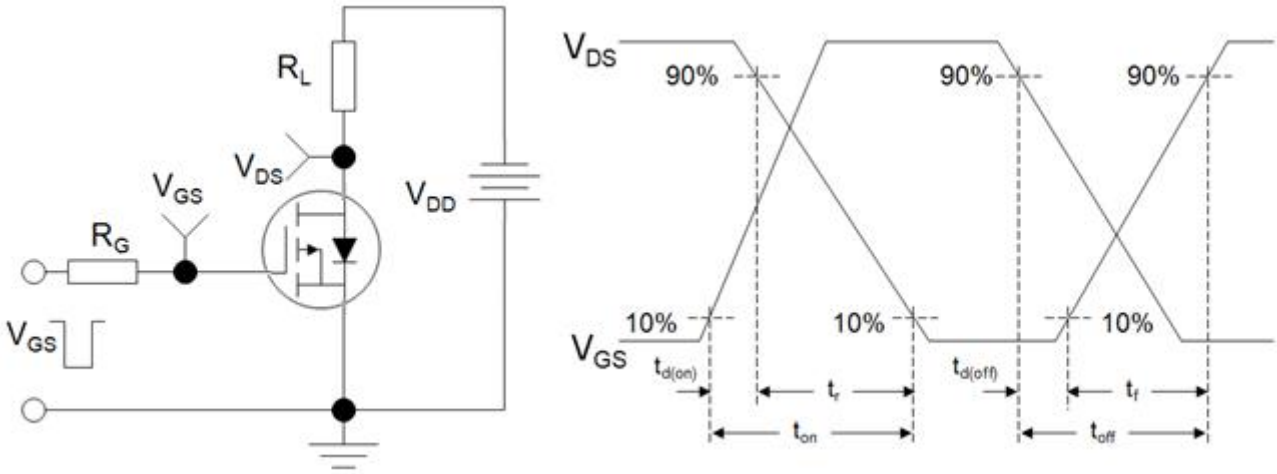
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. EAS condition : Tj=25℃ ,VDD=-30V,VGS=-10V,L=0.5mH,Rg=25Ω
3. Identical low side and high side switch with identical R_G

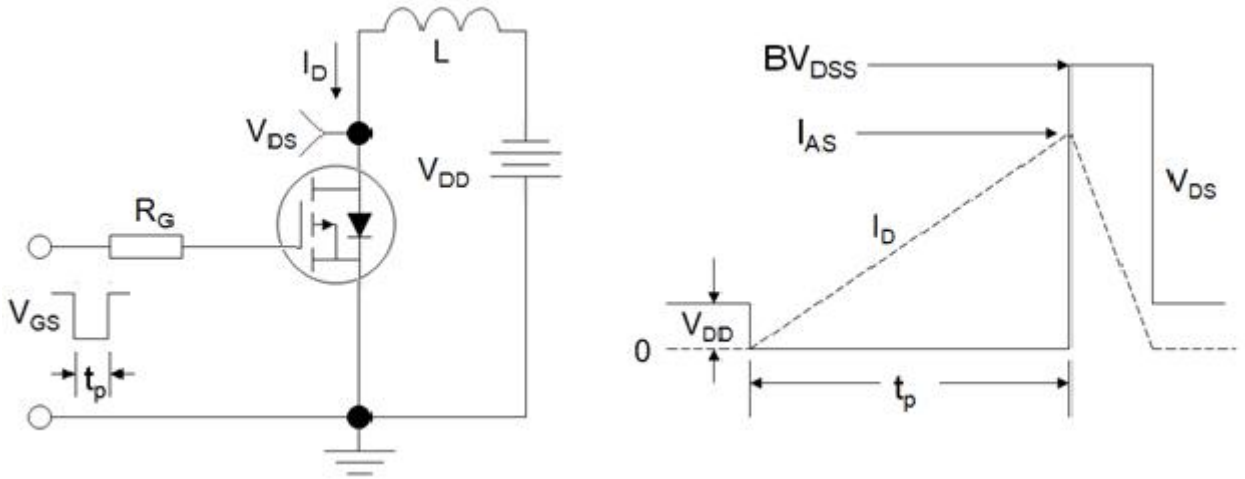
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 1. Output Characteristics

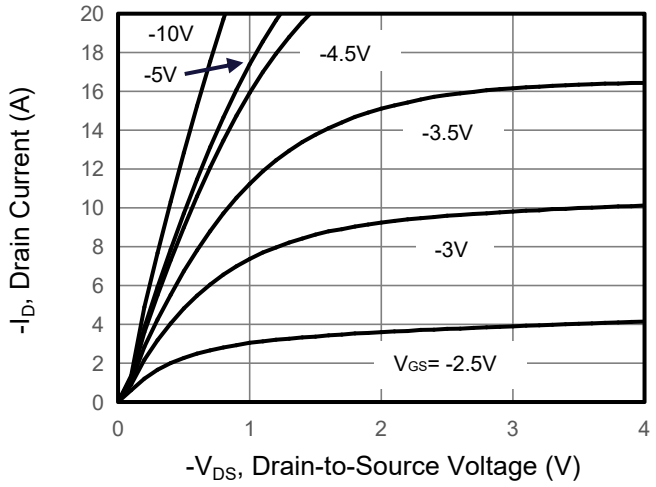


Figure 2. Transfer Characteristics

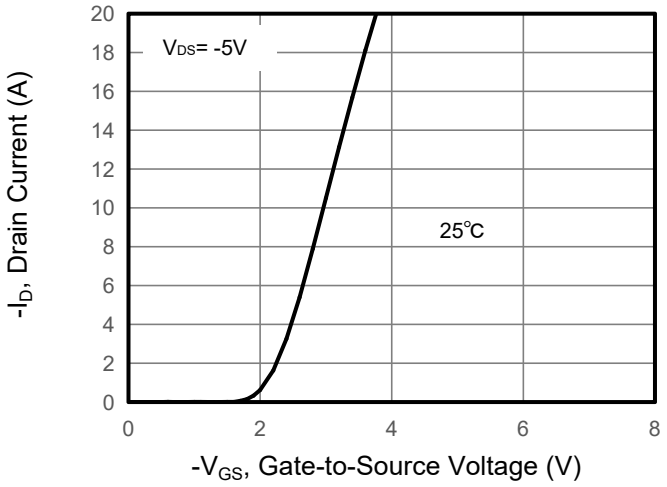


Figure 3.Drain Source On Resistance

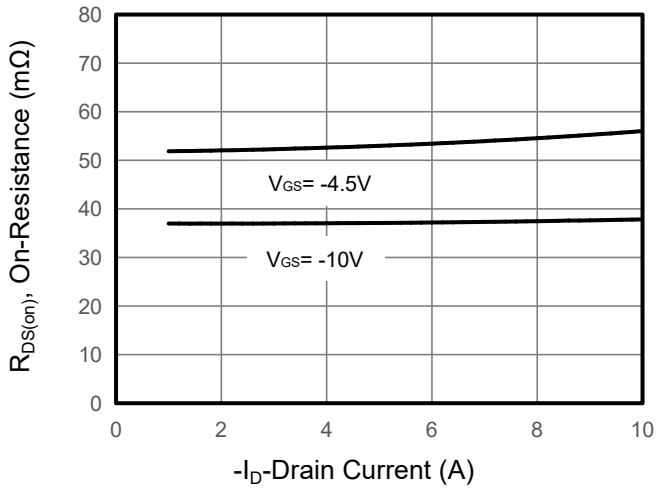


Figure 4. Gate Charge

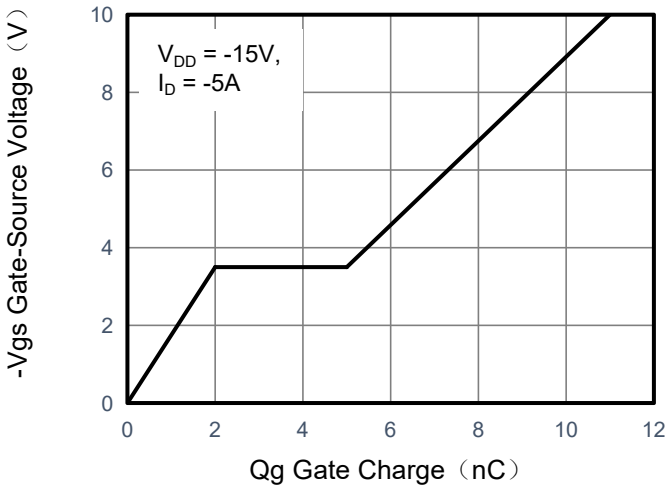


Figure 5. Capacitance

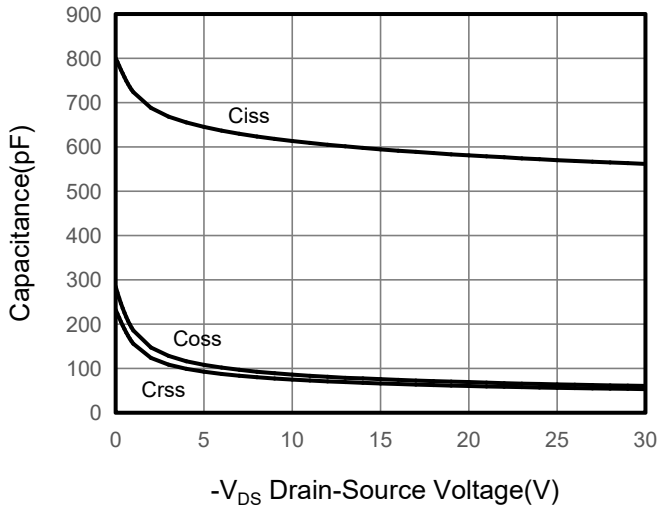
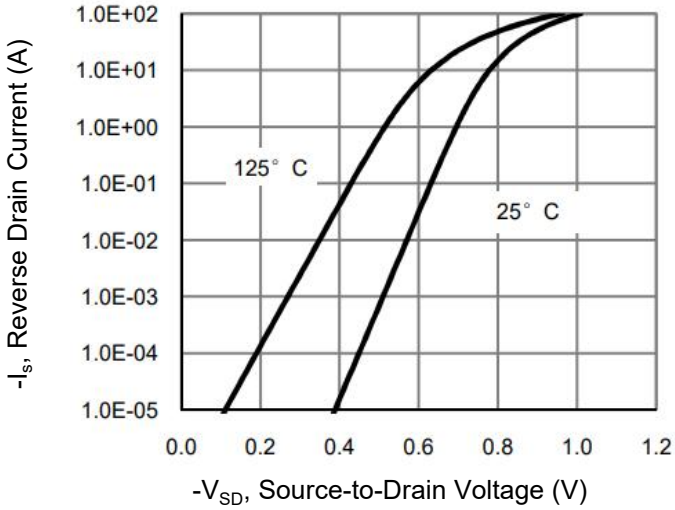


Figure 6. Source-Drain Diode Forward



Typical Characteristics T_J = 25ºC, unless otherwise noted

Figure 7. Drain-Source On-Resistance

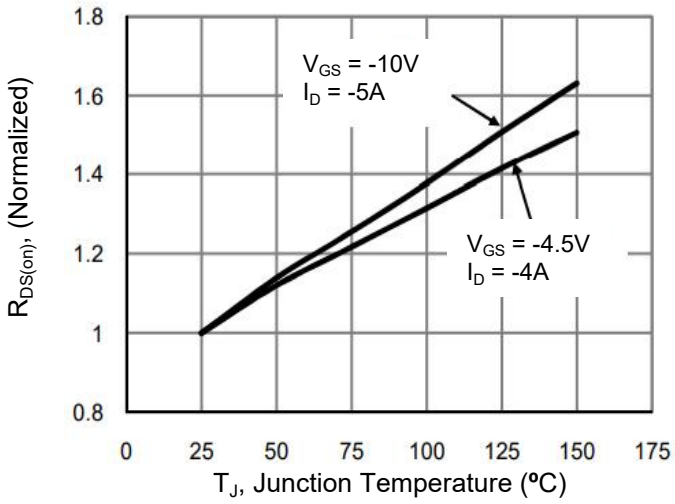


Figure 10. Safe Operation Area

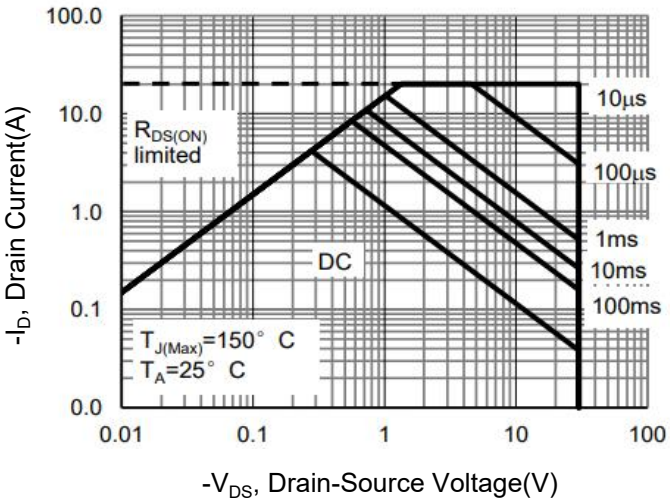
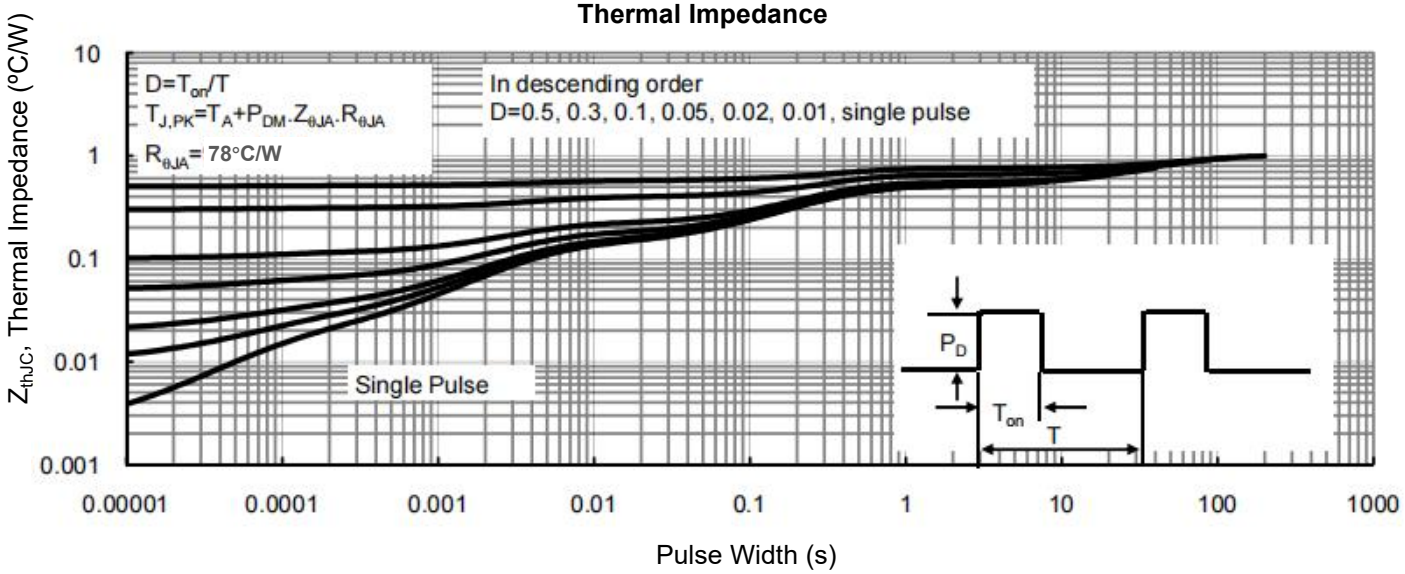
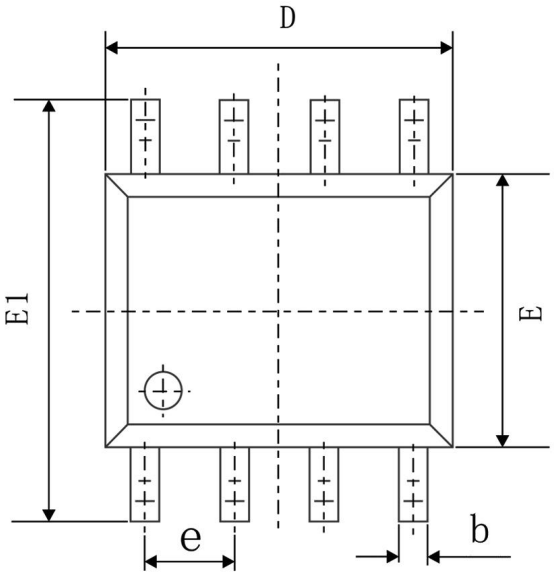


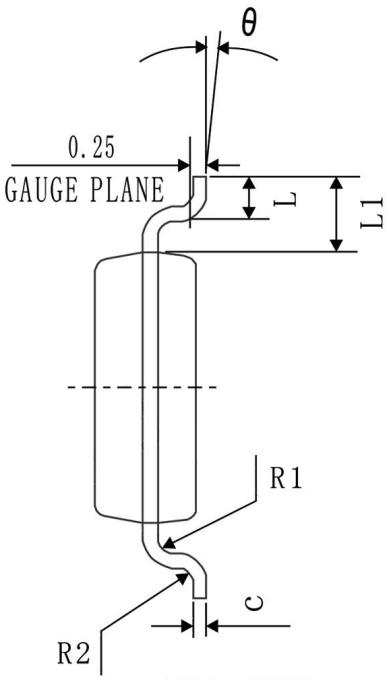
Figure 9. Normalized Maximum Transient Thermal Impedance



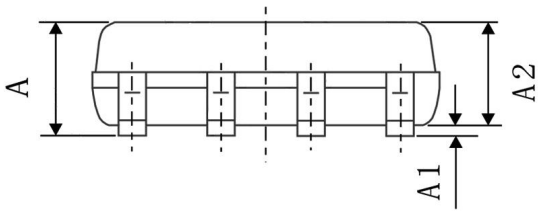
SOP-8 Dual Package Information



TOP VIEW



SIDE VIEW



SIDE VIEW

SYMBOL	MIN	NOM	MAX
A	1.40	1.60	1.80
A1	0.05	0.15	0.25
A2	1.35	1.45	1.55
b	0.30	0.40	0.50
c	0.153	0.203	0.253
D	4.80	4.90	5.00
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
L	0.45	0.70	1.00
θ	2°	4°	6°
L1	1.04 REF		
e	1.27 BSC		
R1	0.07 TYP		
R2	0.07 TYP		