MICRONAS

Hardware
Documentation

Data Sheet

HVC 4x Family

Motor Drivers for Control of BLDC, BDC, or Stepper Motors

Smart|HVC Technology

easy|LIN® Technology

ARM Powered®

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Motor Drivers for Control of BLDC, BDC, or Stepper Motors

Release Note: Revision bars indicate significant changes compared to the HVC 4222F-D2 Data Sheet.

1. Introduction

The HVC 4x family contains a group of highly integrated, intelligent embedded BLDC motor and stepper motor drivers for direct 12V-battery operation with six integrated half-bridges. All modules to directly drive PMSM, BLDC, or stepper motors are on chip. The CPU is a 32-bit Arm® Cortex®-M3 with 1.25 DMIPS/MHz including a Nested Vectored Interrupt Controller (NVIC). The Integrated Circuit (IC) features a debug interface, timers/counters, capture compare units, a multichannel A/D converter with integrated programmable gain amplifier, an advanced LIN-UART with a LIN 2.x compliant physical layer, linear temperature sensors, Back Electromotive Force Comparators (BEMFC), and PWM-controlled motor output (MOUT) ports with diagnostic functions for Permanent Magnet Synchronous Motors (PMSM), Brushless Direct Current (BLDC) motors, brush-type DC (BDC) motors or bipolar- and 3-phase stepper motor control. The computation capacity supports complex motor control algorithms such as Space Vector Modulation (SVM) for PMSMs. The hardware supports voltage controlled or current regulated bipolar stepper motor control for full-stepping, half-stepping and micro-stepping mode.

The integrated digital and analog features reduce the number of necessary external components to a minimum. Different operating modes make it possible to minimize the current consumption according to the system needs.

The HVC 4x family features a flash program memory with a size of 32 KB or 64 KB, providing high flexibility in code development, production ramp-up, and in-system re-programmability. The 64 KB version contains an MPU for memory protection. Grade 1 and grade 1^+ versions exist. Grade 1^+ indicates an extended operating temperature range for high-temperature applications up to 160 °C junction.

Table 1–1: Ordering Information

Part Number	Flash	SRAM	Junction Temperature	Special Features
HVC 4223F-D2	32 K	2 K	Grade 1	
HVC 4222F-D2	32 K	2 K	Grade 1^+	
HVC 4420F-B1	64 K	4 K	Grade 1	Memory Protection Unit
HVC 4422F-B1	64 K	4 K	Grade 1^+	Memory Protection Unit

1.1. Features

The following list gives an overview of the features of the HVC 4x family (see Table 1–2 on page 11 for a detailed feature list).

Core and Interrupt System

- CPU: Arm® Cortex®-M3 core with on-chip serial-wire debug interface (Memory Protection Unit MPU for the 64 KB version)
- Nested Vectored Interrupt Controller (NVIC): over 20 interrupt lines, each programmable with 8 (3-bit) priority levels.
- 24-bit SysTick timer
- CPU operating modes: ACTIVE, OVERVOLTAGE
- Power-saving modes (CPU inactive): IDLE, SLEEP
- Retention mode for start-stop applications: RETENTION
- Programmable CPU clock of up to 20 MHz

Internal Oscillators:

- Main oscillator: 40 MHz with clock divider and EMI reduction
- Auxiliary oscillator: 35 kHz

Memory

- RAM: 2/4 KB
- Flash: 32/64 KB
- NVRAM: 512 byte (448 byte for customer use)

Functional Safety[1)]

- For the HVC 4x family there is additional information available how to use the diagnostic and safety features of the IC on top of the standard AEC-Q100 requirements. This functional safety readiness results in additional documentation like FMEDA summary report and a dedicated Functional Safety Manual.
- The Functional Safety Manual describes, how to implement the Application Software and Application itself in order to correctly and beneficially utilize the regarding device features. The Functional Safety Manual provides information to support customers to realize an ISO 26262 compliant system using the HVC 4x family as a QM hardware part inside functional safety applications.
- The FMEDA summary report describes the assumed Safety Goal, the corresponding Failure Modes as well as the base failure rates according to IEC TR 62380.

[1)] The HVC family members are developed as QM part with respect to ISO 26262.

Advanced Motor Control

– One enhanced PWM (EPWM) module with 12-bit resolution and six outputs to control either a BLDC motor with six half-bridges (B6 configuration) or a bipolar stepper motor with four half-bridges. The module supports center- and edge-aligned mode with automatic dead-time insertion.

– Three high-voltage Back Electromotive Force Comparators (BEMFC) are supporting zero crossing detection for sensorless BLDC motor control with integrated virtual star point reference. Furthermore, the three comparators can be used for closed-loop current control with bipolar stepper motors or alternatively for BEMF voltage measurements with stepper motor for commutation and / or stall detection.

– Integrated phase current measurement for bipolar stepper motor control with closed-loop current control.

– Two 8-bit DACs used as reference for current limitation (CLDAC) for bipolar stepper motors in closed-loop current control.

– One 12-bit ADC with HW trigger option:
Five external inputs (four single ended and one differential) + V_{BVDD} + V_{MON} + linear temperature sensor + input for motor current sensing + inputs for stepper motor stall detection + inputs for LIN Auto-Addressing (BSM).

– ADC reference: internal band-gap reference

– One integrated Programmable Gain Amplifier (PGA) as part of the ADC signal path.

High-Current Drivers and Phase Sensing

– MOUT ports:
Six half-bridges with integrated charge pump for motor control, connected each to one MOUT port. Bridge configuration for either BLDC motor, BDC motor(s), or bipolar stepper motor by connecting the MOUT ports accordingly.

– MVSS0 and MVSS1 pins to connect an external shunt resistor to ground for current measurement e.g. in BLDC motor control applications.

– Integrated bridge current measurement for bipolar stepper motor closed-loop current control and overcurrent detection.

– Phase voltage sensing via the integrated BEMF comparators (BEMFC).

MOUT (Motor Output) Ports – Protection and Diagnosis

– Power-bridge open load detection with BEMFCs.

– Power-bridge overcurrent protection: The concerned half-bridge or all six half-bridges are automatically switched off in an overcurrent condition.

Other Analog Peripherals

– HSBVDD port:
High-side switch to battery supply (BVDD) with overcurrent protection for power supply of external devices (e.g. Hall sensors).

– Thermal shutdown at overtemperature.

– Supply supervision: undervoltage reset, V_{BAT} and BVDD under/overvoltage supervision with alarm interrupt.

– Voltage supervision possible by software up to load dump voltage (application SW has to limit the power consumption with respect to the limits of the thermal budget).

– Start-stop applications supported by RETENTION mode.

– Two overtemperature detection units (placed close to power-bridge).

– One linear temperature sensor readable by the ADC.

– One overtemperature detection unit for return from overtemperature shutdown.

Input and Output

– Low-voltage General-Purpose I/O (LGPIO) ports:
General purpose I/O ports with 3.2 V digital I/O (digital input: floating, weak pull-up or pull-down, digital output: push-pull or open drain) and analog input function.

– LIN 2.x physical layer interfaces (pins LIN, LIN_O). Including hardware provisions to support LIN Auto-Addressing.

Communication

– LIN telegram supporting UART with automatic baud rate adjustment and receive/ transmit FIFOs, usable for LIN slave operation.

– Synchronous Serial Peripheral Interface (SPI), master mode only.

– Special PWM module (PWMIO), e.g. for customer specific bus communication. The module can be accessed either via LGPIO alternative functions or the LIN pin. If LGPIO ports shall be used the ESD-protection and open-drain architecture must be applied by external components.

Timers and Counters

– One Capture Compare (CAPCOM) unit with three channels and one 16-bit free-running counter.

– Two 16-bit timer modules: usable as timer, counter, input capture, or PWM output.

Miscellaneous

– Digital watchdog clocked with the system clock f_{SYS}.

– Window watchdog and wake-up timer clocked with the auxiliary oscillator clock f_{AUX}.

– Power supply voltage (V_{BVDD}):
  - Nominal: 8 V to 18 V
  - With degraded analog parameters from 5.4 V to 8 V. From 18 V to 40 V with limited BVDD current according to thermal power budget boundaries.
  - Support of jump-start and load-dump requirements.

– 5 V LDO pre-regulator with support of start-stop applications.

– RAM data retention to support crank-pulse / start-stop applications.

– Automotive AEC-Q100 Grade 1 qualified

– Extended junction temperature range: –40 °C to 160 °C

LIN Auto-Addressing Support

– In applications where LIN Auto-Addressing is required, either by a need for plug&play or “off-the-shelf” requirements, the HVC can support by a dedicated IP set. With minimized additional software effort, a LIN slaves’ node address is automatically determined. This helps reducing additional cost for mechanical- or application-related implementations.

– To utilize device with LIN Auto-Addressing enabled, a dedicated license fee has to be agreed with TDK-Micronas

– An agreement results in a dedicated hardware version where LIN Auto-Addressing is enabled.

– Please contact your local sales support for additional information.

Table 1–2: HVC 4x family feature list

Item	HVC 4x family with integrated motor bridges	
Core and Interrupt System		
CPU	Arm® Cortex®-M3	
	Memory Protection Unit for 64 KB flash version	
CPU active operation mode	ACTIVE, OVERVOLTAGE	
CPU power saving modes	IDLE, SLEEP	
Retention mode to support start-stop applications	RETENTION	
CPU clock (f_{CPU})	Up to 20 MHz	
Interrupt Controller	HVC 422xF	NVIC with 22 interrupt lines, 8 priority levels
	HVC 442xF	NVIC with 23 interrupt lines, 8 priority levels
EMI reduction module	Selectable in CPU ACTIVE operating modes	
Integrated Oscillators	40 MHz main oscillator with clock divider 35 kHz auxiliary oscillator	
Memory		
RAM	HVC 422xF	2 KB
	HVC 442xF	4 KB
Flash / ROM	HVC 422xF	32 KB flash
	HVC 442xF	64 KB flash
Startup ROM	1 KB (includes utility routines for flash erase and program)	
NVRAM[1)]	512 byte (448 byte for customer use)	
Advanced Motor Control		
Enhanced PWM module with up to six outputs and up to 12-bit resolution to control either a B6 bridge configuration for BLDC motor or a four half-bridge configuration for bipolar stepper motor control. The module supports center- and edge-aligned mode with automatic dead-time insertion	1	
High-voltage Back Electromotive Force Comparator (BEMFC) for diagnostics, BEMF zero crossing detection and closed-loop current control	3	
BEMF comparator reference	Integrated virtual star point resistor network or Current Limit DAC (CLDAC).	
Motion feedback for sensored rotor position detection	E.g. via Hall sensor switches connected to LGPIO ports.	
One 12-bit ADC with Programmable Gain Amplifier (PGA) and HW trigger option	Inputs for V_{BAT} + V_{BVDD} + linear temperature sensor + input for motor current shunt voltage sensing + differential inputs for stepper motor stall detection + LIN current sense + four LGPIO ports single-ended input + 2 LGPIO ports for differential input[3)] + LIN auto-addressing (according to bus-shunt method)	
ADC reference	Internal (band gap)	
Resistor network serving as virtual star-point reference to the BEMF comparator	1	
Protection and Diagnosis		
MOUT overcurrent protection	Yes	
Overtemperature protection	Yes	
V_{BVDD} overvoltage detection	Yes	
Differential port for motor current shunt measurement	Yes	
Phase current sensing	BLDC motor control: with external shunt connected to MVSS0 and MVSS1 Stepper motor control: integrated current measurement	

Table 1–2: HVC 4x family feature list**, continued**

Item	HVC 4x family with integrated motor bridges	
Integrated High-Current Drivers		
Integrated charge pump with charge pump capacitor pin VCP	Yes	
MOUT ports	Six fully integrated half-bridges. Configurable by external connection of MOUTx pins for BLDC, BDC or bipolar stepper motor control.	
Other Analog Peripherals		
HSBVDD port: High-side switch to battery supply (BVDD) with overcurrent protection for power supply of external devices (e.g. hall sensors)	Yes	
Overtemperature supervision for Thermal Shutdown (TSD) with two overtemperature detection (OTD) units	Yes	
Overtemperature detection unit for return from TSD	Yes	
Linear temperature sensor readable by ADC	1	
Supply supervision: undervoltage reset, V_{BAT} over-/undervoltage alarm interrupts. Voltage supervision possible by software beyond 18V with limited BVDD supply current according to thermal budget limitations.	Yes	
Communication		
LIN-UART with automatic baud rate adjustment and receive/transmit FIFOs	1	
SPI module	1	
PWMIO module	1	
Input and Output		
LGPIO ports (general purpose I/O) with 3.2 V digital I/O (push-pull or open drain mode).	11 ports One LGPIO port pair usable as 3.2 V differential analog input.[2)] Four ports usable as 3.2 V single-ended analog input.	
LIN 2.x physical layer interfaces (LIN, LIN_O). Including support of LIN Auto-Addressing.	1 Alternatively usable as PWM communication interface with PWMIO module.	
Timers and Counters		
24-bit SysTick timer	1	
CAPCOM unit with three channels and 16-bit free running counter	1	
16-bit timers usable as timer, counter, capture input, output compare or PWM output	2	
Miscellaneous		
Digital watchdog clocked with the system clock f_{SYS}	Yes	
Window watchdog and wake-up timer clocked with the auxiliary oscillator clock (f_{AUX})	Yes	
5V LDO pre-regulator	Yes, can be used to drive external 5V loads at SMPSI pin	
Support of start-stop function (RETENTION mode)	Yes	
Package	PQFN6x6, 40 pins	
T_J temperature range	HVC 4223F and HVC 4420F	$-40\ °C \le T_J \le 150\ °C$
	HVC 4x22F	$-40\ °C \le T_J \le 160\ °C$

[1)] NVRAM is a non-volatile memory which is used to store non-volatile application data and to configure basic functions of the system, like operating status of digital and window watchdogs after reset, etc.

[2)] The differential input LGPIO8/9 is not calibrated and has only limited accuracy.

1.2. Top Level / Block Diagrams

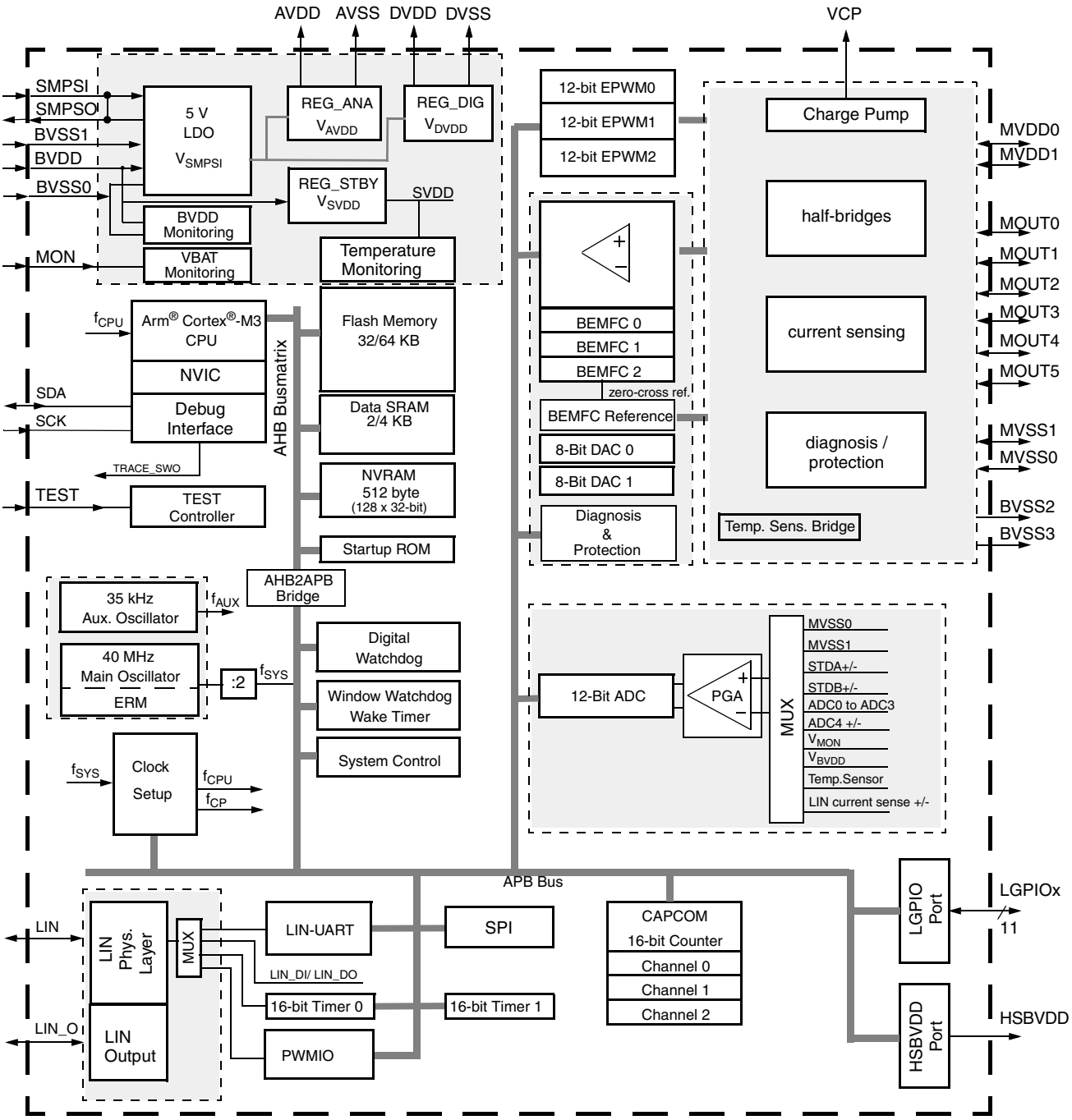
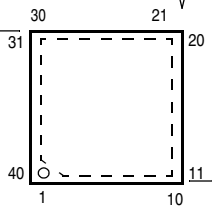


Fig. 1–1: Block diagram of the HVC 4x family

2. Package and Pins

2.1. Pin Assignment

Pin Name	Pin No.
LGPIO4	21
LGPIO5	22
LGPIO6	23
LGPIO7	24
LGPIO8	25
LGPIO9	26
LGPIO10	27
MOUT5	28
MOUT3	29
MVSS1	30
MOUT2	31
MVDD1	32
BVSS3	33
VCP	34
LIN	35
BVSS0	36
LIN_O	37
BVSS2	38
MVDD0	39
MOUT0	40



Pin No.	Pin Name
20	SDA
19	SCK
18	LGPIO3
17	LGPIO2
16	LGPIO1
15	LGPIO0
14	AVDD
13	AVSS
12	DVSS
11	DVDD
10	TEST
9	SMPSI
8	SMPSO
7	BVSS1
6	BVDD
5	MON
4	HSBVDD
3	MOUT4
2	MOUT1
1	MVSS0

Fig. 2–1: Pin assignment of the HVC 4x family in PQFN40 package.

2.2. Pin List

Table 2–1 shows the primary functions of the pins of the HVC 4x family.
Refer to Table 2–2 for the alternative functions assigned to the I/O pins.

Table 2–1: Pin description

Name	Type[1)]	Module / Function[2)]
Power Supply Pins		
BVDD	P	Positive power supply (14 V nominal)
BVSS0	P	Battery ground
BVSS1	P	Internally connected to EPAD. Must be connected to BVSS0
BVSS2	P	Must be connected to BVSS0
BVSS3	P	Must be connected to BVSS0
AVDD	P	Output of the internal AVDD regulator (must be buffered by an external capacitor to AVSS)
AVSS	P	Analog ground
SMPSI	P	Internally connected to SMPSO (must be buffered by an external capacitor to BVSS1)
SMPSO	P	Output of 5 V LDO. Pin is internally connected to pin SMPSI and therefore can be left open. For compatibility reasons with HVC 4223F Bx, this pin may also be externally shorted to SMPSI.
DVDD	P	Output of the internal DVDD regulator (must be buffered by an external capacitor to DVSS)
DVSS	P	Digital ground
Power Supply Pins for Integrated Half-Bridges		
MVDD0	P	Positive power supply of half-bridges. Pins must be shorted with low impedance on the PCB.
MVDD1	P	
MVSS0	P	Common ground of half-bridges; BLDC motor control: Both connected to system ground with one shunt. Stepper motor control: Both connected to system ground. No external shunt necessary.
MVSS1	P	
VCP	P	Output of the internal charge pump (must be buffered by an external capacitor to BVDD)

Table 2–1: Pin description**, continued**

Name	Type[1)]	Module / Function[2)]
Application Pins		
SDA	I/O	Debug interface data (in application mode the pin can be left open due to the internal weak pull-up resistor)
SCK	I	Debug interface clock (in application mode the pin can be left open due to the internal weak pull-down resistor)
MON	I	Supply voltage supervision input. If not used for V_{BAT} supervision, the MON pin shall be connected to BVDD.
LGPIO0 to LGPIO10	I/O	3.2 V digital I/O Input: floating, weak pull-up or weak pull-down Output: push-pull, open-drain The LGPIO ports 0 to 3 can be used as single ended 3.2 V analog input. The ports LGPIO8 and LGPIO9 together as 3.2 V differential analog input [3)]. If not used in the application the pins can be left open. To avoid cross-currents it is recommended to activate the internal weak pull-down resistors for unused LGPIO pins. Alternatively, connect unused pins to GND.
MOUT0 to MOUT5	O	Outputs of the six half-bridges, whereas one MOUTx connects to one half-bridge each (refer to block diagram Fig. 1–1 on page 13)
LIN_O	O	LIN output for LIN Auto-Addressing purpose (together with the LIN pin). If not used, the LIN_O pin can be connected to LIN or left open.
LIN	I/O	LIN transceiver I/O. Alternatively V_{BAT} open drain digital I/O for PWM communication function.
HSBVDD	P	High-side switch to BVDD supply. If not used in the application this pin should be connected to BVDD.
TEST	I	Test pin In application mode it is recommended to connect the pin to GND.
Exposed Pad (chip back-side area for thermal coupling of the device to the PCB)		
-/-	-/-	The exposed pad is directly connected to the substrate at the chip backside. It is recommended to connect the exposed pad to GND.

1) Types are defined as: I = Input, O = Output, P = Power

2) Refer also to Fig. 2–2 on page 22 and Fig. 2–3 on page 23 for the recommended circuitry

3) The differential input LGPIO8/9 is not calibrated and has only limited accuracy.

2.3. Multifunctional Pins

2.3.1. LGPIO Ports

The LGPIO ports (LGPIO0 to LGPIO10) are implemented as low-voltage general-purpose I/Os. Each LGPIO port can be separately configured to operate in one of several input or output modes.

All LGPIO ports are configurable in three different digital input modes (floating, weak pull-up or pull-down) whereas the analog input mode is only available for LGPIO0 to LGPIO3 (single ended analog input) and LGPIO8/9 (differential analog input). In digital input mode the input level of the LGPIO ports is signaled in the data input register of the LGPIO module (LGPIOx.DI) and is in parallel available as input signal for internal digital peripherals (refer to Table 2–2). In analog input mode the input voltage of the according port is routed to the ADC input multiplexer and the corresponding bit in LGPIOx.DI is set to '0'.

All LGPIO ports are configurable in two digital output modes (push-pull or open drain) and additionally the ports can be separately configured to operate in normal output mode or alternative output mode. In normal output mode the level of the LGPIO ports is defined by the data output register of the LGPIO module (LGPIOx.DO). In alternative output mode the level of the LGPIO ports is driven by output signals generated from internal digital peripherals. For each LGPIO port there are two alternative output signals available. Table 2–2 shows the functions which can be assigned to the LGPIO pins.

Table 2–2: LGPIO pin function assignments

Pin Name	Pin Function LGPIO					Analog Input
	Normal Input	Normal Output	Alternative Output#0	Alternative Output#1	Alternative Inputs	
3.2 V digital input (floating, pull-up or pull-down), 3.2 V digital output (push-pull or open drain), 3.2 V analog input						
LGPIO0	LGPIO0.DI	LGPIO0.DO	CAPCOM0_OUT	TIMER0_OUT	CAPCOM0_IN[1)], TIMER0_IN	ADC0
LGPIO1	LGPIO1.DI	LGPIO1.DO	CAPCOM1_OUT	TIMER1_OUT	CAPCOM1_IN[1)], TIMER1_IN	ADC1
LGPIO2	LGPIO2.DI	LGPIO2.DO	CAPCOM2_OUT	TRACE_SWO	CAPCOM2_IN[1)]	ADC2
LGPIO3	LGPIO3.DI	LGPIO3.DO	TIMER0_OUT	TRACE_SWO	TIMER0_IN[1)], LINUART_RX	ADC3
LGPIO4	LGPIO4.DI	LGPIO4.DO	TIMER1_OUT	LINUART_TX	TIMER1_IN[1)], SPI_MISO[1)]	-
LGPIO5	LGPIO5.DI	LGPIO5.DO	TRACE_SWO	CAPCOM0_OUT	PWMIO_IN[1)], CAPCOM0_IN	-
LGPIO6	LGPIO6.DI	LGPIO6.DO	PWMIO_OUT	CAPCOM1_OUT	CAPCOM1_IN	-
LGPIO7	LGPIO7.DI	LGPIO7.DO	SPI_CSN	CAPCOM2_OUT	CAPCOM2_IN	-
LGPIO8	LGPIO8.DI	LGPIO8.DO	SPI_SCK	TRACE_SWO	-	ADC4+
LGPIO9	LGPIO9.DI	LGPIO9.DO	SPI_MOSI	TRACE_SWO	PWMIO_IN, LINUART_RX[1)]	ADC4-
LGPIO10	LGPIO10.DI	LGPIO10.DO	LINUART_TX	PWMIO_OUT	SPI_MISO	-

[1)] Selectable by MUX setting for Alternative Input Select (LGPIO_AIS).

2.3.2. LIN I/O

The LIN port is mainly used to drive the output via the physical LIN 2.x interface for the communication via the LIN bus. In addition to the LIN I/O function of the port, alternative output or input functions can be assigned according to Table 2–3 on page 18.

An incoming LIN message can be used as wake signal for the system in the power-saving modes (IDLE and SLEEP).

Table 2–3: LIN I/O function assignment

Pin Name	Pin Function LIN I/O					
	Normal Input	**Normal Output**	**Alternative Output#0**	**Alternative Output#1**	**Alternative Output#2**	**Alternative Input**
LIN Transceiver I/O						
LIN [1) 2)]	LINUART_RX	LINUART_TX	PWMIO_OUT	TIMER0_OUT	LIN_DO	PWMIO_IN, LIN_DI
LIN_O	For slave node position detection together with LIN pin. Connected internally via series resistor to LIN port.					

[1)] The LIN pin can be alternatively used for PWM communication with the PWMIO module (selectable by MUX setting).
[2)] The LIN can be used as wake-port in the power saving modes (IDLE and SLEEP).

2.3.3. MOUT

The MOUT ports (MOUT0 to MOUT5) are implemented as high-current outputs for direct motor operation. The ports are driven by the integrated power bridges and can be configured either in paired mode (for BLDC motors) or separated mode (for stepper motors).

Table 2–4 shows the functions which can be assigned to the MOUT ports.

Table 2–4: Motor half-bridge outputs

Pin Name	Controlled Transistor	Pin Output Function				Analog I/O	
		BLDC		Stepper		Comparator and Reference	
		EPWM Module	Phase Assignment	EPWM Module	Phase Assignment	BLDC	Stepper
MOUT0	high-side	EPWM_HS(0)	U	EPWM_HS(0)	A1	BEMFC0, integrated star point resistor network.	Integrated phase current measurement. Reference with CLDAC0.
	low-side	EPWM_LS(0)		EPWM_LS(0)			
MOUT1	high-side	EPWM_HS(1)		EPWM_HS(1)	A2		
	low-side	EPWM_LS(1)		EPWM_LS(1)			
MOUT2	high-side	EPWM_HS(2)	V	EPWM_HS(2)	B1	BEMFC1, integrated star point resistor network.	Integrated phase current measurement. Reference with CLDAC1.
	low-side	EPWM_LS(2)		EPWM_LS(2)			
MOUT3	high-side	EPWM_HS(3)		EPWM_HS(3)	B2		
	low-side	EPWM_LS(3)		EPWM_LS(3)			
MOUT4	high-side	EPWM_HS(4)	W	EPWM_HS(4)	Not used	BEMFC2, integrated star point resistor network.	Integrated phase current measurement. Reference input configurable for CLDAC0 or CLDAC1.
	low-side	EPWM_LS(4)		EPWM_LS(4)			
MOUT5	high-side	EPWM_HS(5)		EPWM_HS(5)			
	low-side	EPWM_LS(5)		EPWM_LS(5)			

2.3.4. Alternative Function Description

The table below describes all special function designators used in the tables above.

Table 2–5: Alternative function descriptions

Name	Function
ADCx	Analog input connected to ADC input multiplexer [x: 0 to 4]
BEMFCx	Input of BEMF comparator x [x: 0 to 2]
CAPCOMx_IN	Capture input of the CAPCOM channel x [x: 0 to 2]
CAPCOMx_OUT	Compare output of the CAPCOM channel x [x: 0 to 2]
EPWM_HS(x), EPWM_LS(x)	Enhanced PWM module output according to MOUTx [x: 0 to 5]
LGPIOx.DI	LGPIO port data input register [x: 0 to 10]
LGPIOx.DO	LGPIO port data output register [x: 0 to 10]
LINUART_RX	Receive input line of the LIN-UART
LINUART_TX	Transmit output line of the LIN-UART (connected to LIN port output multiplexer)
LIN_DI	LIN port input register (to LIN transceiver receive input)
LIN_DO	LIN port data output (connected to LIN port output multiplexer)
PWMIO_OUT	Output of the PWMIO module
PWMIO_IN	Input of the PWMIO module
TIMERx_IN	TIMER module x input [x: 0 to 1]
TIMERx_OUT	TIMER module x output [x: 0 to 1]
TRACE_SWO	Trace Data Single Wire Output
SPI_SCK	SPI clock
SPI_MOSI	SPI Master Out Slave In
SPI_MISO	SPI Master In Slave Out
SPI_CSN	SPI Chip Select

2.4. External Components Circuit Diagrams

If using the device in the extended temperature range, the application developer is responsible for verifying the external circuit parameters over production, voltage and temperature variation to fulfill the following requirements:

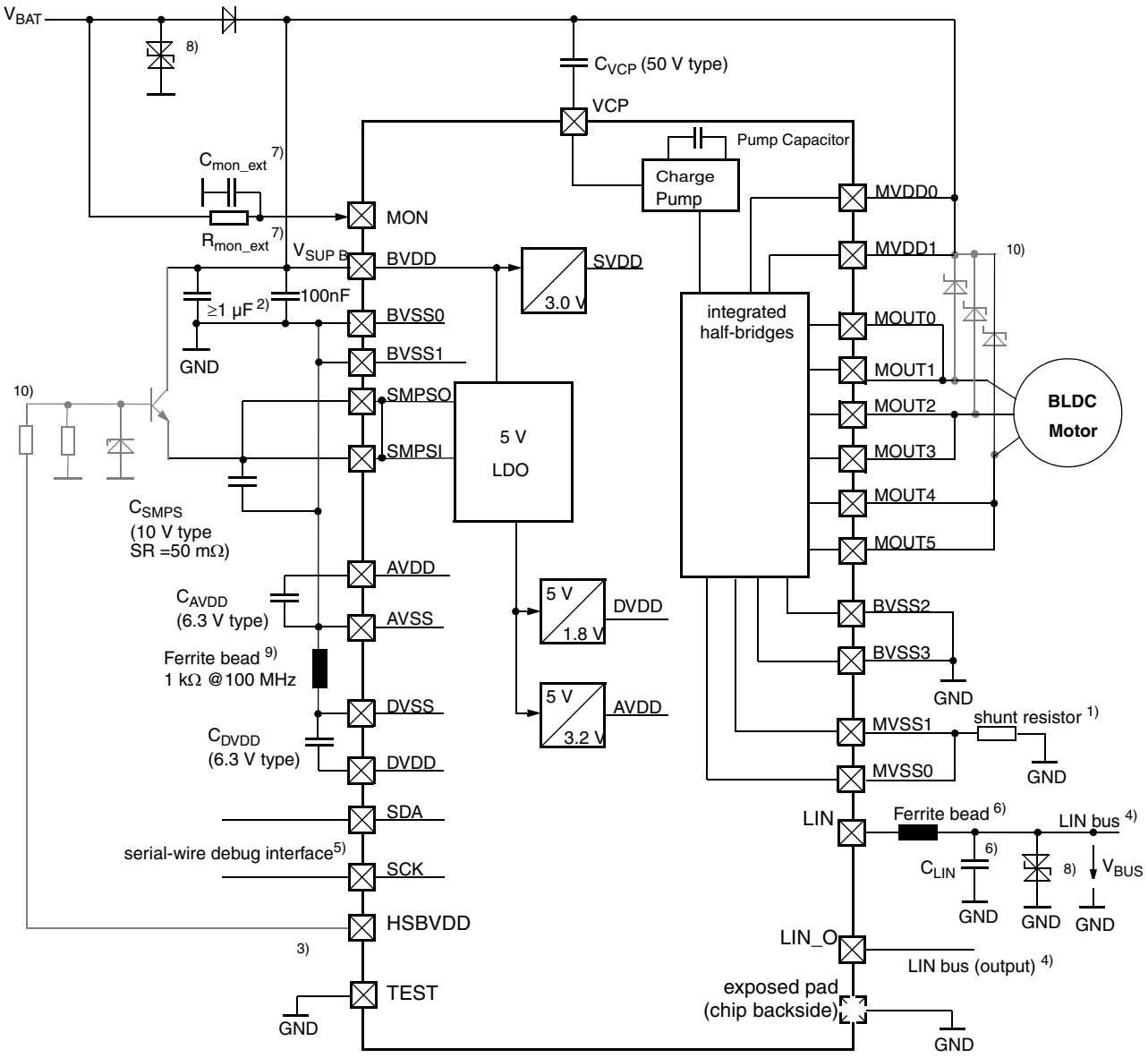
– The V_{SMPSI} voltage must not exceed 7.5 V in order to avoid triggering the ESD protection of the SMPSI pin.

– In order to bypass the internal linear regulator, the V_{SMPSI} voltage should be greater than $V_{SMPSI(max)}$. If the externally supplied voltage on SMPSI is lower than the internal pre-regulator voltage, the bypass is not effective.

– The total output current of the SMPSI pin must be within the specification limits (parameter $I_{out\ total}$).

– The internal 5V regulator at the pin SMPSI must only be bypassed in ACTIVE and OVERVOLTAGE mode and therefore it must be possible to disable the bypass circuit e.g. by the HSBVDD pin. Turning on the HSBVDD port will switch on the external NPN transistor which then overdrives the SMPSI node to reduce the internal current flowing from BVDD to SMPSI. The bypass circuit with NPN transistor (10) in Fig. 2–2 and Fig. 2–3 is one suggestion to bypass the internal regulator. The customer might apply a specific circuit fulfilling the afore mentioned properties. TDK-Micronas shall review the customer schematic to confirm its principle function. The customer must provide simulation and measurement results to confirm its function within the range of the device specification.

2.4.1. External Components Circuit Diagrams for BLDC Motor Control



Notes: All capacitors are ceramic types. Refer to the **"Recommended Operating Conditions"** for the resistor, inductor and capacitor values. Blocking capacitors have to be placed as close as possible to the pins.

1) Choose the shunt resistor value according to the application needs and the limits specified in **"Electrical Data"** section, respectively.

2) Choose the BVDD capacitor value according to the application needs, e.g. if the NVRAM shall be programmed after V_{BVDD} has dropped below the undervoltage interrupt threshold.

3) To control SMPSI pass transistor

4) In applications with LIN auto-addressing the LIN pin is the input of the LIN bus and LIN_O the output to the LIN bus.

5) It is recommended to provide access to the debug interface in the customer application HW for the purpose of analysis.

6) Components to be applied for specific EMC tests and/or to be compliant to different OEM requirements. Refer also to corresponding standards and test specifications.

7) The resistor is required to limit the input current for negative input voltages relative to V_{BVSS0} . The capacitor filters the noise coming from V_{BAT}. If the MON is not used in the application, it should be connected to BVDD (pin is protected against reverse polarity and input current is minimized).

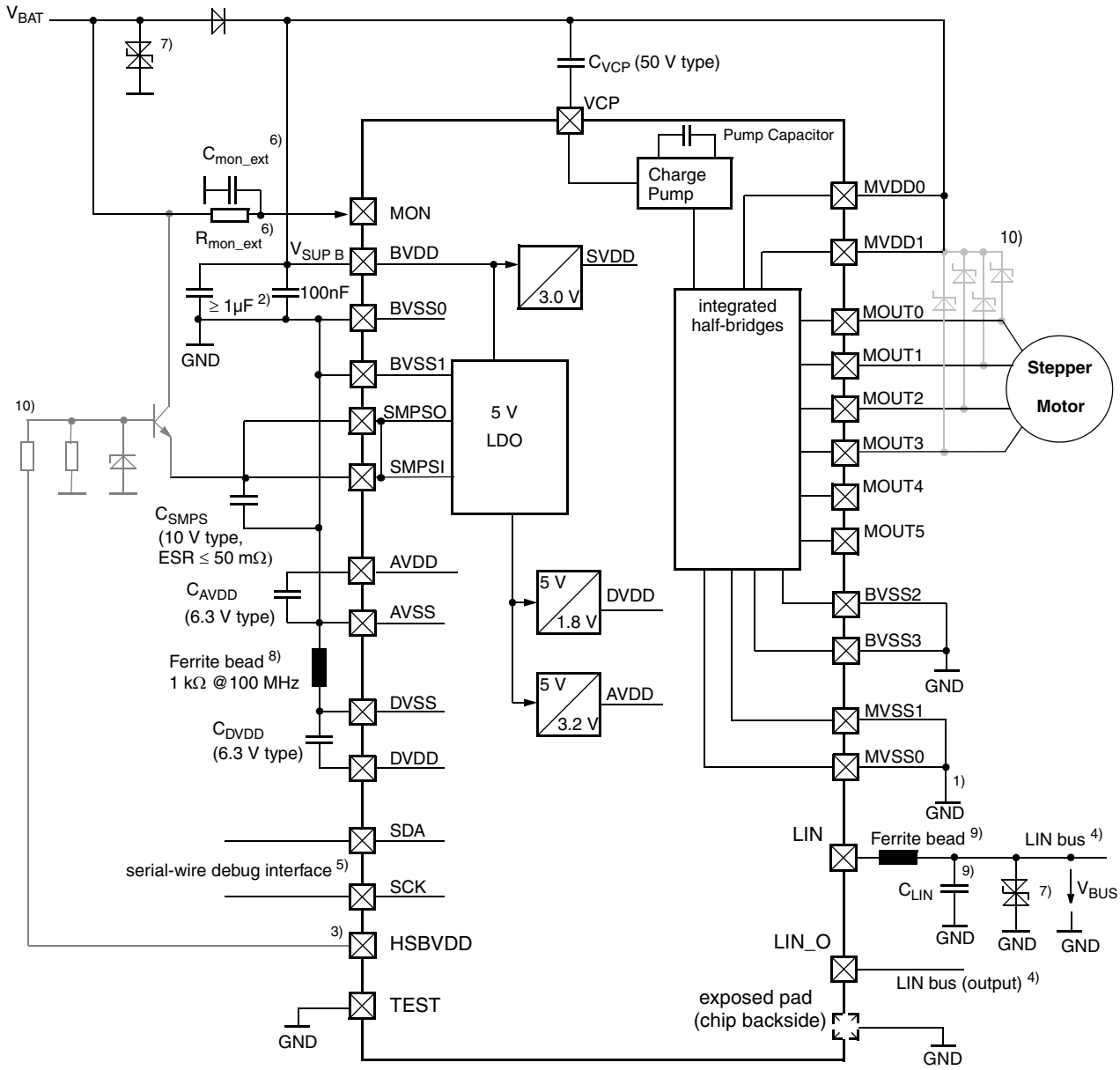
8) A TVS diode or sufficiently dimensioned capacitor is recommended with respect to ISO7637-2:2004 Pulse 2a.

9) A ferrite bead is recommended to be conform with the EME requirements of some OEMs. An impedance of 1 kΩ @ 100 MHz is recommended.

10) Optional circuitry to reduce internal power dissipation. Contact TDK-Micronas for the recommended dimensioning and type of the external components.

Fig. 2–2: Recommended circuitry for BLDC motor control

2.5. External Components Circuit Diagram for Stepper Motor Control



Notes: All capacitors are ceramic types. Refer to the **"Recommended Operating Conditions"** for the resistor, inductor and capacitor values. Blocking capacitors have to be placed as close as possible to the pins.

1) Stepper motor phase currents measured chip internally. No external shunt resistor needed.

2) Choose the BVDD capacitor according to the application needs, e.g. if the NVRAM shall be programmed after VBVDD has dropped below the undervoltage interrupt threshold.

3) To control SMPSI pass transistor.

4) In applications with LIN auto-addressing the LIN pin is the input of the LIN bus and LIN_O the output to the LIN bus.

5) It is recommended to provide access to the debug interface in the customer application HW for the purpose of analysis.

6) The resistor is required to limit the input current for negative input voltages relative to V_{BVSS0}. The capacitor filters the noise coming from V_{BAT}. If the MON is not used in the application, it should be connected to BVDD (pin is protected against reverse polarity and input current is minimized).

7) A TVS diode or sufficiently dimensioned capacitor is recommended with respect to ISO7637-2:2004 Pulse 2a.

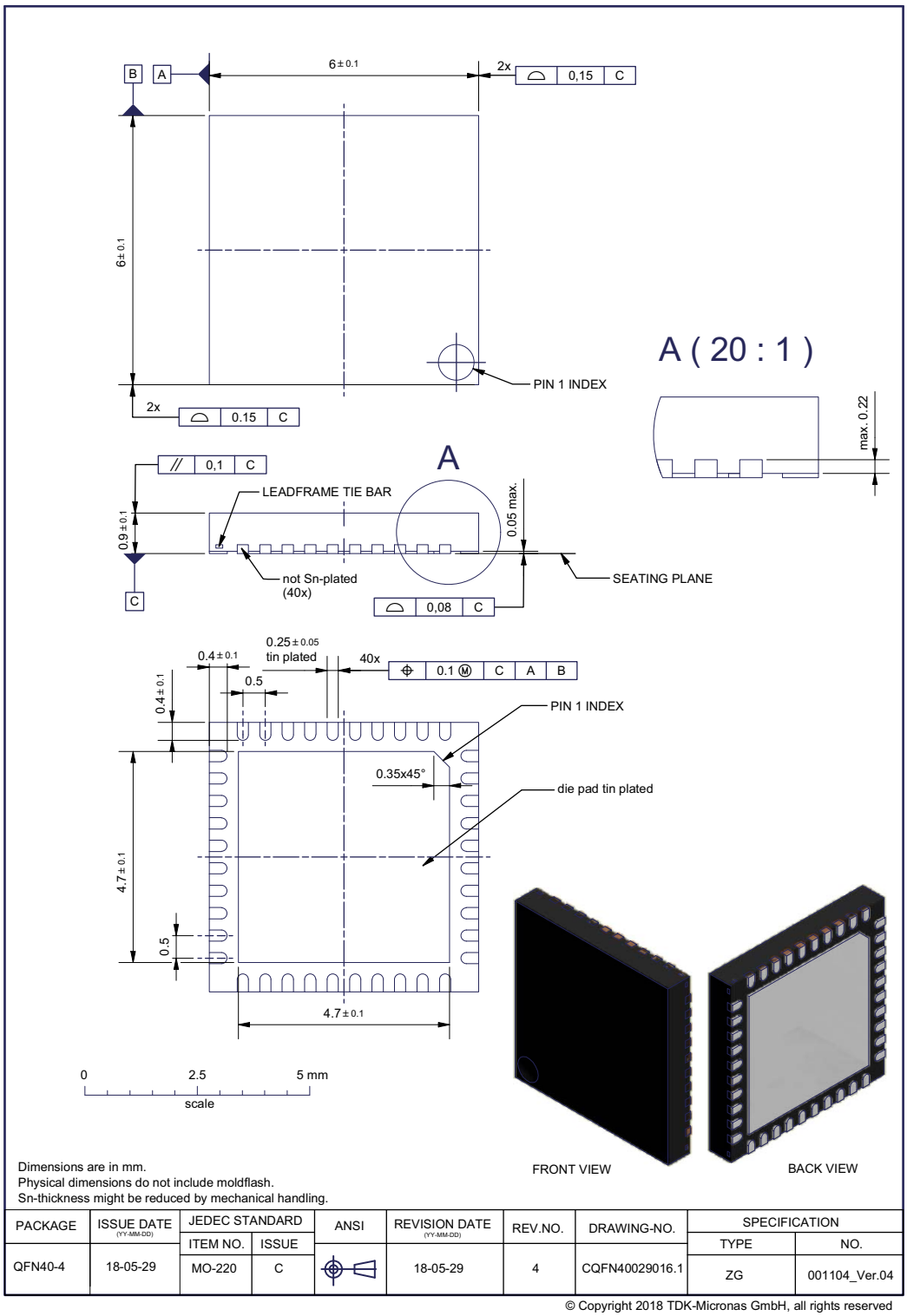
8) A ferrite bead is recommended to be conform with the EME requirements of some OEMs. An impedance of 1 kΩ @ 100 MHz is recommended.

9) Components to be applied for specific EMC tests and/or to be compliant to different OEM requirements. Refer also to corresponding standards and test specifications.

10) Optional circuit to reduce internal power dissipation. Please contact TDK-Micronas for the recommended dimensioning and type of the external components

Fig. 2–3: Recommended circuitry for stepper motor control

2.6. Package Outline Dimensions



PACKAGE	ISSUE DATE (YY-MM-DD)	JEDEC STANDARD		ANSI	REVISION DATE (YY-MM-DD)	REV.NO.	DRAWING-NO.	SPECIFICATION	
		ITEM NO.	ISSUE					TYPE	NO.
QFN40-4	18-05-29	MO-220	C		18-05-29	4	CQFN40029016.1	ZG	001104_Ver.04

Fig. 2–4: PQFN40-4: **P**lastic **Q**uad **F**lat **N**on-leaded package, **40** pins, 6.0×6.0×0.9 mm^3, 0.5 mm pitch.
Ordering code: DL. Weight approximately 0.105 g

3. Electrical Data

3.1. Absolute Maximum Ratings

Stress conditions beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum ratings conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high electro-static voltages or electric fields; however, it is advised that normal precautions must be taken to avoid application of any voltage higher than absolute maximum-rated voltages.

Note All voltages listed in Table 3–1 are referenced to $V_{BVSS0} = V_{BVSS1} = V_{BVSS2} = V_{BVSS3} = V_{AVSS} = V_{DVSS} = 0$ V and $V_{BVDD} = V_{MVDD0} = V_{MVDD1}$ except where otherwise noted. All ground pins must be connected to a low-resistive ground plane close to the IC. Negative currents indicate currents flowing out of the chip.

Table 3–1: Absolute maximum ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit	Condition
T_J	Junction temperature under bias		–40	175	°C	A thermal shutdown (TSD) is generated above recommended operation temperature to force device into a reset state (see Section 3.4.)
$T_{storage}$	Transportation/short-term storage temperature		–55	150	°C	Device only without packing material.
$V_{SUP\ B}$	Main supply voltage	BVDD, MVDD0, MVDD1	–0.3	40	V	
$DV/Dt_{\ VSUP\ B}$	Main supply voltage slope	BVDD, MVDD0, MVDD1		10	V/µs	$V_{BVDD} \leq 19$ V For 40 V $\geq V_{BVDD} >$ 19 V refer to maximum main supply voltage slope value according to ISO 7637-2:2004 pulse 5b. E07 pulse requirement with 0.5 V/min is fulfilled. For elevated temperature range together with recommend external components as shown in Fig. 2–2 and Fig. 2–3 the C_{SMPS} shall be $C_{SMPS} \geq 4.7$ µF

Table 3–1: Absolute maximum ratings**, continued**

Symbol	Parameter	Pin Name	Min.	Max.	Unit	Condition
I_{SUP}	Supply current	BVDD, BVSS0, BVSS1, BVSS2, BVSS3	–100	100	mA	Supply current limitation with respect to product reliability over lifetime (e.g. due to electro migration). The current can be interpreted as an RMS value.
	Motor supply current	MVDD0, MVDD1, MVSS0, MVSS1, MOUTx	–1000	1000	mA	With MOUTx port limits for $I_{out\ RMS}$ and $I_{out\ peak}$ according to the recommended operating conditions.
V_{MVSS}	Motor bridge ground	MVSS0, MVSS1	–0.3	0.3	V	
V_{in}	Input voltage on LIN pin	LIN	–27	40	V	
	Input voltage for 3.2 V GPIO ports	SDA, SCK, LGPIOx, TEST	–0.3	3.65	V	Min. value calculated according to V_{AVSS} –0.3 V Max. value calculated according to V_{AVDD} +0.3 V
	Input voltage on MOUT pins	MOUTx	–0.3	40	V	5 × 400 ms, with 30 sec. period. cumulative 1 h max. The application SW has to take measures to reduce the motor-current or to turn off the motor due to the deactivated charge-pump in overvoltage mode. It is recommended to stop the motor and to turn-on all power-bridge low-side MOSFETs. Dynamically lower voltages during free-wheeling are covered by the maximum specified phase currents.
	Input voltage on HSBVDD pin	HSBVDD	–0.3	40	V	5 × 400 ms, with 30 sec. period. cumulative 1 h max. Min. value calculated according to V_{BVSS} – 0.3 V
	Input voltage on MON pin applied via resistor R_{mon_ext} (see Fig. 2–2 and Fig. 2–3)	MON	–27	40	V	5 × 400 ms, with 30 sec. period. cumulative 1 h max.
I_{out}	Output current LGPIOx pins and SDA pin	SDA, LGPIOx	–20	20	mA	
	Output current for HSBVDD port	HSBVDD	–30	0	mA	
$I_{out\ total}$	Sum of output currents derived from AVDD regulator for 3.2 V GPIO ports and from AVDD pin	SDA, LGPIOx, AVDD	–20		mA	
	Sum of output currents derived from SMPSI pin, AVDD regulator for 3.2 V GPIO ports and from AVDD pin	SMPSI, SDA, LGPIOx, AVDD	–40		mA	

3.2. ESD and Latch-Up

Table 3–2: ESD and latch-up

Symbol	Parameter	Min.	Max.	Unit	Comment
I_{latch}	Maximum latch-up free current (measurement according to AEC Q100-004 Grade 1 at T_A=+125 °C)	–300	300	mA	MOUT pins, T_J > 130 °C
		–1000	1000	mA	MOUT pins, T_A = 25 °C
		–100	100	mA	All other pins.
V_{HBM}	Human body model, equivalent to discharge 100 pF with 1.5 kΩ (measurement according to AEC-Q100-002)	–8	8	kV	LIN [1)]
		–2	2	kV	All other pins.
$V_{System\ ESD}$	According to IEC 61000-4-2 (330 Ω, 150 pF)	–6	6	kV	LIN to GND[1)]
V_{CDM}	Charged device model (measurement according to AEC-Q100-011) [1)]	–750	750	V	Machine model is only optional according to AEC-Q100.
V_{MM}	Machine model (measurement according to JESD22-A115 / AEC-Q100-003)	–200	200	V	Machine model is only optional according AEC-Q100.

[1)] According to OEM requirement specification “Hardware Requirements for LIN, CAN, and FlexRay Interfaces in Automotive Applications v1.3” from May 4, 2012. Further components like varistor, TVS diode, or passives might be necessary to fulfill requirements of other OEM specifications.

3.3. Transient Supply Voltage

Table 3–3: Transient supply voltage

Parameter	Pin Name	Min.	Max.	Unit
ISO 7637-2:2004 pulse 1 [1)]	BVDD	–100		V
ISO 7637-2:2004 pulse 2a [2)]	BVDD		75 [3)7)]	V
ISO 7637-2:2004 pulse 2b	BVDD		10	V
ISO 7637-2:2004 pulse 3a [1) 4)]	BVDD	–150		V
ISO 7637-2:2004 pulse 3b [4) 5)]	BVDD		100 [7)]	V
ISO16750-2:2012	BVDD	[6)]	[6)]	V
ISO 16750-2:2012	BVDD		40 400	V ms
ISO 16750-2	BVDD		28 2	V min.

1) With reverse polarity diode.
2) Reverse polarity diode and 1 µF blocking capacitor with low ESR.
3) According to OEM requirement specification “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications v1.3” from May 4, 2012.
4) 4.7 kΩ minimum series resistance for I/O ports.
5) The sum of the whole clamping currents must not exceed 100 mA.
6) Values according to OEM specifications.
7) With TVS diode.

The ISO 7637 standard is the base for the OEM supplier specifications.

Automotive test pulses are applied on module level. The IC pins used to connect the module to the wiring harness shall be used with appropriate protection circuitry. Refer also to Fig. 2–2 on page 22 and Fig. 2–3 on page 23.

3.4. Recommended Operating Conditions

Warning **Do not insert the device into a live socket. Instead, after proper insertion into the socket apply power by switching on the external power supply.**

Failure to comply with the above recommendations will result in unpredictable behavior of the device and may result in device destruction. Functional operation of the device at conditions beyond those indicated in the “Recommended Operating Conditions” is not implied and may result in unpredictable behavior, reduce reliability and lifetime of the device.

All externally applied discrete components must be selected according to the required temperature range in the application.

Note All voltages listed in Table 3–4 are referenced to $V_{BVSS0} = V_{BVSS1} = V_{BVSS2} = V_{BVSS3} = V_{DVSS} = V_{AVSS} = 0$ V and $V_{SUP\ B} = V_{BVDD} = V_{MVDD} = V_{MVDD1}$ except where otherwise noted. All ground pins (BVSS0, BVSS1, BVSS2, BVSS3, AVSS, DVSS) must be connected to a low-resistive ground plane close to the IC. The pins MVSS0 and MVSS1 might be connected to ground via shunt resistor for motor current measurements.

Table 3–4: Recommended operating conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Condition
T_J	Junction temperature under bias HVC 4x22F only		–40		160	°C	According to Mission Profile for extended temperature range up to 160 °C. Please contact TDK-Micronas for more detailed information.
	all others		-40		150	°C	
$V_{SUP\ B}$	Main supply voltage	BVDD, MVDD0, MVDD1	8	14	18	V	2)3)
			5.4		40	V	1)2)3) 5 x 400 ms, with 30 sec. period. cumulative 1 h max. Refer to Table 3–3 on page 28 for transient supply voltages.
$V_{SUP\ B\ RETENTION}$	Main supply voltage during RETENTION mode	BVDD, MVDD0, MVDD1	2.5			V	RAM content is preserved. No CPU function. Return from RETENTION mode with Power-on Reset (POR).

Table 3–4: Recommended operating conditions**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Condition
V_{MVSS}	Motor bridge ground	MVSSx	−0.065		0.3	V	Min value limited due to linearity of ADC. If negative voltage ADC measurement is not needed this voltage can be extended to −0.3 V.
3.2 V Port input voltage							
V_{il}	Input low voltage	LGPIOx, TEST, SCK, SDA	0		0.28	V_{AVDD}	
V_{ih}	Input high voltage	LGPIOx, TEST, SCK, SDA	0.72		1	V_{AVDD}	
Port output currents							
I_{out}	Continuous output current LGPIO port	LGPIOx	−4		4	mA	
	Continuous output current HSBVDD port	HSBVDD	−15			mA	
	Continuous output current SMPSI	SMPSI	−40			mA	According to $I_{out\ total}$ in Table 3–1 on page 25. The sum of currents derived from SMPSI, AVDD, and LGPIO ports must not exceed the here specified limits!
$I_{out\ RMS}$	MOUT port RMS output current	MOUTx	−300		300	mA	According to the fly-back current derating specified under Section 3.6. on page 42.
$I_{out\ peak}$	MOUT port peak output current t_{ON} < 1 s (single MOUT)	MOUTx	−500		500	mA	Contact TDK-Micronas for dedicated application support.
LIN Transceiver[3)]							
V_{BUS}	LIN bus voltage	LIN	−2.7		20.7	V	
t_{whi}	High time after Wake Pulse	LIN	1			1 / f_{AUX}	
AVDD Regulator, 3.2 V supply voltage							
C_{AVDD}	External buffer capacitor	AVDD	100		470	nF	[4)]
DVDD Regulator, 1.8 V supply voltage							
C_{DVDD}	External buffer capacitor	DVDD	1		2.2	µF	[4)]

Table 3–4: Recommended operating conditions**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Condition
Charge pump (integrated bridge)							
C_{VCP}	Charge pump capacitor	VCP	22		1000	nF	4)
5 V LDO							
C_{SMPS}	SMPS capacitor ESR ≤ 50 mΩ	SMPSI	1	2.2	22	µF	4) For elevated temperature range together with recommend external components as shown in Fig. 2–2 and Fig. 2–3 the C_{SMPS} shall be $C_{SMPS} \geq 4.7\mu F$
V_{BAT} Monitor							
R_{mon_ext}	External resistor on MON Pin for current limitation	MON	4.7		27	kΩ	4)
C_{mon_ext}	External capacitor on MON Pin	MON	47			nF	4)

1) Some analog parameters may degrade and full motor operation is not guaranteed.
2) If $V_{BVDD} > V_{BVDDO}$ the application SW is responsible to limit the power dissipation to keep T_J inside Recommended Operating Conditions.
3) Compliant with “LIN Physical Layer Specification Revision 2.1”.
4) All externally applied discrete components must be selected according to the required temperature range in the application.

3.5. Characteristics

Note Unless otherwise written all parameters listed in Table 3–5 are valid for the conditions $V_{BVSS0} = V_{BVSS1} = V_{BVSS2} = V_{BVSS3} = V_{DVSS} = V_{AVSS} = 0$ V, 8 V ≤ V_{BVDD} ≤ 18 V, $V_{SUP\ B} = V_{BVDD} = V_{MVDD0} = V_{MVDD1}$, T_J = −40 °C to 150 °C. HVC 4x22F devices are also tested at 160 °C. External components and connections according to Fig. 2–2 on page 22 or Fig. 2–3 on page 23.

Table 3–5: Characteristics

Symbol	Parameter	Pin Name	Min.	Typ.[1)]	Max.	Unit	Conditions
Package							
R_{thJC}	Thermal resistance from junction to case				10	K/W	Parameter is simulated with model of 1s1p board according JEDEC. Values are only valid if the exposed pad is soldered onto the PCB.
R_{thJA}	Thermal resistance from junction to ambient				25	K/W	
Supply Currents (CMOS levels on all inputs, no loads on outputs)							
I_{DDP}	ACTIVE mode supply current HVC 422xF	BVDD		22	30	mA	$f_{SYS} = f_{CPU}$ = 20 MHz, V_{BVDD} = 12 V, all peripherals on. I_{DDP} can be reduced by activating peripherals only during the time they are used.
	ACTIVE mode supply current HVC 442xF			25	38		
I_{DDI}	IDLE mode supply current HVC 422xF	BVDD		2.6	3.5	mA	Main osc. off CP off ERM off, All peripherals off, V_{BVDD} = 12 V, Maximum value valid for $T_J \leq 100$ °C.
	IDLE mode supply current HVC 442xF				4		
I_{DDSL}	SLEEP mode supply current	BVDD, MVDD0, MVDD1		35	50	µA	[2)] RAM off, main osc. off, auxiliary osc. on $V_{AVDD} = V_{DVDD} = V_{SMPSI}$ = 0 V Maximum value valid at $T_A = T_J \leq 100$ °C. $T_J \sim T_A$ due to the very low self-heating in SLEEP Mode.

Table 3–5: Characteristics**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.[1)]	Max.	Unit	Conditions
Low-Voltage General-Purpose I/O Ports (LGPIO Ports), SDA, SCK, and TEST Pin							
V_{ihl}	Input high-to-low threshold voltage	LGPIOx, SDA, SCK, TEST	0.28			V_{AVDD}	
V_{ilh}	Input low-to-high threshold voltage				0.72	V_{AVDD}	
V_{hyst}	Schmitt trigger hysteresis		0.5			V	[2)]
I_{ihigh_pd}	Input with weak pull-down		5	30	110	µA	V_{in}=V_{AVDD}. LGPIO port internal weak pull-down configuration applied.
I_{ilow}	Input low current		–10		10	µA	V_{in} = 0 V
I_{ilow_pu}	Input with weak pull-up	LGPIOx, SDA	–110	–30	–5	µA	V_{in} = 0 V. LGPIO port internal weak pull-up configuration applied.
I_{ihigh}	Input high current		–10		10	µA	V_{in} = V_{AVDD} No internal weak pull-down/up configuration applied.
V_{ol}	Port low output voltage	LGPIOx, SDA			0.4	V	I_{ol} = 4 mA
V_{oh}	Port high output voltage	LGPIOx, SDA	0.8			V_{AVDD}	I_{oh} = –4 mA
HSBVDD Pin							
V_{oh}	Port high output voltage	HSB-VDD	1			V_{BVDD} – 1 V	I_O = –15 mA
I_{ocson}	Overcurrent shutdown in on-state	HSB-VDD			–20	mA	HSBVDD.DO = 1

Table 3–5: Characteristics**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.[1)]	Max.	Unit	Conditions
MOUT Ports							
$R_{DS(ON)hs}$	Static drain-source on-resistance of high-side N-channel MOSFET	MOUTx		2	2.8	Ω	I_{MOUT} = –500 mA, $V_{MVSS0} = V_{MVSS1} = V_{BVSS0} = V_{BVSS1} = V_{BVSS2} = V_{BVSS3}$
$R_{DS(ON)ls}$	Static drain-source on-resistance of low-side N-channel MOSFET	MOUTx		2	2.8	Ω	I_{MOUT} = 500 mA, $V_{MVSS0} = V_{MVSS1} = V_{BVSS0} = V_{BVSS1} = V_{BVSS2} = V_{BVSS3}$
I_{ocshi}	Overcurrent shutdown in high state	MOUTx	–0.9			A	
I_{ocslo}	Overcurrent shutdown in low state	MOUTx			0.9	A	
R_{MOUT}	MOUT pull-down resistor network (for BEMFC reference generation)	MOUTx		96		kΩ	$V_{MOUT0} = V_{MOUT1} = V_{MOUT2} = V_{MOUT3} = V_{MOUT4} = V_{MOUT5}$ 2)
LIN Pin (7 V ≤ V_{BVDD} ≤ 18 V)							
V_{BUSL}	Output low voltage	LIN		0.8	1.2	V	Refer to LIN-Specification v1.3, $V_{Busdom\_DRV\_LoSUP}$
R_{SLAVE}	Internal pull-up resistance at output	LIN	20	30	60	kΩ	
V_{BUS_OH}	Transmitter recessive voltage	LIN	0.8		1	V_{BVDD}	Open load
I_{BUS_LIM}	Current shutdown threshold for driver dominant state	LIN	40		200	mA	V_{BUS} = 18 V Driver on
$I_{BUS\_PAS\_dom}$	Input leakage current at the receiver inclusive pull-up resistor as specified	LIN	–1			mA	V_{BUS} = 0 V V_{BAT} = 12 V Driver off
$I_{BUS\_PAS\_rec}$	Leakage current at the receiver inclusive pull-up resistor as specified	LIN			20	µA	8 V < V_{BUS} < 18 V 8 V < V_{BAT} < 18 V $V_{BUS} \geq V_{BAT}$ Driver off
$I_{BUS\_NO\_GND}$	Leakage current at ground loss	LIN	–1		1	mA	$V_{GND} = V_{BVDD}$ 0 V < V_{BUS} < 18 V V_{BAT} =12 V
$I_{BUS\_NO\_BAT}$	Leakage current at BVDD loss	LIN			30	µA	$V_{BVDD} = V_{GND}$ 0 V < V_{BUS} < 18 V V_{BAT} =disconnected
V_{BUSdom}	Receiver dominant state	LIN			0.4	V_{BVDD}	Without external diode.
V_{BUSrec}	Receiver recessive state	LIN	0.6			V_{BVDD}	
V_{BUS_CNT}	Center of receiver threshold	LIN	0.475	0.5	0.525	V_{BVDD}	$V_{BUS\_CNT} = (V_{th\_dom} + V_{th\_rec}) / 2$
V_{HYS}	Hysteresis of receiver threshold	LIN			0.175	V_{BVDD}	$V_{HYS} = V_{th\_rec} - V_{th\_dom}$

Table 3–5: Characteristics**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.[1)]	Max.	Unit	Conditions
LIN Driver, 20.0 kbps (t_{Bit} = 50 µs), LIN_CR.SR = 2, bus load conditions (C_{BUS}; R_{BUS}): 1 nF; 1 kΩ / 6.8 nF; 660 Ω / 10 nF; 500 Ω; 7 V ≤ V_{BVDD} ≤ 18 V.							
D1	Duty cycle 1	LIN	0.396				$TH_{Rec(max)}$ = 0.744 x V_{BVDD}; $TH_{Dom(max)}$ = 0.581 x V_{BVDD}; V_{BVDD} = 7.0 V to 18 V; D1 = $t_{Bus\_rec(min)}$ / (2 x t_{Bit})
D2	Duty cycle 2	LIN			0.581		$TH_{Rec(min)}$ = 0.422 x V_{BVDD}; $TH_{Dom(min)}$ = 0.284 x V_{BVDD}; V_{BVDD} = 7.6 V to 18 V; D2 = $t_{Bus\_rec(max)}$ / (2 x t_{Bit})
LIN Driver, 10.4 kbps (t_{Bit} = 96 µs), LIN_CR.SR = 3, Bus/LIN load conditions (C_{Bus}; R_{Bus}): 1 nF; 1 kΩ / 6.8 nF; 660 Ω / 10 nF; 500 Ω; 7 V ≤ V_{BVDD} ≤ 18 V.							
D3	Duty cycle 3	LIN	0.417				$TH_{Rec(max)}$ = 0.778 x V_{BVDD}; $TH_{Dom(max)}$ = 0.616 x V_{BVDD}; V_{BVDD} = 7.0 V to 18 V; D3 = $t_{Bus\_rec(min)}$ / (2 x t_{Bit})
D4	Duty cycle 4	LIN			0.590		$TH_{Rec(min)}$ = 0.389 x V_{BVDD}; $TH_{Dom(min)}$ = 0.251 x V_{BVDD}; V_{BVDD} = 7.6 V to 18 V; D4 = $t_{Bus\_rec(max)}$ / (2 x t_{Bit})
The following parameters are defined in the LIN specification Rev. 2.x: V_{th_dom}, V_{th_rec}, $TH_{Rec(max)}$, $TH_{Rec(min)}$, $TH_{Dom(max)}$, $TH_{Dom(min)}$, $t_{Bus\_rec(max)}$, $t_{Bus\_rec(min)}$, t_{Bit}							

Table 3–5: Characteristics**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.[1)]	Max.	Unit	Conditions
LIN Transceiver (7 V ≤ V_{BVDD} ≤ 18 V).							
t_{rx_pd}	Receiver propagation delay	LIN			6	µs	
t_{rx_sym}	Receiver propagation delay symmetry	LIN	–2		2	µs	
C_{SLAVE}	Slave capacitance	LIN	30	48	60	pF	Guaranteed by design with respect to LIN 2.1 physical layer conformance test specification.
dV/dt_{fall}	Falling edge slew rate	LIN		1.5		V/µs	SR = 1, 2, or 3[2)]
				10			SR = 0[2)] With bus-load C_{BUS} =1 nF and R_{BUS} =1 kΩ. Fast slew-rate e.g. needed for operation with PWMIO at LIN port.
dV/dt_{rise_max}	Maximum rising edge slew rate	LIN		1.5		V/µs	SR = 1, 2, or 3[2)]
				10			SR = 0[2)] With bus-load C_{BUS} =1 nF and R_{BUS} =1 kΩ. Fast slew-rate e.g. needed for operation with PWMIO at LIN port.
t_{wup}	Low pulse time for wake-up	LIN	28		150	µs	V_{BUS} < V_{BVDD} / 2 – 360 mV. Minimum value according to “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications v1.3” from May 4, 2012. Maximum value according to “LIN Specification Package Revision 2.1” from November 24, 2006.
LIN Auto-Addressing related parameter (9 V ≤ V_{BVDD} ≤ 15 V, 0 °C ≤ T_A ≤ 50 °C). According to “Lastenheft Klima-Standardaktuator mit LIN-Bus Schnittstelle 2.x” from January 28, 2013.							
I_{CS}	Current source	LIN	1.85	2.05	2.25	mA	
R_{BSM}	Bus shunt resistor	LIN, LIN_O		1	1.25	Ω	

Table 3–5: Characteristics**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.[1)]	Max.	Unit	Conditions
BEMF Comparators (BEMFC)							
$BEMFC_{delay}$	BEMF Comparator delay time	MOUTx		500	550	ns	2)
$BEMFC_{hyst}$	BEMF Comparator input hysteresis	MOUTx	30		70	mV	2)
8-Bit Current Limit DAC (CLDAC)							
LSB_{CLDAC}	LSB value CLDAC		1.6	2.0	2.8	mA	2) Without SW trimming for gain and offset correction I_{MOUT} > 10 mA
LSB_{CLDAC}	LSB value CLDAC		1.9	2	2.1	mA	2) 3) With SW trimming for gain and offset correction I_{MOUT} > 10 mA
ZE_{CLDAC}	CLDAC zero error		–20		10	LSB	2) Without SW trimming for gain and offset correction
ZE_{CLDAC}	CLDAC zero error		–5		5	LSB	2) 3) With SW trimming for gain and offset correction
DNL_{CLDAC}	CLDAC differential non-linearity		–0.5		0.5	LSB	2)
INL_{CLDAC}	CLDAC integral nonlinearity		–5.0		5.0	LSB	2)
12-Bit ADC (including signal path)							
$LSB_{ADC\&SP}$	LSB value of the ADC including the signal path			0.976		mV	Guaranteed by design ($V_{REF-ADC}$ trimmed).
$INL_{ADC\&SP}$	ADC integral non-linearity including the signal path		–16		16	LSB	2)
$DNL_{ADC\&SP}$	ADC differential non-linearity including the signal path		–8		8	LSB	2)

Table 3–5: Characteristics**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.[1)]	Max.	Unit	Conditions
$V_{in\ ADC}$	ADC linear input voltage range LGPIO ports versus AVSS	LGPIO0, LGPIO1, LGPIO2, LGPIO3	0		3.3	V	[2)] G_{PGA} = 4
	ADC linear input voltage range MON and BVDD versus AVSS	MON, BVDD	8		18	V	[2)] G_{PGA} = 4
	ADC linear input voltage range STDA and STDB inputs (from motor phase)	MOUT0, MOUT1, MOUT2, MOUT3	–18		18	V	[2)] G_{PGA} = 4
	ADC linear input voltage range motor current shunt MVSSx versus BVSS0	MVSS0, MVSS1	–65		300	mV	[2)] G_{PGA} = 4
			–65		175	mV	[2)] G_{PGA} = 10
	ADC linear input voltage range differential input LGPIO8 versus LGPIO9	LGPIO8, LGPIO9	–2.7		2.7	V	[2)] G_{PGA} = 4
SPE	Signal path error of ADC measurement at LGPIO ports versus AVSS	LGPIO0, LGPIO1, LGPIO2, LGPIO3	–3		3	%	[2)] G_{PGA} = 4
			–5		5	%	[2)] G_{PGA} = 10 SPE for gain 20 and 40 on customer request.
	Signal path error of ADC measurement at MON and BVDD versus AVSS	MON, BVDD	–2		2	%	[2)] G_{PGA} = 4
	Signal path error of ADC measurement at STDA and STDB inputs (from motor phase)	MOUT0, MOUT1, MOUT2, MOUT3	–5		5	%	[2)] G_{PGA} = 4
			–7		7	%	[2)] G_{PGA} = 10
	Signal path error of ADC measurement at motor current shunt MVSSx versus BVSS0	MVSS0, MVSS1	–4		4	%	[2)] G_{PGA} = 4 –65 mV ≤ V_{MVSS} ≤ 0.3 V
			–7		7	%	[2)] G_{PGA} = 10 –65 mV ≤ V_{MVSS} ≤ 175 mV
	Signal path error of ADC measurement at differential input LGPIO8 versus LGPIO9	LGPIO8, LGPIO9	–5		5	%	[2)] G_{PGA} = 4
	Signal path error of ADC measurement at differential input LGPIO8 versus LGPIO9	LGPIO8, LGPIO9	–8		8	%	[2)] G_{PGA} = 10

Table 3–5: Characteristics**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.[1)]	Max.	Unit	Conditions
$ZE_{ADC\&SP}$	ADC zero error including the LGPIO signal path	LGPIO0, LGPIO1, LGPIO2, LGPIO3	–20		20	LSB	[2)] G_{PGA} = 4
			–50		50	LSB	[2)] G_{PGA} = 10. ZE for gain 20 and 40 on customer request.
	ADC zero error including the STDA or STDB signal path	MOUT0, MOUT1, MOUT2, MOUT3	–20		20	LSB	[2)] G_{PGA} = 4 BEMFC off
			–40		20	LSB	[2)] G_{PGA} = 4 BEMFC on
			–50		50	LSB	[2)] G_{PGA} = 10 BEMFC off
			–100		50	LSB	[2)] G_{PGA} = 10 BEMFC on
	ADC zero error including the LGPIO8/9 signal path	LGPIO8, LGPIO9	–20		20	LSB	[2)] G_{PGA} = 4
			–60		60	LSB	[2)] G_{PGA} = 10
	ADC zero error including the MON or BVDD signal path	MON, BVDD	–20		20	LSB	[2)] G_{PGA} = 4
	ADC zero error including the MVSSx signal path	MVSS0, MVSS1	–20		20	LSB	[2)] G_{PGA} = 4 –65 mV ≤ V_{MVSS} ≤ 0.3 V
			–50		50	LSB	[2)] G_{PGA} = 10 –65 mV ≤ V_{MVSS} ≤ 175 mV
CR	Conversion range		–1		1	$V_{REF-ADC}$	Guaranteed by design ($V_{REF-ADC}$ trimmed).
t_c	Conversion time			1		µs	Conversion time variation according to f_{MAIN} tolerance must be added.
t_W	ADC signal path warm-up time				10	µs	[2)]
$V_{REF-ADC}$	ADC reference voltage			2		V	Guaranteed by design. $V_{REF-ADC}$ trimmed.

Table 3–5: Characteristics**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.[1)]	Max.	Unit	Conditions
High-Resolution Temperature Sensors							
ΔT	Temperature error of sensor readable by ADC		–10		10	°C	[2)]
Temperature supervision / Thermal shutdown							
T_{TSD}	Thermal shutdown temperature HVC 4x22F		167	172	177	°C	[2)]
	others		155	165	175	°C	[2)]
T_{TSDR}	Thermal shutdown return temperature		125	135	145	°C	[2)]
40 MHz Main Oscillator							
f_{MAIN}	Main oscillator output frequency		37.1	40	41.1	MHz	With ERM off.
35 kHz Auxiliary Oscillator							
f_{AUX}	Auxiliary oscillator output frequency		21	35	49	kHz	
5V LDO Pre-regulator (Supply Voltage to AVDD and DVDD Regulators)							
V_{SMPSI}	SMPS output voltage	SMPSI	4.5	5	5.5	V	
AVDD Regulator (Analog Supply Voltage)							
V_{AVDD}	Internal analog supply voltage	AVDD	3.1	3.25	3.35	V	
DVDD Regulator (Digital Supply Voltage)							
V_{DVDD}	Internal digital supply voltage	DVDD	1.6	1.85	1.98	V	
V_{BAT} Monitor							
V_{BATin}	MON pin input voltage where the ADC can be used for V_{BAT} measurement and the V_{BAT} OV/UV comparators work according specification	MON	6			V	[2)]
V_{BATUp}	Battery undervoltage low-to-high threshold	MON		7.9	8.25	V	
V_{BATUn}	Battery undervoltage high-to-low threshold	MON	7.32	7.67		V	
V_{BATOp}	Battery overvoltage low-to-high threshold	MON		20.6	21.4	V	
V_{BATOn}	Battery overvoltage high-to-low threshold	MON	18.8	19.4		V	
BVDD Monitor							
V_{BVDDUp}	BVDD undervoltage low-to-high threshold	BVDD		6.45	6.75	V	
V_{BVDDUn}	BVDD undervoltage high-to-low threshold	BVDD	5.97	6.26		V	
V_{BVDDOp}	BVDD overvoltage low-to-high threshold	BVDD	18.2	19	19.7	V	
V_{BVDDOn}	BVDD overvoltage high-to-low threshold	BVDD	17.2	17.9	18.4	V	

Table 3–5: Characteristics**, continued**

Symbol	Parameter	Pin Name	Min.	Typ.[1]	Max.	Unit	Conditions
Power-On Reset (POR) Voltage							
V_{POR}	POR release threshold voltage if going from power-up to ACTIVE mode	BVDD			5.4	V	[2]
V_{POR_sleep}	Supply voltage limit where a POR is asserted if chip is in SLEEP mode	BVDD	0.5			V	[2]
$V_{POR\_retention}$	Supply voltage limit where a POR is asserted if chip is in RETENTION mode	BVDD			2.5	V	[2]
V_{POR_tsd}	Supply voltage limit where a POR is asserted if chip is in TSD mode	BVDD			3	V	[2]
RETENTION Mode							
V_{RET}	Threshold voltage when going from ACTIVE mode to RETENTION mode. Refer also to the respective state chart in the User Guide of HVC 4223F.	BVDD			5.35	V	[2]
NVRAM							
t_{STORE}	Time to store all data within one NVRAM page				15	ms	Storage time for NVRAM page data.
N_{Ns}	Number of store cycles for each NVRAM page		10 k			cycles	T_J = 150 °C For store cycles at 150°C < $T_J \leq$ 160 °C please contact TDK-Micronas
			100 k			cycles	T_J = 25 °C
t_{Nret}	NVRAM data retention		16			years	Qualified according to AEC-Q100 for temperature grade 1.
Flash							
N_{Fwe}	Flash memory endurance write/erase cycles		1000			cycles	Qualified according to AEC-Q100 for temperature grade 3. Customer specific mission profiles might allow other cycle numbers.
t_{Fret}	Flash memory data retention		16			years	Qualified according to AEC-Q100 for temperature grade 1.

1) Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied, and are not 100% tested.
2) Parameter is derived from design characterization on a small sample size.
3) For detailed information on the CLDAC trimming algorithm, please refer to the Application Note “HVC 4223F CLDAC Trimming Algorithm”.

3.6. MOUT Fly-Back Current Derating

To allow operation at elevated temperatures according to the customer mission profile, it is recommended to apply additional circuitry.

1. Freewheeling Schottky diodes connected from the three motor phase outputs MOUT0/1, MOUT2/3 and MOUT4/5 to MVDD.
2. Supply SMPSI node externally by over-driving this node (applying a higher voltage)
   - An NPN transistor to reduce power dissipation of internal 5V regulator. See Fig. 2–2 and Fig. 2–3.
   - If the node SMPSI is externally supplied, the internal linear regulator will limit the internal current from BVDD to a minimum.

If the freewheeling Schottky diodes are not used, Fig. 3–1 and Fig. 3–2 illustrate the derating curves for the sum of the MOUT port fly-back currents with respect to the fly-back discharge type (passive or active). Refer also to the recommended operating conditions.

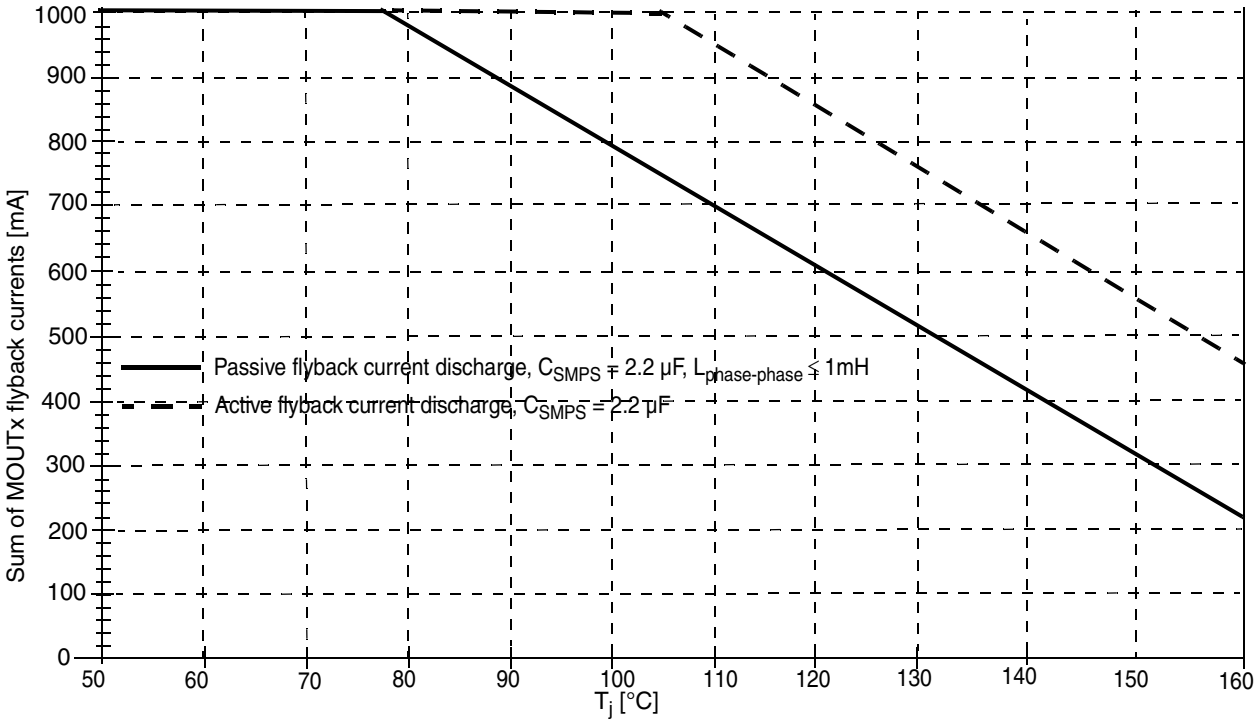


Fig. 3–1: Brushless motor derating curve for sum of MOUT currents with active or passive fly-back current discharge.

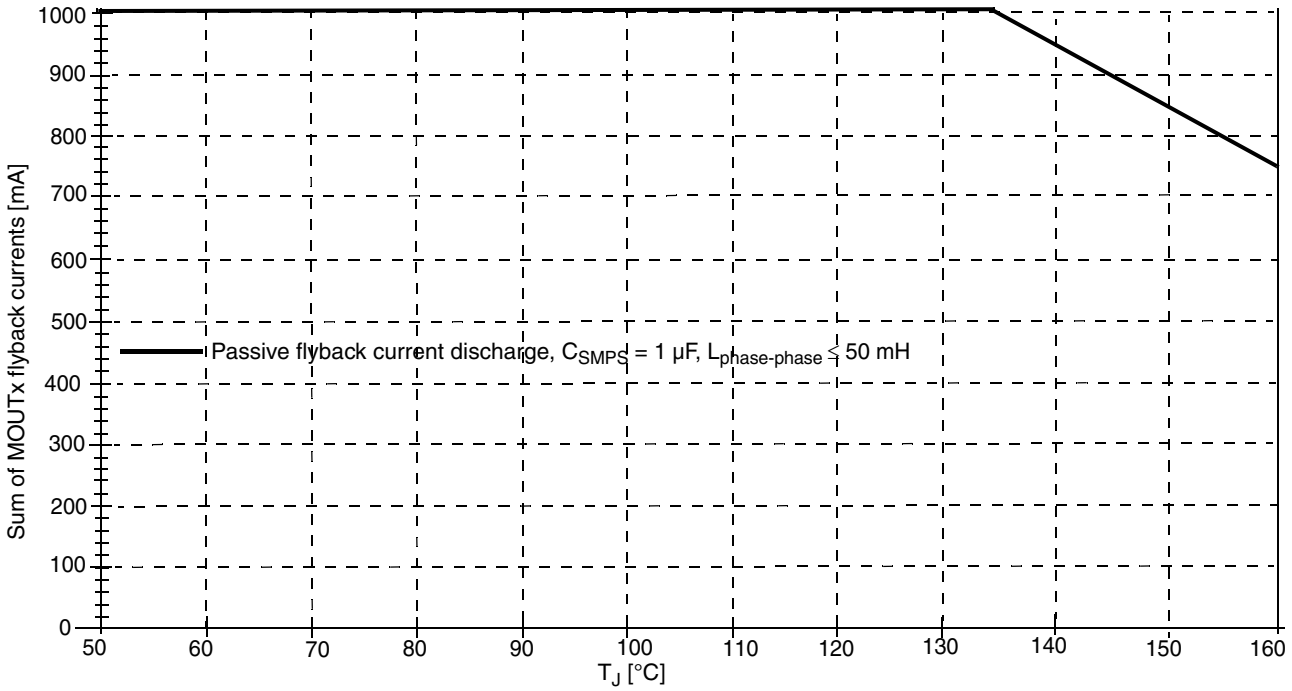


Fig. 3–2: Stepper motor derating curve for sum of MOUT currents with passive fly-back current discharge.

Note Single reset events (e.g. by watch-dog reset or other chip reset sources) during motor operation will cause passive freewheeling. Such conditions are acceptable with motor currents within the active flyback SOA curves.

4. Functional Description

4.1. Power Supply

The HVC 4x family can be directly connected to the 12 V automobile on-board power supply and withstands all disturbances appearing on the car's supply, specified in ISO 7637-2:2004. The polarity protection for the HVC 4x family should be provided by an external device (e.g. diode or MOSFET). An external voltage regulator for the system supply is not required.

4.1.1. Start-Stop Applications

The HVC 4x family preserves the SRAM during voltage drops e.g. at car engine start-up (cranking- and start-stop conditions). In this case the BVDD voltage drops from its typical value to the range of $V_{POR\_retention} \leq V_{BVDD} < V_{RET}$. Only the digital regulator is functional. In this mode, the peripherals and the Arm® core are kept in the reset state and no program is executed. Memory contents are retained while analog and digital functions are stopped (RETENTION mode).

If the supply voltage V_{BVDD} did not drop below $V_{POR\_retention}$ during RETENTION mode, the CPU starts from the reset vector and the RETENTION mode is signaled in the reset source status register. If V_{BVDD} drops below $V_{POR\_retention}$, then the POR signal is generated. In such a case the chip starts up in normal power-up mode without retaining the content of the volatile memories (SRAM and RAM layer of NVRAM).

4.2. Voltage Regulators

The HVC 4x family features a 5V pre-regulator which generates an intermediate voltage that is used by internal linear regulators to supply the different voltage domains.

4.3. Operating Modes

In order to offer a flexible solution in terms of high system performance and low current consumption, the HVC 4x family provides several operating modes:

– ACTIVE mode, in which all features are available and the CPU is clocked at selectable speed.

– RETENTION mode, in which the CPU and the peripherals are reset and the RAM content is preserved.

– Power-saving modes (IDLE and SLEEP), in which only few parts of the system are active to achieve low current consumption. An activity on the LIN bus can wake-up the system from IDLE or SLEEP. In addition the wake-up timer or an over/undervoltage condition on the BVDD or MON pin can be used as wake-up source from IDLE.

– THERMAL SHUTDOWN mode, in which only a few modules of the device are active to achieve a minimum of current consumption and to avoid malfunction during over-temperature condition.

– OVERVOLTAGE mode, in which all features are available but the charge pump is switched off automatically. It is in the responsibility of the application SW to reduce the current consumption of the chip in order to meet the thermal budget of the device, and it is recommended to switch off the MOUT ports within the BVDD_OV interrupt service routine.

4.4. Temperature Monitoring

The HVC 4x family features two overtemperature detection units to monitor the junction temperature inside the chip for overtemperature protection and one temperature sensor for the purpose of a controlled return from a Thermal Shutdown (TSD). The sensors are placed close to the power-bridges, where most of the power in the device is dissipated.

An additional linear temperature sensor is connected to the ADC to provide junction temperature information to the application SW. By polling the corresponding channel of the ADC, the application SW can continuously monitor the junction temperature and react on rising temperatures, e.g. by switching-off modules or reducing the CPU clock. If the temperature exceeds a certain threshold the TSD logic will invoke a TSD reset to protect the device from being thermally destroyed.

Note The TSD is a device protection mechanism for exceptional failure conditions only. The application SW has to take care that T_J does not exceed the shut-down temperature T_{TSD}(min).

4.5. Core

The HVC 4x family features an Arm® Cortex®-M3 core (revision r2p1) which is an industry-leading 32-bit RISC processor, widespread in the automotive industry. The Arm Cortex-M3 is based on a Harvard architecture with a 3-stage pipeline and supports an address space of 4 Gbyte. It executes the Thumb®-2 instruction set for optimal performance and code size, including division and single-cycle multiply, and reaches a high performance of 1.25 DMIPS/MHz at zero wait-states (Dhrystone 2.1).

4.5.1. Core Extensions

As the Arm Cortex-M3 is targeting a wide range of applications, the processor is based on a modular concept which includes fixed (basic) components (e.g. Arm core, NVIC) as well as optional core extensions listed below. The configuration for HVC 4x family is as follows:

- NVIC: up to 23 IRQs, 8 priority levels
- DAP: AHB-AP & SW-DP
- Serial wire viewer
- Three data watchpoints
- Flash patch: 8 breakpoint comparators

4.5.2. Debug Interface

The Arm Cortex-M3 includes a Debug Access Port (DAP), which is used to connect a Debug Port (DP) to the Arm core to allow external access by a debugger.

For the HVC 4x family the Serial Wire Debug Port (SW-DP) interface is implemented. For the debug interface two dedicated pins, SCK (clock input), and SDA (bidirectional data IO) are reserved, which are not multiplexed with any alternative functions.

4.5.3. Read-Out Protection

The HVC 4x family can be protected against unauthorized access by disabling the debug interface via a configuration bit in the customer area of the NVRAM. The debug interface can be re-enabled only by TDK-Micronas (e.g. for failure analysis) or by code inside the customer application SW.

4.5.4. Memory Protection Unit

The HVC 442xF double memory (64 KB Flash) versions feature an MPU (Memory Protection Unit) which divides the memory map into separate regions. Each of them is controlled by the MPU via location, size, memory attributes, and access permissions. By providing access permission bits, the Region Access Control Registers control the access to the corresponding memory regions. Access to an area without required permission does result in raising a MemManage fault. Without programming and enabling the MPU, the system behavior is exactly the same compared to HVC 422xF.

More details are included in the User Guide of HVC 4x Family. Original information can be found in the “Arm®v7-M Architecture Reference Manual”, which is the information base around the MPU implemented in the HVC 4x Family.

4.6. Clock System

There are two independent on-chip RC oscillators and a clock input for the Arm® debug interface. The main oscillator is combined with an EMI reduction module and provides the operating clock (f_{MAIN}) to the system. In parallel the clock of the auxiliary oscillator (f_{AUX}) can be used to clock the window watchdog for supervising both RC oscillators or to generate a time triggered wake-up event from IDLE mode. Clock dividers inside the peripherals are used to derive the internal clocks for the analog and digital modules from f_{MAIN}.

4.6.1. Clock Supervision

A supervision of both RC oscillator clocks (f_{MAIN} and f_{AUX}) can be achieved using the window watchdog (WWDG). The WWDG is clocked with f_{AUX} and requires continuous triggering by the CPU (running at f_{CPU} which is derived from f_{MAIN}) within a dedicated time window. If the triggering is not done within the valid trigger window the device will be reset.

4.6.2. EMI Reduction Module (ERM)

The ERM reduces electromagnetic radiation that might cause interference to other electronic equipment. The reduction of the radiation is done by applying a predefined modulation on the frequency of the main oscillator.

Without modulation, the noise emission of the chip is concentrated at discrete frequencies. The controlled modulation of the oscillator introduced by the ERM distributes the power of the emission over a defined frequency range, thus reducing the power spectral density at the oscillator frequency and its harmonics.

4.7. Bus System

The on-chip bus system of the HVC 4x family is based on the Advanced Microcontroller Bus Architecture (AMBA®) which is an open standard defined by Arm. Within the bus system, the Arm Cortex-M3 is the only master and therefore initiates every read/write transfer.

4.8. Memory

The HVC 4x family features several on-chip memory blocks to provide high flexibility. For storing instruction code a startup ROM and a flash memory are used whereas volatile and non-volatile application data are stored in the SRAM or in the NVRAM respectively.

4.8.1. Memory Map

The Arm Cortex-M3 provides a fixed linear memory map with 4 Gbyte of addressable memory space. The internally predefined memory map specifies which bus interface is to be used when a memory location is accessed. In order to make it easier to port software the registers of all internal peripherals like Nested Vectored Interrupt Controller (NVIC) or Instruction Trace Module (ITM) have a fixed position in the memory map.

For the HVC 4x family the memory mapping is aligned to the Arm recommendations for integrating a Cortex-M3 core in a SoC design.

4.8.2. Startup ROM

The HVC 4x family contains a startup ROM with the size of 1024 byte, organized as a 256-word by 32-bit array. It is used to store the start-up sequence which is executed after a reset, the default interrupt table and flash utility functions that can be used by the application SW. The memory content is fixed by design and cannot be reprogrammed in application.

4.8.3. Flash Memory

The HVC 422xF devices contain one block of flash memory which has the size of 32 KB and is organized as an 8192-word by 32-bit array. The HVC 442xF flash memory is organized in two blocks with the size of 32 KB each and is organized as a two-times 8192-word by 32-bit array. It is used to store the application SW and can be reprogrammed in system. For programming, each flash memory block is organized in 256 pages of 128 byte and for erasing in 16 sectors of 2 KB. Each block can only be programmed page by page while erasing is performed either sector by sector or the entire flash memory at once.

The flash memory is able to detect and to correct a single bit error within a 32-bit word. A double bit-error is detected during read of a 32-bit word. The error conditions are signalled in the flash status registers and can be configured as interrupt source.

4.8.4. SRAM

The on-chip SRAM has the size of 2 KB in the HVC 422xF - organized as a 512-word by 32-bit array, and 4 KB in the HVC 442xF - organized as a 1024-word by 32-bit array. It is used to store volatile application data, but can also be used to store and execute instruction code.

The content of the SRAM is preserved in ACTIVE, IDLE, RETENTION, and OVERVOLTAGE mode but will be lost after power-down, thermal shutdown, and in SLEEP mode.

4.8.5. NVRAM

The on-chip NVRAM has the size of 512 byte (448 byte available for customer use) and is organized as a 128-word by 32-bit array. It is used to store non-volatile application data like trimming values or error counters. The NVRAM consists of a 512 byte RAM module and an EEPROM of the same size.

Before entering power-down mode the non-volatile data can be preserved in the EEPROM by a STORE sequence which has to be triggered intentionally by the application SW. After power-on reset the memory content of the EEPROM is automatically transferred to the RAM (RECALL sequence).

4.9. Power-Bridges / MOUT Ports

For the control of BLDC, BDC or stepper motors the HVC 4x family provides the following features:

– Six integrated N/N-channel half-bridges, each connected to one MOUT port for direct motor operation, respectively switching of inductive loads. Each half-bridge consists of two N-channel power FETs for switching high-current loads to motor ground (MVSS0/1) or positive motor supply (MVDD0/1)

– Internal cross-current protection by gate-voltage monitoring

– High-side N-channel FETs are driven by gate-drivers with internal charge-pump

– Overcurrent detection for each low-side and high-side FET and automatic overcurrent shut-down (high impedance) of either all half-bridges or the affected half-bridge only

– Interrupt source for overcurrent shutdown

– Integrated resistor network for internal reference voltage generation and signal conditioning of MOUT voltages (e.g. BEMF detection for sensor-less BLDC control or commutated bipolar stepper motor driving)

– Integrated current sensors on all low-side FETs to support phase current limitation (e.g. closed-loop current control for bipolar stepper motor application)

– Switched off automatically during SLEEP, RETENTION and TSD mode

The MOUT ports are driven by N/N-channel half-bridges and are implemented for direct motor operation (e.g. brush-type and brushless DC motors or bipolar stepper motors). They can switch high-currents on inductive loads without external components.[1)] Each of the half-bridges consists of two N-channel power FETs which are used as a low-side switch[2)] to the motor ground (MVSS0/1) and as a high-side switch to motor supply (MVDD0/1), respectively. The power FETs are driven by internal gate-drivers which are controlled by the EPWM module.

A diagnosis block monitors the gate voltages of the power FETs and provides a signal which is used in the EPWM module to implement the cross-current protection. Additionally, the currents flowing through the power FETs are monitored to detect an overcurrent condition which is evaluated in the EPWM module to either switch-off all six half-bridges or the affected half-bridge only as well as to generate an overcurrent interrupt.

[1)] For V_{BVDD} > 18 V it is recommended to turn off the power-bridge due to deactivated charge-pump.

[2)] It is recommended to use passive free-wheeling only on the low-side of the power-bridge. This is due to the power dissipation by a parasitic bipolar transistor which conducts free-wheeling currents to the substrate causing device heating. If high-side passive free-wheeling shall be used it is recommended to apply external free-wheeling diodes to the respective MOUT port.

4.9.1. BLDC Motor Control

The three phases of a BLDC motor are connected to the six MOUT ports as illustrated in Fig. 2–2 on page 22. The voltage levels at the MOUT ports are scaled down and connected to the BEMF comparators. A resistive network connected to the MOUT ports can be configured by multiplexers to generate a virtual starpoint voltage as a reference for the BEMF comparators (refer to Fig. 1–1 on page 13). For the control of sensorless BLDC motors, the BEMF comparators can be used to detect the BEMF zero-crossing of the floating motor phase.

4.9.2. Stepper Motor Control

The two coils of a bipolar stepper motor are connected to four of the six MOUT ports as illustrated in Fig. 2–3 on page 23. The ports MOUT0 to MOUT3 are internally connected to resistive voltage dividers providing the scaled down MOUTx voltages to the corresponding BEMF comparators.

The internal current through the low-side switches of the ports MOUT0 to MOUT3 can be measured for the purpose of current controlled stepper motor driving. The currents are compared to individual 8-bit DAC current reference values. The EPWM module switches off the corresponding bridge if the current exceeds the given reference value. The bridge ground pins of the MOUT ports (MVSS0 and MVSS1) have to be grounded externally. Optionally, an external shunt resistor can be connected between MVSS0/1 and system ground to measure the total motor current by the ADC.

4.9.3. BEMF Comparators

The BEMF comparators can be used to acquire the voltage induced by the back electromotive force on a floating BLDC or stepper motor phase to build up a sensorless motor control application without external components.

The following features are provided:

– Configurable to detect the zero-crossing of the BEMF voltage in an open motor phase of either a BLDC or a stepper motor.
– Configurable to compare a phase current with an 8-bit programmable reference current to implement current limit feature.
– Interrupt generation on every change on the comparator output.
– Fast reaction time for BEMF evaluation in BLDC and stepper motor applications.

4.10. Ports

4.10.1. Low-Voltage General-Purpose I/O (LGPIO)

– Digital output: push-pull or open drain
– Digital input: floating, weak pull-down or weak pull-up
– Analog input: Four ports with single-ended analog input functionality and two ports configurable as differential analog input. The differential input is not calibrated and has only limited accuracy.
– Alternative output and input functions selectable
– Port interrupt on rising and/or falling edges

4.10.2. LIN Port

– Physical LIN interface according LIN 2.x
– Support of LIN Auto-Addressing
– Overcurrent protection
– Multiple I/O sources selectable (PWMIO, LIN-UART, Timer 0, LIN_DO)
– Wake-port function (in SLEEP and IDLE mode)
– Selectable slew-rate
– Support of LIN tx dominant time-out function to switch off the transmitter if the LIN bus is stuck at dominant level (according OEM requirement specification “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications v1.3” from May 4, 2012)

The LIN port is mainly used to drive the output via the physical LIN interface for the communication via the LIN bus. Alternatively, it can be used for PWM communication together with the PWMIO module.

4.10.3. High-Side BVDD Switch (HSBVDD)

The HVC 4x family features a HSBVDD port which is composed of a high-side switch to V_{BVDD} equipped with an overcurrent protection circuitry. It is designed to supply external devices, such as hall sensors. If the output current exceeds the specified overcurrent limit, the HSBVDD port is switched off automatically. The occurrence of an overcurrent condition may trigger an interrupt.

4.10.4. MON Pin

The MON pin is a high voltage analog input pin to monitor the battery supply voltage. For connection to the battery supply refer to Fig. 2–2 on page 22 and Fig. 2–3 on page 23.

4.11. Peripherals

The HVC 4x family features several peripherals to offer an optimized solution for typical BLDC, BDC, and stepper motor applications.

4.11.1. ADC

– 12-bit resolution

– Fast conversion time of 1 µs

– Input multiplexer with 13 analog channels: LGPIO0 to LGPIO3 single-ended, LGPIO8/9 differential, V_{BAT} at MON pin, V_{BVDD}, internal temperature sensor V_{TEMP}, motor current sensing via shunt resistor at MVSS0 and MVSS1, differential inputs STDA+/– and STDB+/– for stepper motor stall detection, differential input LIN Auto- Addressing

– Selectable trigger source for software-driven, event-driven or time-dependent start of the acquisition queue

– Operating clock derived from main oscillator

– Internal band-gap voltage reference $V_{REF-ADC}$

– Acquisition queue for automatic sequential acquisition of up to eight entries

– Programmable gain amplifier with four possible gain settings

– Eight 16-bit sign-extended data registers

– End of conversion and trigger collision interrupt

The analog-to-digital converter allows the conversion of an analog voltage in the range from $-V_{REF-ADC}$ to $+V_{REF-ADC}$. The reference voltage is derived from the internal band-gap.

The acquisition queue holds up to eight entries and is executed after a defined start condition. The entries contain the input source, the PGA gain setting and an entry enable flag. The converted values are stored in dedicated result registers. If all valid entries of the acquisition queue have been executed an interrupt indicates the end of the conversion.

4.11.2. Clock and Reset System Control

The HVC 4x family includes system control registers for the clock system configuration, ERM control, peripheral clock setup in debug mode, power-saving mode setup and interrupt generation (MON and BVDD over/undervoltage).

4.11.3. TIMER

– Two timer modules: TIM0 and TIM1
– Selectable input clocks: internal or external
– 16-bit input clock prescaler
– 16-bit timer counter
– Selectable operating modes: timer, compare or capture
– Optional buffering of prescaler, reload- and capture values
– Selectable output signal: static value, PWM signal or timer input signal

The HVC 4x family features two instances of the timer module (TIM0, TIM1) with identical implementation which operate independently from each other. The timer modules are based on a 16-bit input clock prescaler and a 16-bit timer counter.

The timers can be used e.g. to generate periodic interrupts, to generate PWM output signals or to measure the pulse length of input signals.

4.11.4. LIN-UART

– LIN 2.x compliant data link layer
– Full duplex in non-LIN mode
– 8-bit frames
– Parity: none, odd or even
– One or two stop bits
– Programmable inverters at transmit output and receive input
– Baud rate pre-scaler: adjustment accuracy <0.5% (for entire LIN bit-rate range)
– Interrupts: transmitted, form error, parity error, transmit error, break or synch detected, RX FIFO not empty, RX/TX FIFO fill level reached, RX/TX FIFO overrun, TX FIFO empty, RX/TX FIFO full
– Two independent 9-byte FIFOs for data reception and transmission
– Break/sync detection with automatic bit-rate adjustment in LIN mode
– Automatic LIN-header reception

The LIN-UART is a general purpose UART with enhanced features to unburden the CPU from LIN communication. It is a full duplex UART which can handle 8-bit telegrams with or without odd or even parity and one or two stop bits. The bit timing logic allows to adjust the necessary bit rate in small steps in order to synchronize to the LIN bit rate with a minimum residual error. Two 9-byte FIFOs are available for data reception and transmission. A bit-rate adjustment logic can be used for automatic adjustment of the UART bit rate to the bit rate of the LIN master. The enhanced features are optimized for the LIN slave mode.

The LIN-UART is compliant to the OEM requirement specification “Hardware Requirements for LIN, CAN and FlexRay Interfaces in Automotive Applications v1.3” from May 4, 2012.

4.11.5. PWMIO

– Periodic input signal measurement (1 Hz to 10 kHz)
– Interrupt source (falling or rising edge, counter overflow, and end of period)
– Measurement of high- and low-time of the input signal
– Input deglitch filter with 3 µs selectable
– PWM signal output (single pulse, periodic, static low or high) at LIN pin or LGPIO alternative output (refer to Table 2–2)
– Two independent 14-bit counters for input capture and output compare

The PWMIO module supports a bidirectional communication via a PWM protocol with minimum CPU interaction. It can generate PWM output signals and measure the high- and low-time of an applied PWM input signal. The input and output signals of the PWMIO module are routed to the LIN port and to the LGPIO ports (as alternative functions).

4.11.6. Enhanced PWM (EPWM)

– Support of BLDC, BDC or stepper motor control
– Three EPWM control modules with programmable PWM period, PWM duty cycle and ADC trigger signal
– Center- or edge-aligned PWM signal generation
– Multiplexers for each half-bridge to select control signals for high-side and low-side switches
– Overcurrent and cross-current protection for each MOUT half-bridge
– Current limit mode with PWM duty cycle capture
– Three interrupt lines, each with five interrupt sources: end-of-period, compare value matched, trigger value matched, capture event, overcurrent
– Programmable minimum on-time of PWM signal
– Buffered control registers
– Programmable slew rate for the half-bridges

The HVC 4x family features an enhanced PWM (EPWM) module with 12-bit resolution to generate the digital control signals for the half-bridges that drive the MOUT ports. It is optimized for BLDC, brush-type DC and bipolar stepper motor control supporting open loop control modes (fixed voltage / fixed current) as well as closed loop current control with minimum amount of SW interaction.

4.11.7. Capture Compare Unit (CAPCOM)

– Processing of up to three channels in parallel
– 16-bit clock prescaler
– 16-bit free running CAPCOM counter
– 16-bit capture and compare registers for each channel
– Input capture event on rising, falling, or both edges
– Advanced capture mode with input pattern compare
– Optional buffering for configuration registers
– Three separately configurable output signals (static at logical '0', toggle on compare and/or overflow events)
– One interrupt line for each CAPCOM channel triggered by: overflow, compare, capture, capture overflow events; additional right / wrong pattern detection event for channel 0

The HVC 4x family features a capture-compare unit (CAPCOM) which is optimized to capture and process up to three channels in parallel, e.g. three hall sensor signals for sensor-based six-step BLDC motor control. In parallel the compare feature can be used to generate up to three output signals which are routed as alternative function to LGPIO ports.

4.11.8. SPI

– 4-line interface (CSN, SCK, MISO, MOSI), full-duplex
– Master operation only
– Programmable bit rate from 78.125 kHz up to 2.5 MHz
– Programmable clock phase and polarity
– 8-, 16-, 24-, and 32-bit data frames supported by HW chip select (CSN)
– Chip Select (CSN) generation by HW or SW
– Programmable order of data bits (MSB or LSB first)
– Receive and transmit FIFOs with 8 x 8 bit each, organized according to the data frame width
– Interrupt generation at RX/TX events and FIFO flags

The SPI module provides a serial input and output link to external hardware, e.g. an EEPROM.

4.11.9. Digital Watchdog (DWDG)

– 16-bit down counter

– Counter clock selectable

– Programmable trigger time

– Enabled by NVRAM setting or application SW

The digital watchdog module is used to supervise the program flow. A failure of the program flow that prevents retriggering the watchdog within a configurable time will generate a reset. The occurrence of the reset is stored in the reset status register and so the application SW can distinguish between a DWDG reset and any other reset source and thus react accordingly.

4.11.10. Window Watchdog (WWDG) and Wake-Up Timer

– Auxiliary oscillator as clock source

– Trigger window adjustable from 100% to 0% of the counter period

– Counter clock selectable

– Can be used as wake-up timer in IDLE mode

– Wake-up time adjustable from $256/f_{AUX}$ to $32768/f_{AUX}$ (typ. 7.3 ms to 936 ms)

– Enabled by NVRAM setting or application SW

The window watchdog module is used to supervise the program flow and the clocks generated by the main oscillator and the auxiliary oscillator. A failure of the program flow or an oscillator malfunction that prevents continuous triggering of the watchdog within a configurable time window will generate a reset. The occurrence of the reset is stored in the reset status register. By evaluating the reset status register the application SW can distinguish between a WWDG reset and any other reset source to react accordingly.

In IDLE mode the WWDG module is configured as wake-up timer and can be used to generate periodic wake-up events. The WWDG counter works then as wake-up counter for periodic wake-up.

5. Document History

1. Data Sheet: “HVC 4222F-D2 Flex Servo-Drive for Direct Control of BLDC/BDC/Stepper Motors in High-Temperature Applications”, Edition March 23, 202, DSH000213_001EN. First release of the HVC 4222F-D2 data sheet.
2. Data Sheet: “HVC 4x Family Motor Drivers for Control of BLDC, BDC, or Stepper Motors”, July 9, 2021, DSH 000216_001EN. First release of the HVC 4x family data sheet.

   Major changes compared to the HVC 4222F-D2 data sheet:
   – Combined single and double memory versions - temperature grade 1 and grade 1^{+}.
   – Increased ADC linear input voltage range via single-ended LGPIO ports from 2.7 V to 3.3 V.

TDK-Micronas GmbH
Hans-Bunte-Strasse 19 · D-79108 Freiburg · P.O. Box 840 · D-79008 Freiburg, Germany
Tel. +49-761-517-0 · Fax +49-761-517-2174 · www.micronas.tdk.com