

MOSFET

OptiMOS™ 6 Power-Transistor, 40 V

Features

- N-channel, normal level
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- Optimized design for double side cooling
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

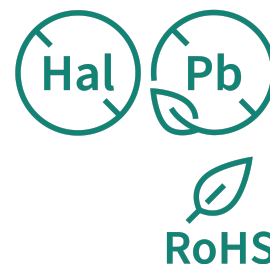
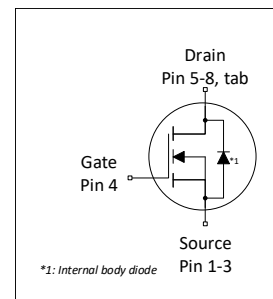
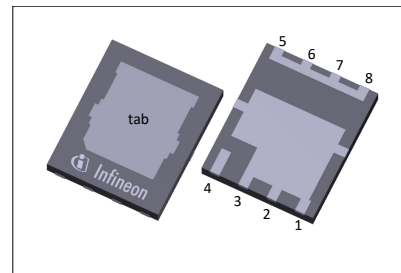
Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

| Parameter | Value | Unit |
|------------------|-------|------|
| V_{DS} | 40 | V |
| $R_{DS(on),max}$ | 0.49 | mΩ |
| I_D | 597 | A |
| Q_{oss} | 142 | nC |
| Q_G | 130 | nC |

PG-WHSON-8



| Type/Ordering Code | Package | Marking | Related Links |
|--------------------|------------|---------|---------------|
| IQD005N04NM6SC | PG-WHSON-8 | DA | - |



Table of Contents

| | |
|---|----|
| Description | 1 |
| Maximum ratings | 3 |
| Thermal characteristics | 4 |
| Electrical characteristics | 5 |
| Electrical characteristics diagrams | 7 |
| Package Outlines | 11 |
| Revision History | 13 |
| Trademarks | 13 |
| Disclaimer | 13 |

1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|--|-------------------|--------|------|-------------------------|------|---|
| | | Min. | Typ. | Max. | | |
| Continuous drain current ¹⁾ | I_D | - | - | 597 422 402 57 | A | $V_{GS}=10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=6\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=10\text{ V}$, $T_A=25\text{ °C}$, $R_{THJA}=50\text{ °C/W}$ ²⁾ |
| Pulsed drain current ³⁾ | $I_{D,pulse}$ | - | - | 2388 | A | $T_C=25\text{ °C}$ |
| Avalanche energy, single pulse ⁴⁾ | E_{AS} | - | - | 1115 | mJ | $I_D=50\text{ A}$, $R_{GS}=25\text{ }\Omega$ |
| Gate source voltage | V_{GS} | -20 | - | 20 | V | - |
| Power dissipation | P_{tot} | - | - | 333 3.0 | W | $T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=50\text{ °C/W}$ ²⁾ |
| Operating and storage temperature | T_j , T_{stg} | -55 | - | 175 | °C | - |

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for source connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|--|------------|--------|------|------|------|----------------------|
| | | Min. | Typ. | Max. | | |
| Thermal resistance, junction - case, bottom | R_{thJC} | - | - | 0.45 | °C/W | - |
| Thermal resistance, junction - case, top | R_{thJC} | - | - | 0.56 | °C/W | - |
| Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾ | R_{thJA} | - | - | 50 | °C/W | - |

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for source connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|----------------------------------|---------------|--------|--------------|--------------|---------------|---|
| | | Min. | Typ. | Max. | | |
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | 40 | - | - | V | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ |
| Gate threshold voltage | $V_{GS(th)}$ | 1.8 | 2.3 | 2.8 | V | $V_{DS}=V_{GS}$, $I_D=1449\text{ }\mu\text{A}$ |
| Zero gate voltage drain current | I_{DSS} | - | 0.1 10 | 1 100 | μA | $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$ |
| Gate-source leakage current | I_{GSS} | - | 10 | 100 | nA | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ |
| Drain-source on-state resistance | $R_{DS(on)}$ | - | 0.42 0.48 | 0.49 0.54 | m Ω | $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$ $V_{GS}=6\text{ V}$, $I_D=50\text{ A}$ |
| Gate resistance | R_G | - | 0.68 | - | Ω | - |
| Transconductance | g_{fs} | 185 | 370 | - | S | $ V_{DS} \geq 2 I_D $, $R_{DS(on)max}$, $I_D=50\text{ A}$ |

Table 5 Dynamic characteristics

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|--|--------------|--------|------|-------|------|--|
| | | Min. | Typ. | Max. | | |
| Input capacitance ⁶⁾ | C_{iss} | - | 9000 | 12000 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$ |
| Output capacitance ⁶⁾ | C_{oss} | - | 2900 | 3800 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$ |
| Reverse transfer capacitance ⁶⁾ | C_{rss} | - | 69 | 120 | pF | $V_{GS}=0\text{ V}$, $V_{DS}=20\text{ V}$, $f=1\text{ MHz}$ |
| Turn-on delay time | $t_{d(on)}$ | - | 15 | - | ns | $V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Rise time | t_r | - | 6 | - | ns | $V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Turn-off delay time | $t_{d(off)}$ | - | 42 | - | ns | $V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |
| Fall time | t_f | - | 9 | - | ns | $V_{DD}=20\text{ V}$, $V_{GS}=10\text{ V}$, $I_D=50\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$ |

⁶⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁷⁾

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|------------------------------------|-------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate to source charge | Q_{gs} | - | 30 | - | nC | $V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge at threshold | $Q_{g(th)}$ | - | 21 | - | nC | $V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate to drain charge ⁸⁾ | Q_{gd} | - | 18 | 26 | nC | $V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Switching charge | Q_{sw} | - | 27 | - | nC | $V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |

Table 6 Gate charge characteristics ⁷⁾

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---------------------------------|----------------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Gate charge total ⁸⁾ | Q_g | - | 130 | 163 | nC | $V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate plateau voltage | V_{plateau} | - | 3.3 | - | V | $V_{DD}=20\text{ V}$, $I_D=50\text{ A}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Gate charge total, sync. FET | $Q_{g(\text{sync})}$ | - | 122 | - | nC | $V_{DS}=0.1\text{ V}$, $V_{GS}=0\text{ to }10\text{ V}$ |
| Output charge ⁸⁾ | Q_{oss} | - | 142 | 189 | nC | $V_{DS}=20\text{ V}$, $V_{GS}=0\text{ V}$ |

⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

| Parameter | Symbol | Values | | | Unit | Note/ Test Condition |
|---------------------------------------|----------------------|--------|------|------|------|---|
| | | Min. | Typ. | Max. | | |
| Diode continuous forward current | I_S | - | - | 294 | A | $T_C=25\text{ °C}$ |
| Diode pulse current | $I_{S,\text{pulse}}$ | - | - | 2388 | A | $T_C=25\text{ °C}$ |
| Diode forward voltage | V_{SD} | - | 0.78 | 1.0 | V | $V_{GS}=0\text{ V}$, $I_F=50\text{ A}$, $T_j=25\text{ °C}$ |
| Reverse recovery time ⁹⁾ | t_{rr} | - | 58 | 116 | ns | $V_R=20\text{ V}$, $I_F=25\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ |
| Reverse recovery charge ⁹⁾ | Q_{rr} | - | 79 | 158 | nC | $V_R=20\text{ V}$, $I_F=25\text{ A}$, $di_F/dt=100\text{ A}/\mu\text{s}$ |
| Reverse recovery time ⁹⁾ | t_{rr} | - | 29 | 58 | ns | $V_R=20\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$ |
| Reverse recovery charge ⁹⁾ | Q_{rr} | - | 221 | 442 | nC | $V_R=20\text{ V}$, $I_F=50\text{ A}$, $di_F/dt=1000\text{ A}/\mu\text{s}$ |

⁹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

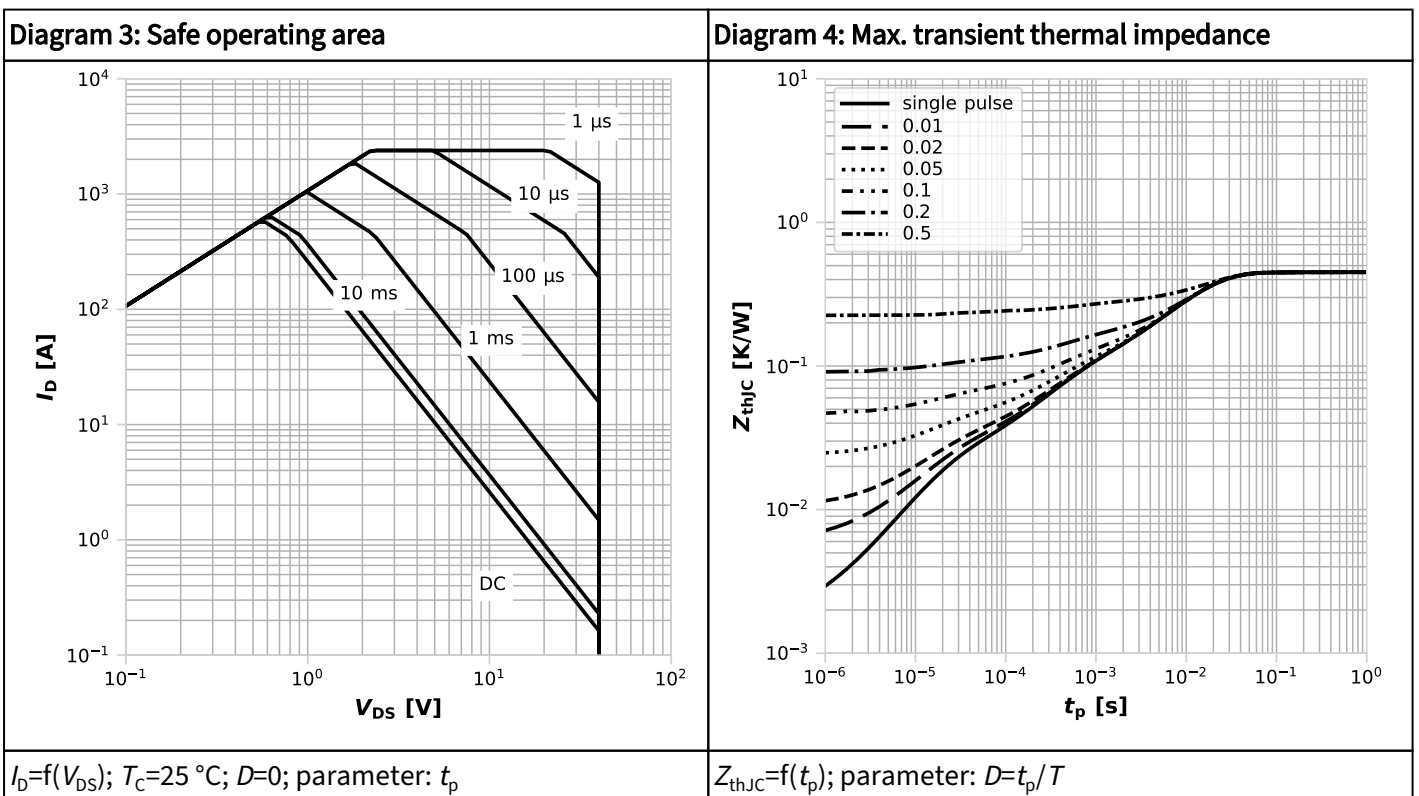
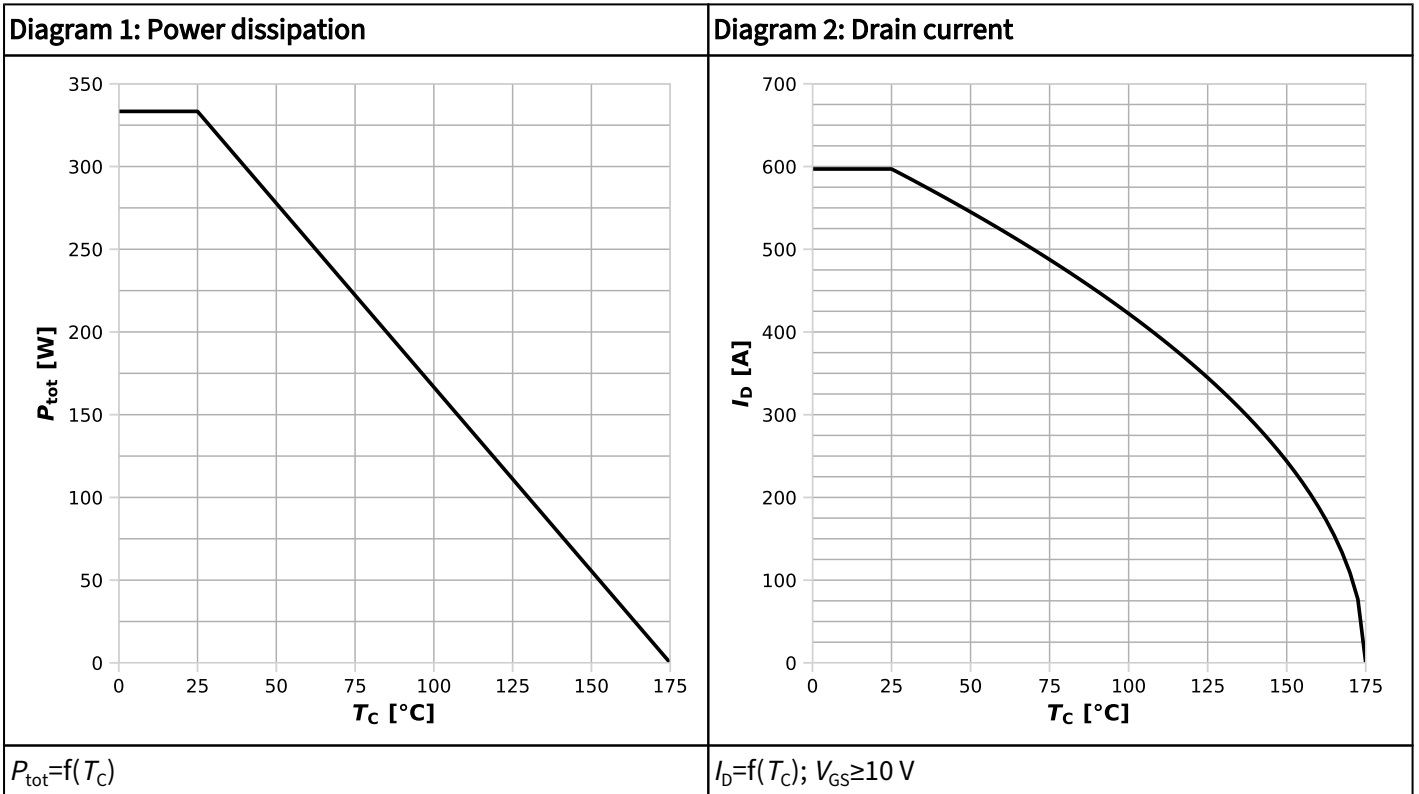
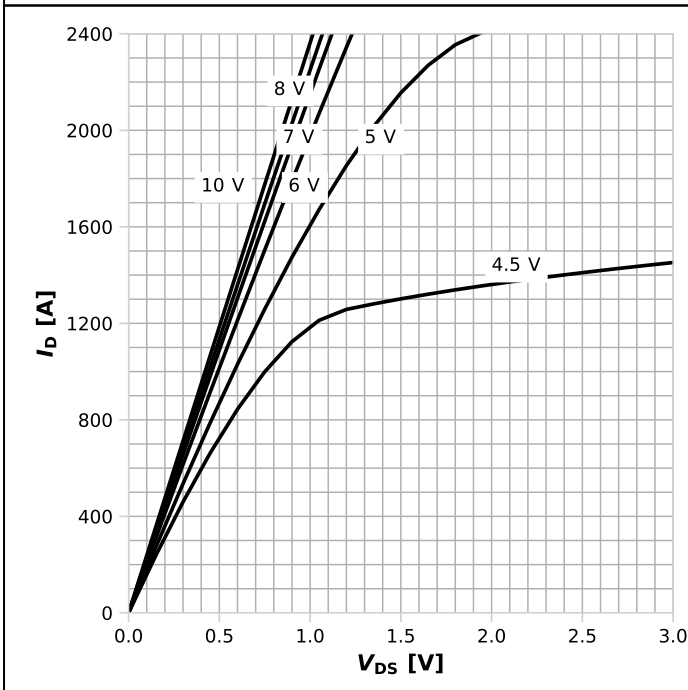
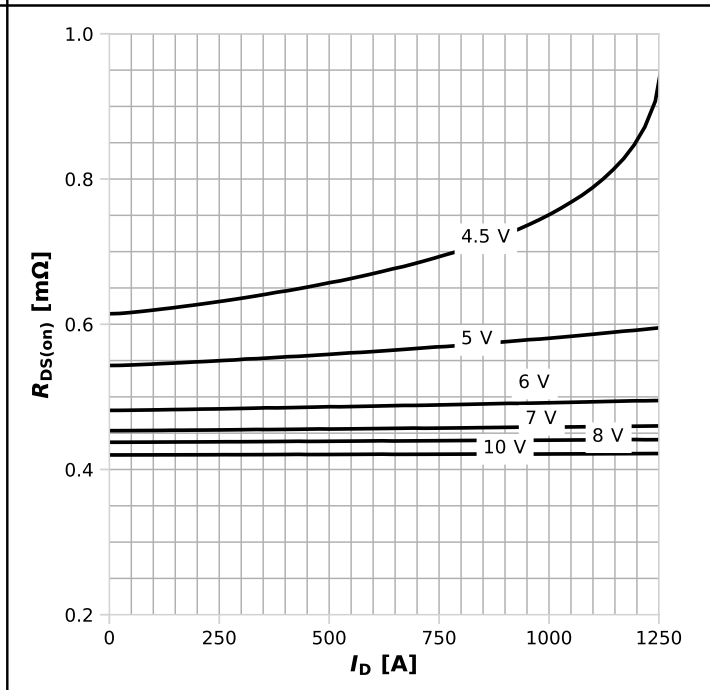


Diagram 5: Typ. output characteristics



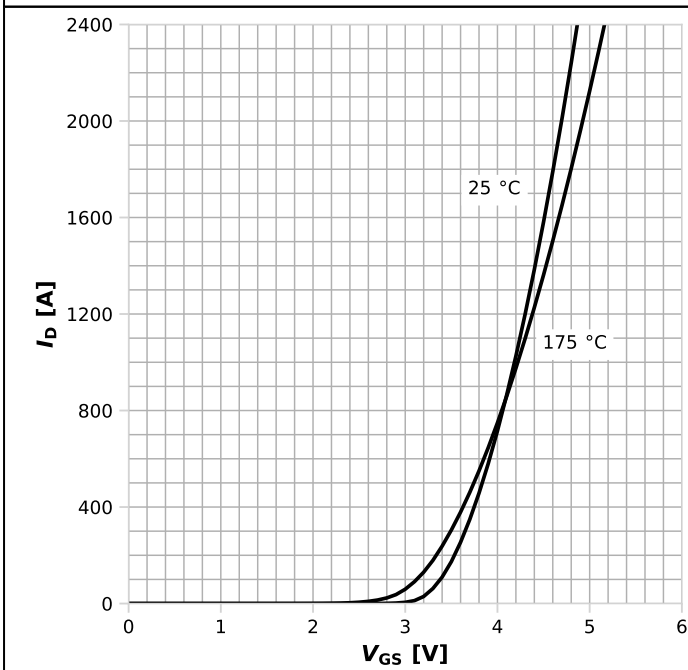
$I_D = f(V_{DS})$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



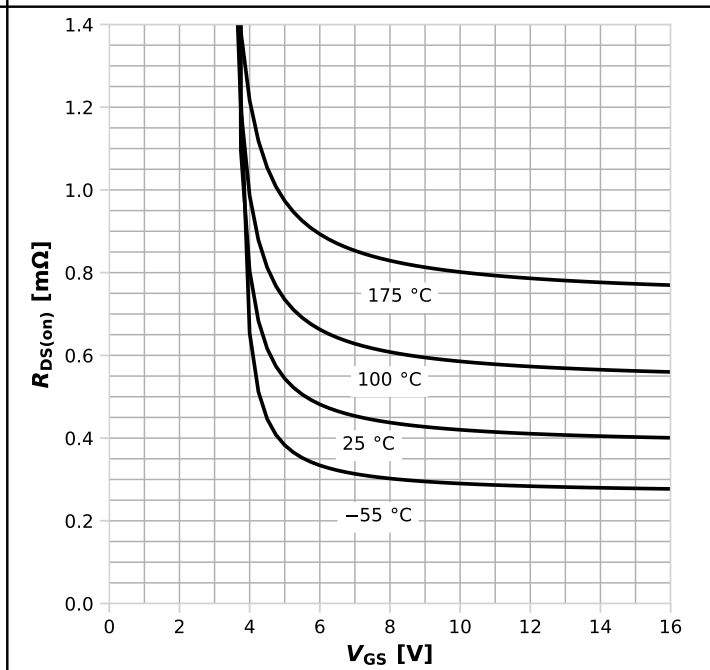
$R_{DS(on)} = f(I_D)$, $T_j = 25\text{ °C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



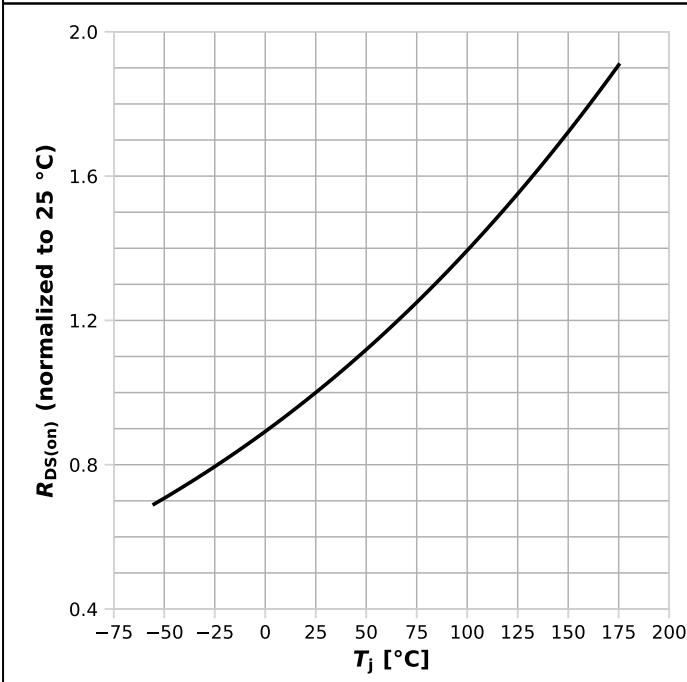
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



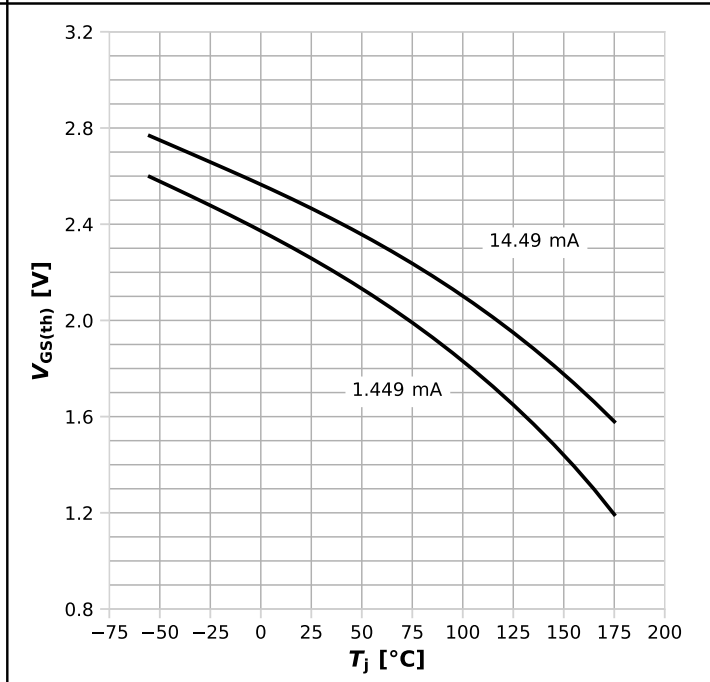
$R_{DS(on)} = f(V_{GS})$, $I_D = 50\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



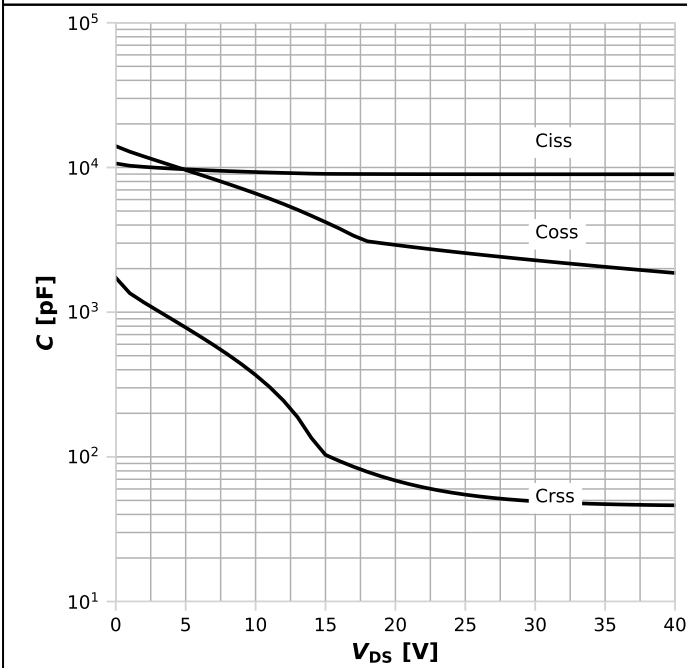
$R_{DS(on)}=f(T_j), I_D=50\text{ A}, V_{GS}=10\text{ V}$

Diagram 10: Typ. gate threshold voltage



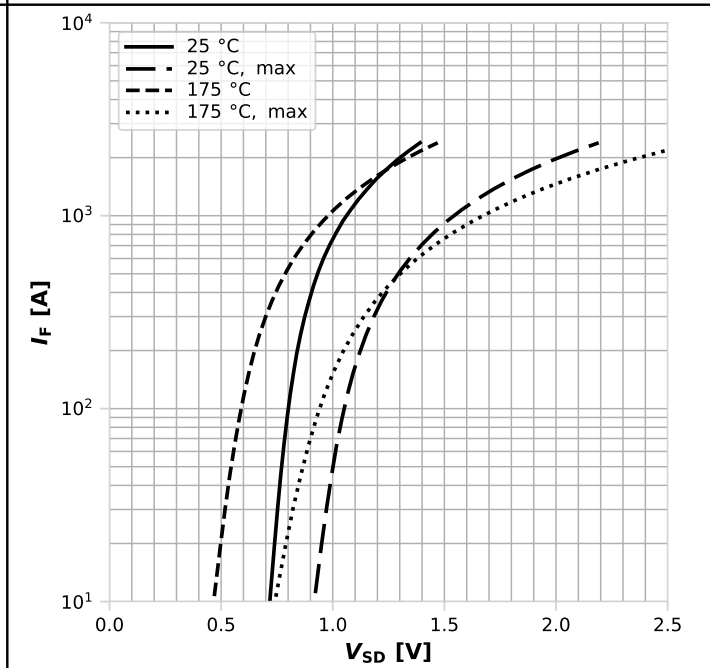
$V_{GS(th)}=f(T_j), V_{GS}=V_{DS};$ parameter: I_D

Diagram 11: Typ. capacitances



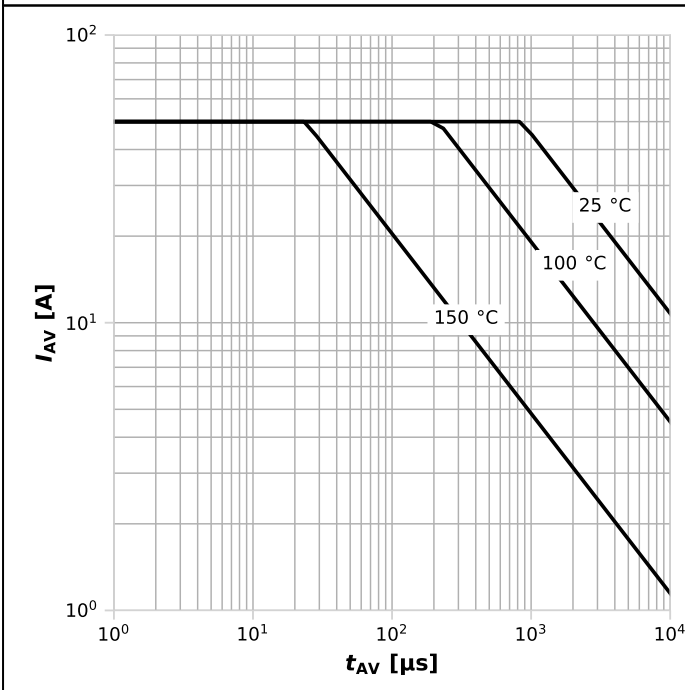
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}$

Diagram 12: Forward characteristics of reverse diode



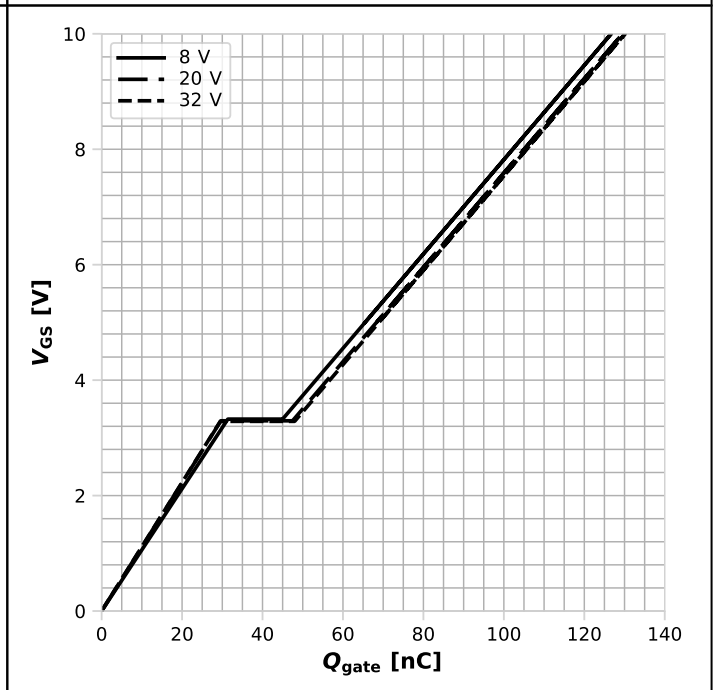
$I_F=f(V_{SD});$ parameter: T_j

Diagram 13: Avalanche characteristics



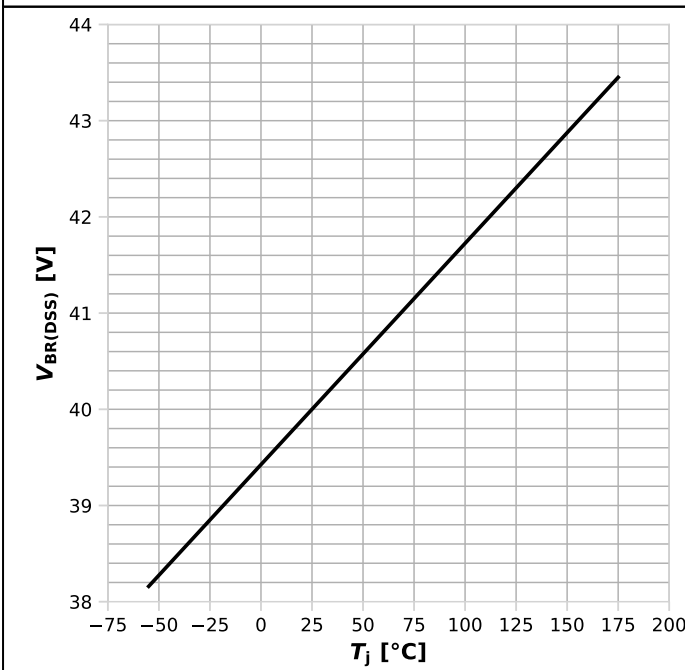
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



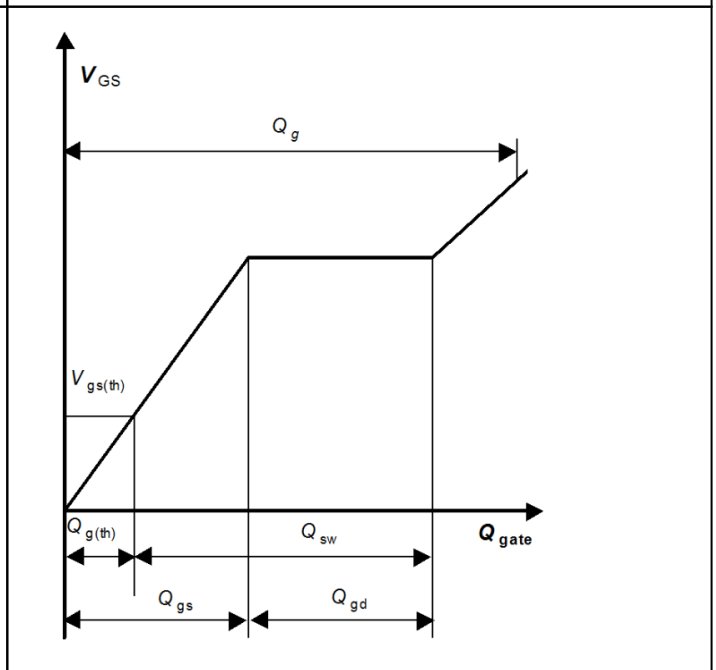
$V_{GS}=f(Q_{gate}), I_D=50 \text{ A pulsed}, T_j=25 \text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



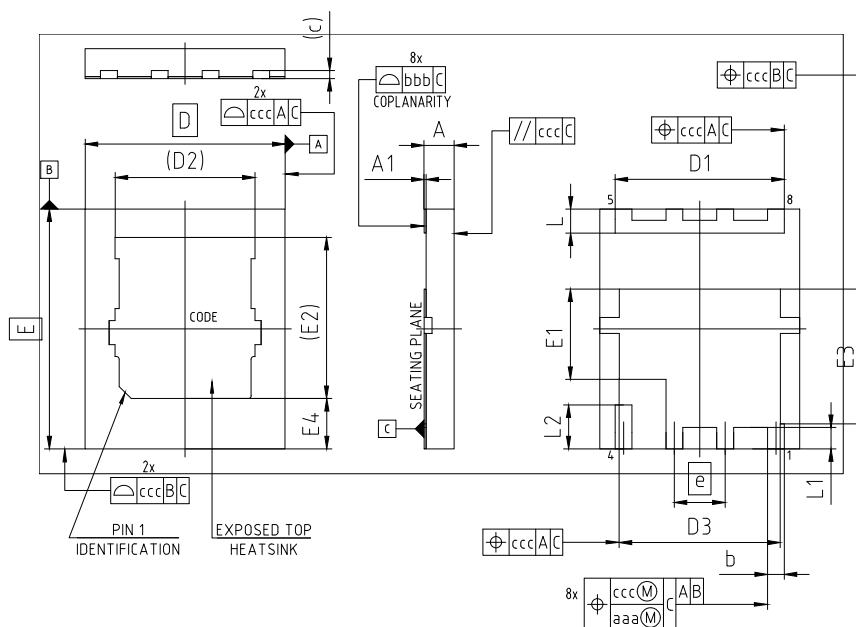
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

Gate charge waveforms



-

5 Package Outlines



| PACKAGE - GROUP NUMBER: PG-WHSON-8-U02 | | | | | |
|---|-------------|------|------------|-------------|------|
| DIMENSIONS | MILLIMETERS | | DIMENSIONS | MILLIMETERS | |
| | MIN. | MAX. | | MIN. | MAX. |
| A | 0.55 | 0.75 | e | 1.27 | |
| A1 | 0.00 | 0.05 | L | 0.50 | 0.70 |
| b | 0.32 | 0.52 | L1 | 0.44 | 0.64 |
| c | 0.20 | | L2 | 1.00 | 1.20 |
| D | 5.00 | | aaa | 0.05 | |
| D1 | 4.13 | 4.33 | bbb | 0.08 | |
| D2 | 3.50 | | ccc | 0.10 | |
| D3 | 3.93 | 4.13 | | | |
| E | 6.00 | | | | |
| E1 | 2.16 | 2.36 | | | |
| E2 | 4.03 | | | | |
| E3 | 3.28 | 3.48 | | | |
| E4 | 1.16 | 1.36 | | | |

NOTE: DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

Figure 1 Outline PG-WHSON-8, dimensions in mm

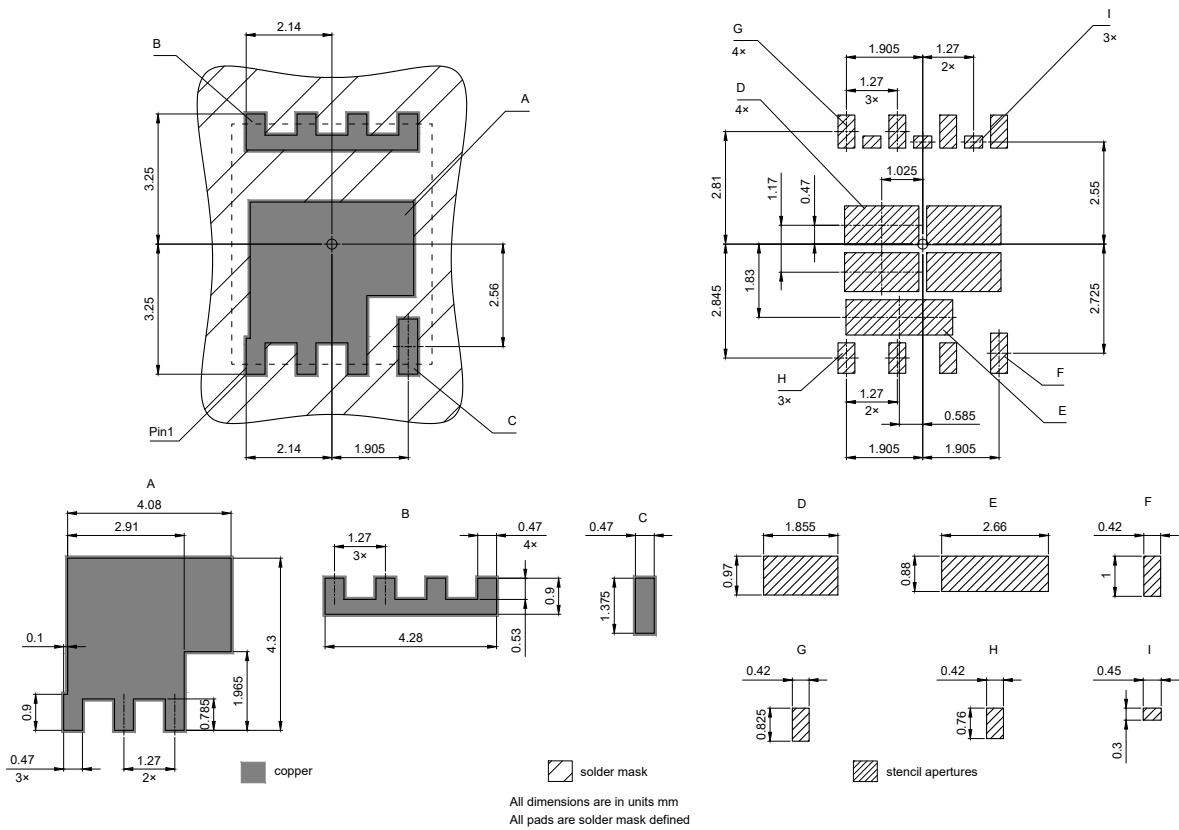


Figure 2 Footprint Drawing PG-WHSON-8, dimensions in mm

Revision History

IQD005N04NM6SC

Revision 2024-10-02, Rev. 2.2

Previous Revision

| Revision | Date | Subjects (major changes since last revision) |
|----------|------------|--|
| 2.0 | 2024-06-13 | Release of final |
| 2.1 | 2024-07-16 | Updated max Rdson |
| 2.2 | 2024-10-02 | Update package drawing and diagram circuit |

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