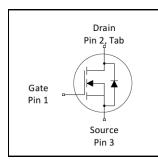
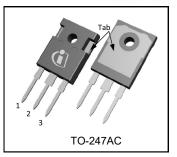
# IRFP90N20DPbF



V <sub>(BR)DSS</sub>	200V
R <sub>DS(on)</sub> max.	0.023Ω
ID	94A©





# Application

• High frequency DC-DC converters

# Benefits

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C<sub>OSS</sub> to Simplify Design
- Fully Characterized Avalanche Voltage and Current
- Lead-Free

Base part number	Package Type	Standard Pack		Orderable Part Number
Base part number	i dekage i ype	Form	Quantity	Orderable Fart Number
IRFP90N20DPbF	TO-247AC	Tube	25	IRFP90N20DPbF

Symbol	Symbol Parameter		Units	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	946		
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	66	Α	
I <sub>DM</sub>	Pulsed Drain Current ①	380		
P <sub>D</sub> @T <sub>C</sub> = 25°C	Maximum Power Dissipation	580	W	
	Linear Derating Factor	3.8	W/°C	
V <sub>GS</sub> Gate-to-Source Voltage		± 30	V	
E <sub>AS</sub> Single Pulse Avalanche Energy ②		1010	mJ	
I <sub>AR</sub> Avalanche Current ①		56	А	
E <sub>AR</sub>	Repetitive Avalanche Energy ①	58	mJ	
dv/dt	Peak Diode Recovery dv/dt③	6.7	V/ns	
TJ	Operating Junction and	-55 to + 175		
T <sub>STG</sub> Storage Temperature Range			°C	
	Soldering Temperature, for 10 seconds (1.6mm from case)	300		
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)		

# **Thermal Resistance**

Symbol	Parameter	Тур.	Max.	Units
$R_{ ext{ heta}JC}$	Junction-to-Case		0.26	
$R_{ ext{ heta}CS}$	Case-to-Sink, Flat, Greased Surface	0.24		°C/W
$R_{ ext{ heta}JA}$	Junction-to-Ambient		40	



# Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	200			V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250µA
$\Delta V_{(BR)DSS} / \Delta T_J$	Breakdown Voltage Temp. Coefficient		0.24		V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance			0.023	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 56A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0		5.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
gfs	Forward Trans conductance	39			S	V <sub>DS</sub> = 50V, I <sub>D</sub> = 56A
1	Drain-to-Source Leakage Current			25	μA	V <sub>DS</sub> = 200V, V <sub>GS</sub> = 0V
I <sub>DSS</sub>				250	μΑ	V <sub>DS</sub> = 160V,V <sub>GS</sub> = 0V,T <sub>J</sub> =150°C
1	Gate-to-Source Forward Leakage			100	nA	V <sub>GS</sub> = 30V
IGSS	Gate-to-Source Reverse Leakage			-100	ПА	V <sub>GS</sub> = -30V

# Dynamic Electrical Characteristics @ $T_J = 25^{\circ}C$ (unless otherwise specified)

Q <sub>g</sub>	Total Gate Charge	 180	270		I <sub>D</sub> = 56A
Q <sub>gs</sub>	Gate-to-Source Charge	 45	67	nC	V <sub>DS</sub> = 160V
Q <sub>gd</sub>	Gate-to-Drain Charge	 87	130		V <sub>GS</sub> = 10V ④
t <sub>d(on)</sub>	Turn-On Delay Time	 23			V <sub>DD</sub> = 100V
t <sub>r</sub>	Rise Time	 160			I <sub>D</sub> = 56A
t <sub>d(off)</sub>	Turn-Off Delay Time	 43		ns	R <sub>G</sub> = 1.2Ω
t <sub>f</sub>	Fall Time	 79			V <sub>GS</sub> = 10V ④
C <sub>iss</sub>	Input Capacitance	 6040			V <sub>GS</sub> = 0V
Coss	Output Capacitance	 1070			V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	 170			f = 1.0MHz
C <sub>oss</sub>	Output Capacitance	 8350		pF	$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0MHz$
C <sub>oss</sub>	Output Capacitance	 420			$V_{GS} = 0V, V_{DS} = 160V, f = 1.0MHz$
C <sub>oss. eff.</sub>	Effective Output Capacitance	 870			V <sub>GS</sub> = 0V,V <sub>DS</sub> = 0V to 160V⑤

# **Diode Characteristics**

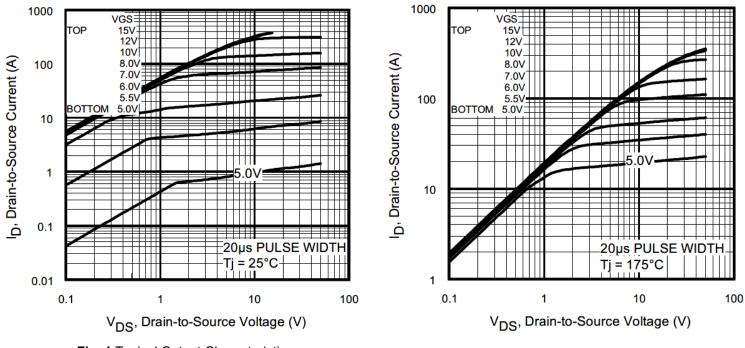
	Parameter	Min.	Тур.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)			94©		MOSFET symbol showing the
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①			380		integral reverse p-n junction diode.
$V_{SD}$	Diode Forward Voltage			1.5	V	T <sub>J</sub> = 25°C,I <sub>S</sub> = 56A,V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time		230	340	ns	T <sub>J</sub> = 25°C ,I <sub>F</sub> = 56A
Q <sub>rr</sub>	Reverse Recovery Charge		1.9	2.8	μC	di/dt = 100A/µs

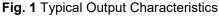
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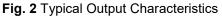
- ${\ensuremath{\mathbb O}}$  Repetitive rating; pulse width limited by max. junction temperature.
- @ Starting  $T_J$  = 25°C, L = 0.64mH,  $R_G$  = 25 $\Omega, \ I_{AS}$  = 56A.
- $\label{eq:ISD} \textcircled{3} \quad I_{SD} \leq 56A, \ di/dt \leq 470 A/\mu s, \ V_{DD} \leq V_{(BR)DSS}, \ T_J \leq 175^\circ C.$
- ④ Pulse width  $\leq$  300µs; duty cycle  $\leq$  2%.
- $\odot$  C<sub>oss</sub> eff. is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>
- © Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 90A.

# IRFP90N20DPbF









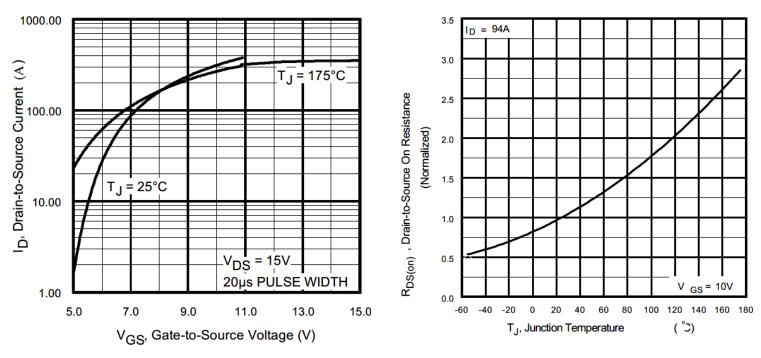
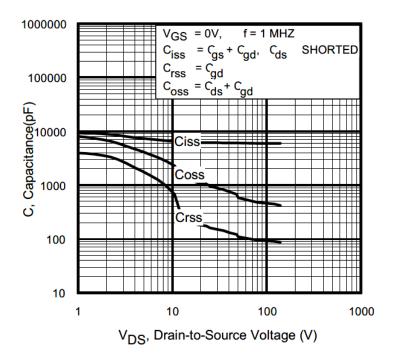
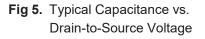


Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature







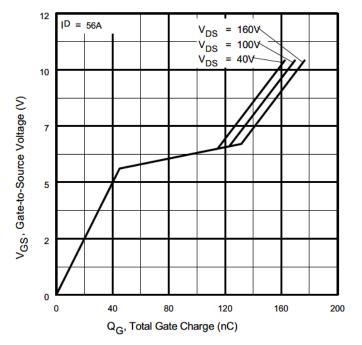
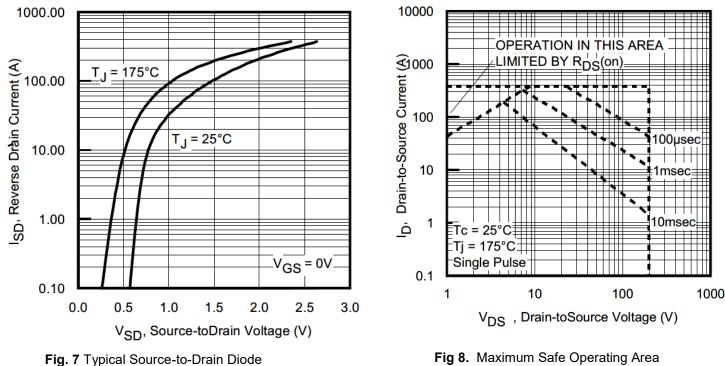


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage



Forward Voltage





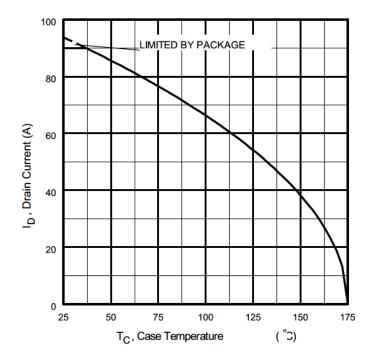


Fig 9. Maximum Drain Current vs. Case Temperature

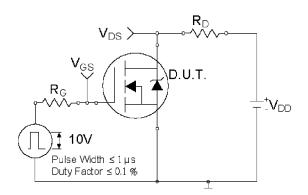


Fig 10a. Switching Time Test Circuit

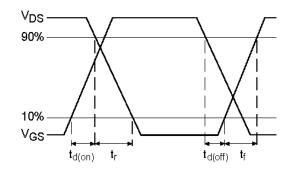
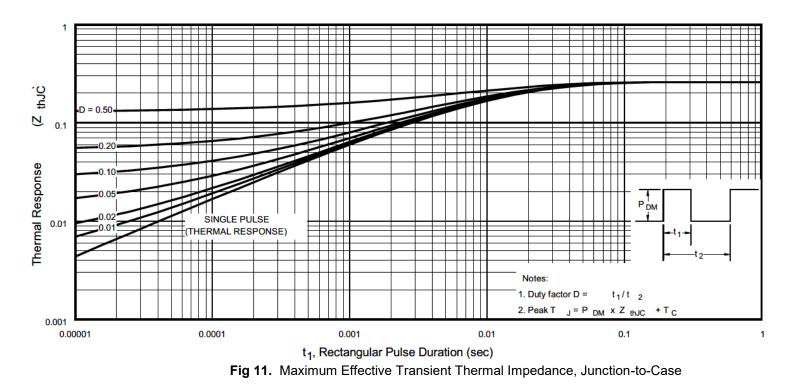


Fig 10a. Switching Time Waveforms





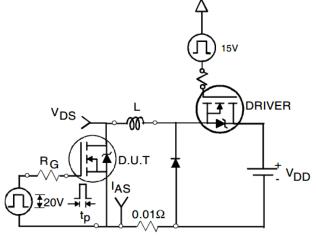


Fig. 12a. Unclamped Inductive Test Circuit

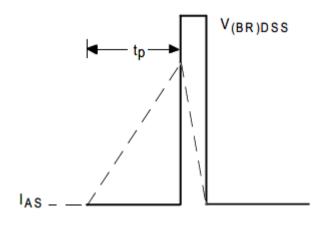


Fig. 12b. Unclamped Inductive Waveforms

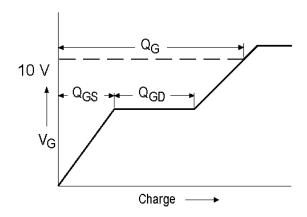


Fig 13a. Basic Gate Charge Waveform

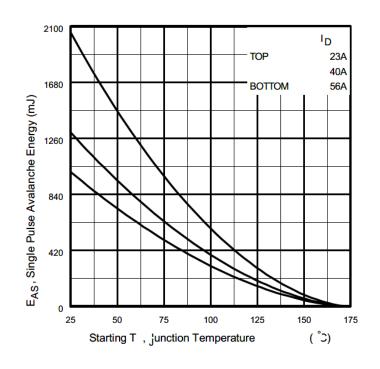


Fig 12c. Maximum Avalanche Energy vs. Drain Current

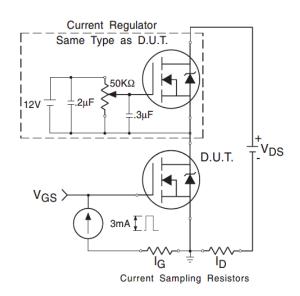
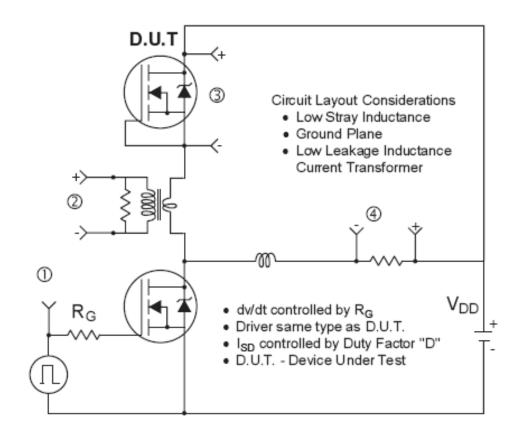
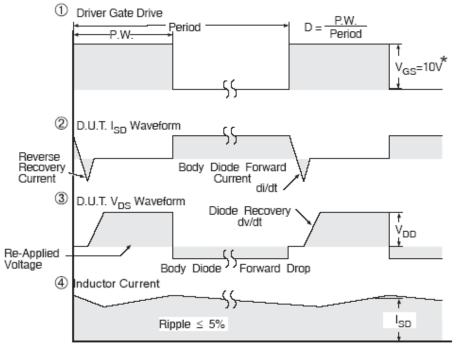


Fig 13b. Gate Charge Test Circuit



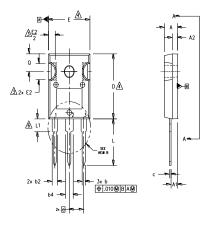




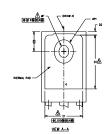
\*  $V_{GS}$  = 5V for Logic Level Devices

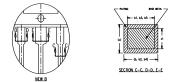
Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

# TO-247AC Package Outline (Dimensions are









		DIMEN	ISIONS		Γ
SYMBOL	INC	HES	MILLIN	IETERS	1
ĺ	MIN.	MAX.	MIN.	MAX.	٦N
A	.183	.209	4.65	5.31	Γ
A1	.087	.102	2.21	2.59	
A2	.059	.098	1.50	2.49	
b	.039	.055	0.99	1.40	
b1	.039	.053	0.99	1.35	
b2	.065	.094	1.65	2.39	
b3	.065	.092	1.65	2.34	
b4	.102	.135	2.59	3.43	
b5	.102	.133	2.59	3.38	
с	.015	.035	0.38	0.89	
c1	.015	.033	0.38	0.84	
D	.776	.815	19.71	20.70	
D1	.515	-	13.08	-	
D2	.020	.053	0.51	1.35	
E	.602	.625	15.29	15.87	
E1	.530	-	13.46	-	
E2	.178	.216	4.52	5.49	
e	.215	BSC	5.46	BSC	1
Øk	.0	10	0.	25	1
L	.559	.634	14.20	16.10	1
L1	.146	.169	3.71	4.29	
øP [	.140	.144	3.56	3.66	

#### NOTES:

- 1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M 1994.
- DIMENSIONS ARE SHOWN IN INCHES.
- 3 CONTOUR OF SLOT OPTIONAL.
- 4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS D1 & E1.
  - LEAD FINISH UNCONTROLLED IN L1.
  - OP TO HAVE A MAXIMUM DRAFT ANGLE OF 1.5 ' TO THE TOP OF THE PART WITH A MAXIMUM HOLE DIAMETER OF .154 INCH.
- 8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-247AC .

	DIMENSIONS						
SYMBOL	INC	HES	MILLIM	ETERS	1		
	MIN. MAX.		MIN.	MAX.	NOTES		
Α	.183	.209	4.65	5.31			
A1	.087	.102	2.21	2.59			
A2	.059	.098	1.50	2.49			
b	.039	.055	0.99	1.40			
b1	.039	.053	0.99	1.35			
b2	.065	.094	1.65	2.39			
b3	.065	.092	1.65	2.34			
b4	.102	.135	2.59	3.43			
b5	.102	.133	2.59	3.38			
с	.015	.035	0.38	0.89			
c1	.015	.033	0.38	0.84			
D	.776	.815	19.71	20.70	4		
D1	.515	-	13.08	-	5		
D2	.020	.053	0.51	1.35			
Ε	.602	.625	15.29	15.87	4		
E1	.530	-	13.46	-			
E2	.178	.216	4.52	5.49			
e	.215	BSC	5.46	BSC	1		
Øk	.010		0.	25	]		
L	.559	.634	14.20	16.10	]		
Ľ	.146	.169	3.71	4.29			
øP	.140	.144	3.56	3.66			
ØP1	-	.291	-	7.39			
Q	.209	.224	5.31	5.69			
S	.217	BSC	5.51	BSC			

#### LEAD ASSIGNMENTS

infineon

<u>HEXFET</u>

1.- GATE 2.- DRAIN 3.- SOURCE

4.- DRAIN

IGBTs, CoPACK

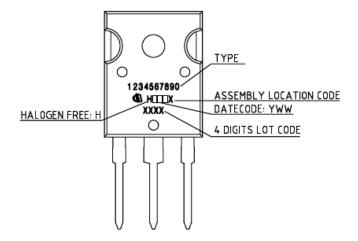
1.- GATE 2.- COLLECTOR 3.- EMITTER 4.- COLLECTOR

**DIODES** 

1.- ANODE/OPEN 2.- CATHODE

3.- ANODE

# **TO-247AC Part Marking Information**



TO-247AC package is not recommended for Surface Mount Application.

# IRFP90N20DPbF



# **Revision History**

Date	Rev.	Comments		
2024-10-03	2.1	<ul> <li>Update datasheet to Infineon format</li> <li>Updated Part marking –page 8</li> <li>Added disclaimer on last page.</li> </ul>		

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