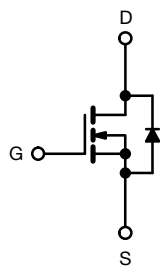


Power MOSFET

TO-220AB


N-Channel MOSFET

FEATURES

- Dynamic dV/dt rating
- 175 °C operating temperature
- Fast switching
- Ease of paralleling
- Simple drive requirements
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


Available
RoHS*
Available

Note

* This datasheet provides information about parts that are RoHS-compliant and / or parts that are non RoHS-compliant. For example, parts with lead (Pb) terminations are not RoHS-compliant. Please see the information / tables in this datasheet for details

DESCRIPTION

Third generation power MOSFETs from Vishay provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The TO-220AB package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220AB contribute to its wide acceptance throughout the industry.

PRODUCT SUMMARY

V _{DS} (V)	60	
R _{DS(on)} (Ω)	V _{GS} = 10 V	0.20
Q _g (Max.) (nC)	11	
Q _{gs} (nC)	3.1	
Q _{gd} (nC)	5.8	
Configuration	Single	

ORDERING INFORMATION

Package	TO-220AB
Lead (Pb)-free	IRFZ14PbF
Lead (Pb)-free and halogen-free	IRFZ14PbF-BE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-source voltage ^f	V _{DS}	60	V
Gate-source voltage ^f	V _{GS}	± 20	
Continuous drain current	I _D	T _C = 25 °C	A
		T _C = 100 °C	
Pulsed drain current ^a	I _{DM}	40	
Linear derating factor		0.29	W/°C
Single pulse avalanche energy ^b	E _{AS}	47	mJ
Maximum power dissipation	P _D	43	W
Peak diode recovery dV/dt ^c	dV/dt	4.5	V/ns
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +175	°C
Soldering recommendations (peak temperature)	For 10 s	300 ^d	
Mounting torque	6-32 or M3 screw	10	
		1.1	N · m

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. V_{DD} = 25 V; starting T_J = 25 °C, L = 1.47 mH, R_g = 25 Ω, I_{AS} = 8 A (see fig. 12)

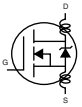
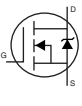
c. I_{SD} ≤ 10 A, dI/dt ≤ 90 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 175 °C

d. 1.6 mm from case

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum junction-to-ambient	R_{thJA}	-	62	°C/W
Case-to-sink, flat, greased surface	R_{thCS}	0.50	-	
Maximum junction-to-case (drain)	R_{thJC}	-	3.5	

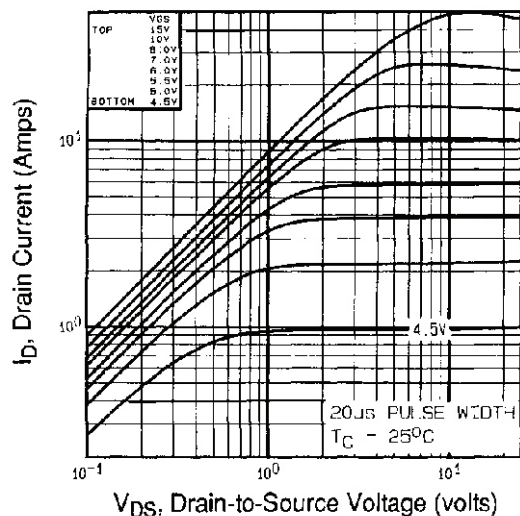
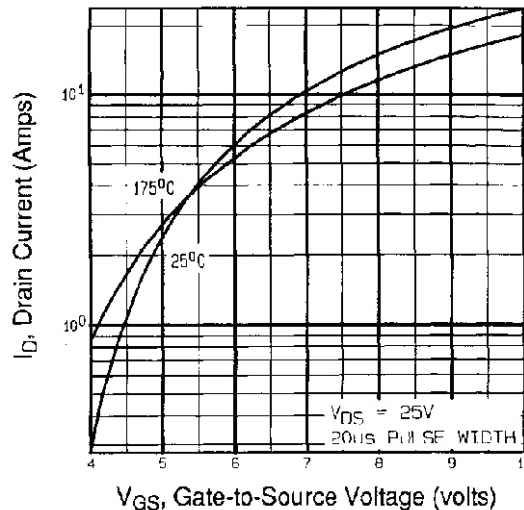
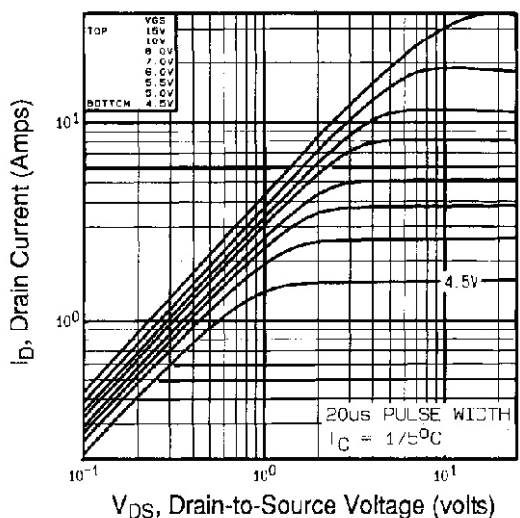
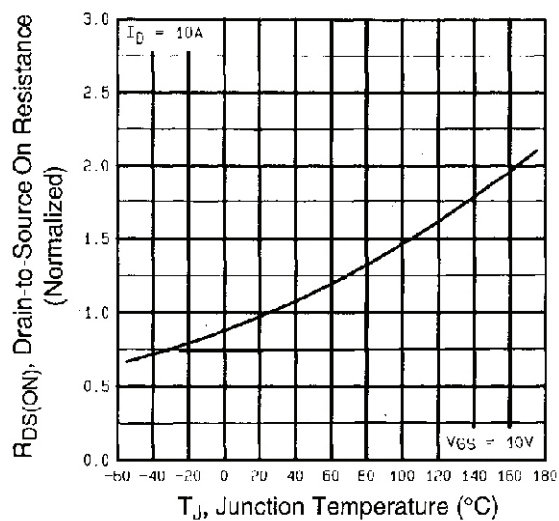
SPECIFICATIONS ($T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$		60	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}$		-	0.063	-	V/ $^\circ\text{C}$
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0	V
Gate-source leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$		-	-	25	μA
		$V_{DS} = 48\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$		-	-	250	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 6.0\text{ A}^b$	-	-	0.20	Ω
Forward transconductance	g_{fs}	$V_{DS} = 25\text{ V}$, $I_D = 6.0\text{ A}^b$		2.4	-	-	S
Dynamic							
Input capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_{DS} = 25\text{ V}$, $f = 1.0\text{ MHz}$, see fig. 5		-	300	-	pF
Output capacitance	C_{oss}			-	160	-	
Reverse transfer capacitance	C_{rss}			-	29	-	
Total gate charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}$, $V_{DS} = 48\text{ V}$, see fig. 6 and 13 ^b	-	-	11	nC
Gate-source charge	Q_{gs}			-	-	3.1	
Gate-drain charge	Q_{gd}			-	-	5.8	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 30\text{ V}$, $I_D = 10\text{ A}$, $R_g = 24\text{ }\Omega$, $R_D = 2.7\text{ }\Omega$, see fig. 10 ^b		-	10	-	ns
Rise time	t_r			-	50	-	
Turn-off delay time	$t_{d(off)}$			-	13	-	
Fall time	t_f			-	19	-	
Internal drain inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal source inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	10	A
Pulsed diode forward current ^a	I_{SM}			-	-	40	
Body diode voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}$, $I_S = 10\text{ A}$, $V_{GS} = 0\text{ V}^b$		-	-	1.6	V
Body diode reverse recovery time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}$, $I_F = 10\text{ A}$, $dI/dt = 100\text{ A}/\mu\text{s}^b$		-	70	140	ns
Body diode reverse recovery charge	Q_{rr}			-	0.20	0.40	μC
Forward turn-on time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11)

b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

Fig. 1 - Typical Output Characteristics, $T_C = 25^\circ\text{C}$

Fig. 3 - Typical Transfer Characteristics

Fig. 2 - Typical Output Characteristics, $T_C = 175^\circ\text{C}$

Fig. 4 - Normalized On-Resistance vs. Temperature

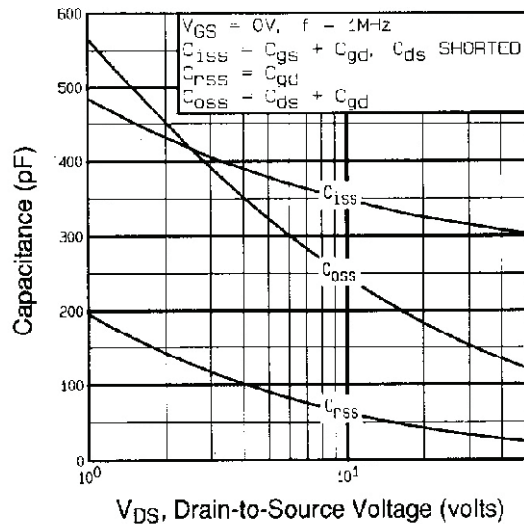


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

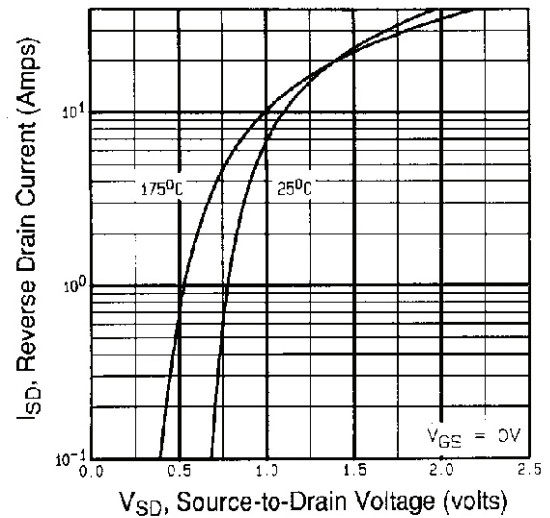


Fig. 7 - Typical Source-Drain Diode Forward Voltage

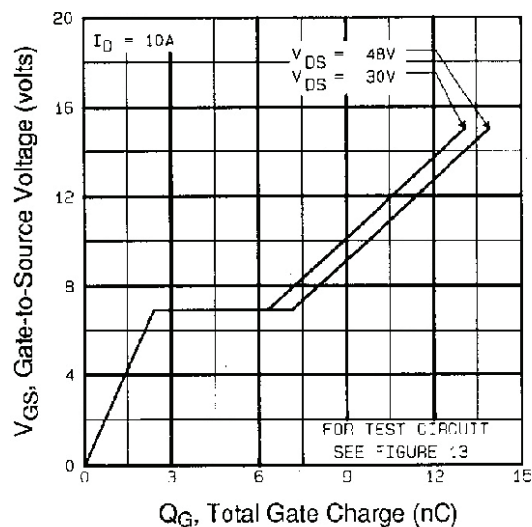


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

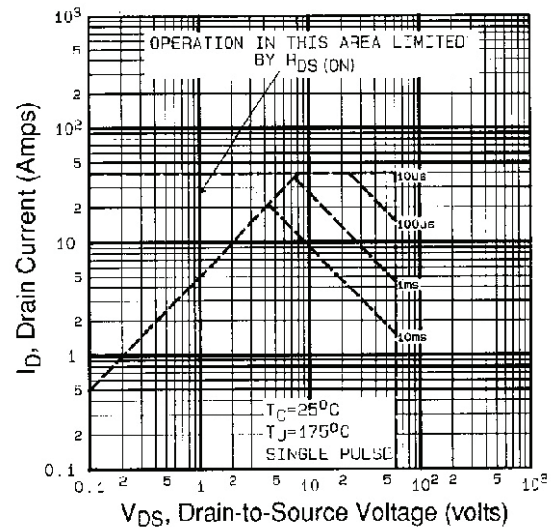
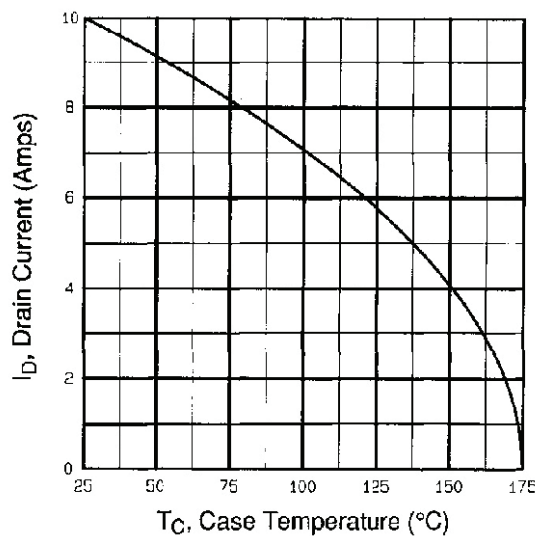
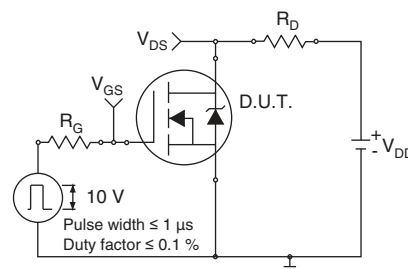
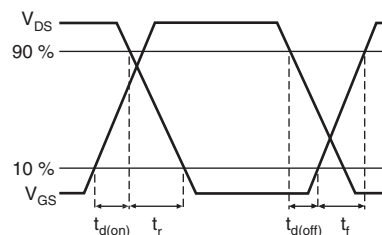
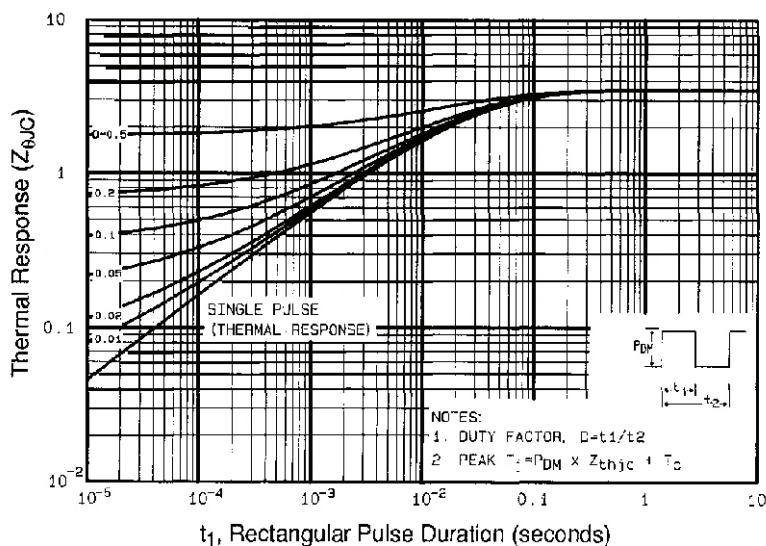
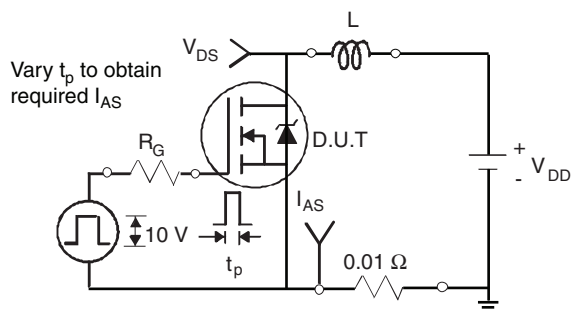
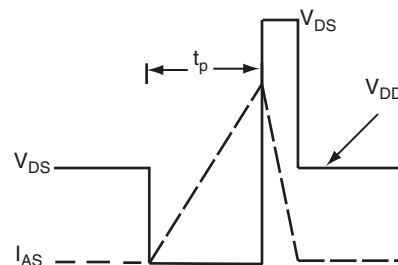
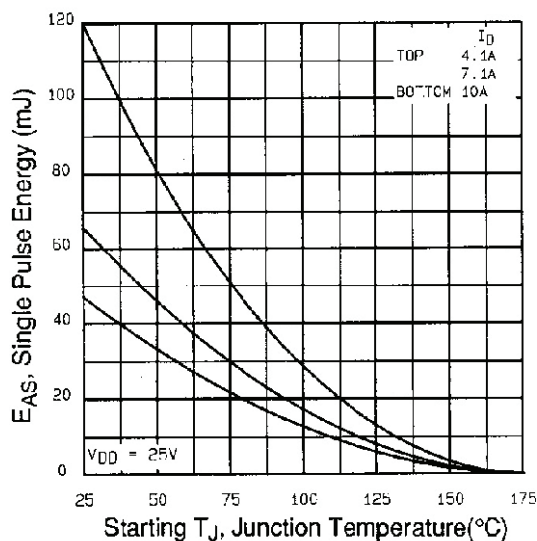
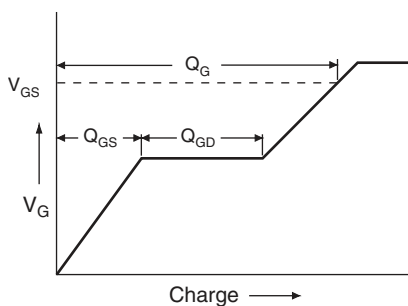
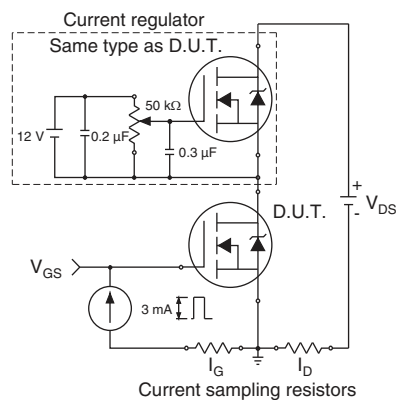
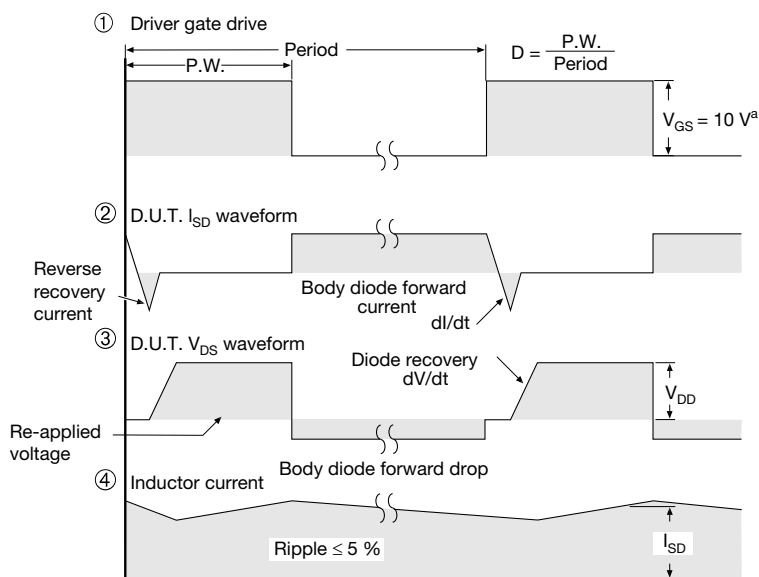
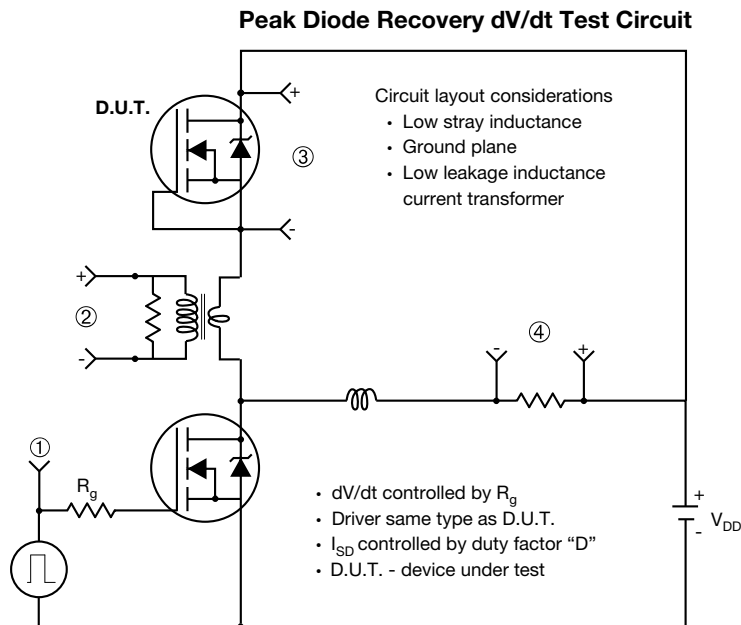


Fig. 8 - Maximum Safe Operating Area


Fig. 9 - Maximum Drain Current vs. Case Temperature

Fig. 10 - Switching Time Test Circuit

Fig. 11 - Switching Time Waveforms

Fig. 12 - Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig. 13 - Unclamped Inductive Test Circuit

Fig. 14 - Unclamped Inductive Waveforms

Fig. 15 - Maximum Avalanche Energy vs. Drain Current

Fig. 16 - Basic Gate Charge Waveform

Fig. 17 - Gate Charge Test Circuit


Note

a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

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