

ECOSPARK[®] Ignition IGBT

300 mJ, 400 V, N-Channel Ignition IGBT

ISL9V3040D3STV

Features

- SCIS Energy = 300 mJ at $T_J = 25^\circ\text{C}$
- Logic Level Gate Drive
- This Device is Pb-Free and is RoHS Compliant
- AEC-Q101 Qualified and PPAP Capable

Applications

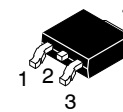
- Automotive Ignition Coil Driver Circuits
- High Current Ignition System
- Coil on Plug Applications

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ Unless Otherwise Stated)

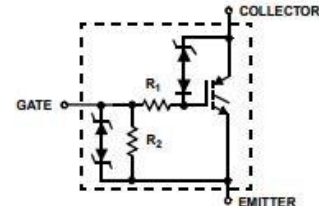
Parameter	Symbol	Value	Units
Collector to Emitter Breakdown Voltage ($I_C = 1\text{ mA}$)	BV_{CER}	400	V
Emitter to Collector Voltage – Reverse Battery Condition ($I_C = 10\text{ mA}$)	BV_{ECS}	24	V
ISCIS = 14.2 A, L = 3.0 mHz, $R_{\text{GE}} = 1\text{ K}\Omega$ (Note 1), $T_C = 25^\circ\text{C}$	E_{SCIS25}	300	mJ
ISCIS = 10.6 A, L = 3.0 mHz, $R_{\text{GE}} = 1\text{ K}\Omega$ (Note 2), $T_C = 150^\circ\text{C}$	E_{SCIS150}	170	mJ
Collector Current Continuous, at $V_{\text{GE}} = 4.0\text{ V}$, $T_C = 25^\circ\text{C}$	IC_{25}	21	A
Collector Current Continuous, at $V_{\text{GE}} = 4.0\text{ V}$, $T_C = 110^\circ\text{C}$	IC_{110}	17	A
Gate to Emitter Voltage Continuous	V_{GEM}	± 10	V
Power Dissipation Total, $T_C = 25^\circ\text{C}$	PD	150	W
Power Dissipation Derating, $T_C > 25^\circ\text{C}$	PD	1	W/ $^\circ\text{C}$
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	300	$^\circ\text{C}$
Reflow soldering according to JESD020C	T_{PKG}	260	$^\circ\text{C}$
HBM-Electrostatic Discharge Voltage at 100 pF, 1500 Ω	ESD	4	kV
CDM-Electrostatic Discharge Voltage at 1 Ω	ESD	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

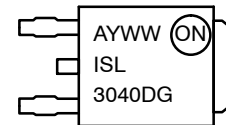
1. Self Clamped inductive Switching Energy (E_{SCIS25}) of 300 mJ is based on the test conditions that is starting $T_J = 25^\circ\text{C}$, L = 3 mHz, ISCIS = 14.2 A, $V_{\text{CC}} = 100\text{ V}$ during inductor charging and $V_{\text{CC}} = 0\text{ V}$ during time in clamp.
2. Self Clamped inductive Switching Energy (E_{SCIS150}) of 170 mJ is based on the test conditions that is starting $T_J = 150^\circ\text{C}$, L = 3 mHz, ISCIS = 10.6 A, $V_{\text{CC}} = 100\text{ V}$ during inductor charging and $V_{\text{CC}} = 0\text{ V}$ during time in clamp.



DPAK (SINGLE GAUGE)
CASE 369C



MARKING DIAGRAM



ISL3040DG = Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping [†]
ISL9V3040D3STV	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ISL9V3040D3STV

THERMAL RESISTANCE RATINGS

Characteristic	Symbol	Max	Units
Junction-to-Case – Steady State (Drain) (Notes 1, 3 and 4)	$R_{\theta JC}$	1	°C/W

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Collector to Emitter Breakdown Voltage	BV_{CER}	$I_{CE} = 2\text{ mA}$, $V_{GE} = 0\text{ V}$, $R_{GE} = 1\text{ K}\Omega$, $T_J = -40\text{ to }150^\circ\text{C}$		370	400	430	V
Collector to Emitter Breakdown Voltage	BV_{CES}	$I_{CE} = 10\text{ mA}$, $V_{GE} = 0\text{ V}$, $R_{GE} = 0$, $T_J = -40\text{ to }150^\circ\text{C}$		390	420	450	V
Emitter to Collector Breakdown Voltage	BV_{ECS}	$I_{CE} = -75\text{ mA}$, $V_{GE} = 0\text{ V}$, $T_J = 25^\circ\text{C}$		30	–	–	V
Gate to Emitter Breakdown Voltage	BV_{GES}	$I_{GES} = \pm 2\text{ mA}$		± 12	± 14	–	V
Collector to Emitter Leakage Current	I_{CER}	$V_{CE} = 175\text{ V}$, $R_{GE} = 1\text{ K}\Omega$	$T_J = 25^\circ\text{C}$	–	–	25	μA
			$T_J = 150^\circ\text{C}$	–	–	1	mA
Emitter to Collector Leakage Current	I_{ECS}	$V_{EC} = 24\text{ V}$	$T_J = 25^\circ\text{C}$	–	–	1	mA
			$T_J = 150^\circ\text{C}$	–	–	40	
Series Gate Resistance	R_1			–	70	–	Ω
Gate to Emitter Resistance	R_2			10 K	–	26 K	Ω

ON CHARACTERISTICS

Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{CE} = 6\text{ A}$, $V_{GE} = 4\text{ V}$, $T_J = 25^\circ\text{C}$	–	1.25	1.65	V
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{CE} = 10\text{ A}$, $V_{GE} = 4.5\text{ V}$, $T_J = 150^\circ\text{C}$	–	1.58	1.80	V
Collector to Emitter Saturation Voltage	$V_{CE(SAT)}$	$I_{CE} = 15\text{ A}$, $V_{GE} = 4.5\text{ V}$, $T_J = 150^\circ\text{C}$	–	1.90	2.20	V

DYNAMIC CHARACTERISTICS

Gate Charge	$Q_{G(ON)}$	$I_{CE} = 10\text{ A}$, $V_{CE} = 12\text{ V}$, $V_{GE} = 5\text{ V}$	–	17	–	nC	
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_{CE} = 1\text{ mA}$, $V_{CE} = V_{GE}$	$T_J = 25^{\circ}\text{C}$	1.3	–	2.2	V
			$T_J = 150^{\circ}\text{C}$	0.75	–	1.8	
Gate to Emitter Plateau Voltage	V_{GEP}	$V_{CE} = 12\text{ V}$, $I_{CE} = 10\text{ A}$	–	3.0	–	V	

SWITCHING CHARACTERISTICS

Current Turn-On Delay Time–Resistive	$t_{d(ON)R}$	$V_{CE} = 14\text{ V}$, $R_L = 1\text{ }\Omega$, $V_{GE} = 5\text{ V}$, $R_G = 470\text{ }\Omega$, $T_J = 25^\circ\text{C}$	–	0.7	4	μs
Current Rise Time–Resistive	t_{rR}		–	2.1	7	
Current Turn-Off Delay Time–Inductive	$t_{d(OFF)L}$	$V_{CE} = 300\text{ V}$, $L = 1\text{ mH}$, $V_{GE} = 5\text{ V}$, $R_G = 470\text{ }\Omega$, $I_{CE} = 6.5\text{ A}$, $T_J = 25^\circ\text{C}$	–	4.8	15	
Current Fall Time–Inductive	t_{fL}		–	2.8	15	

TYPICAL CHARACTERISTICS

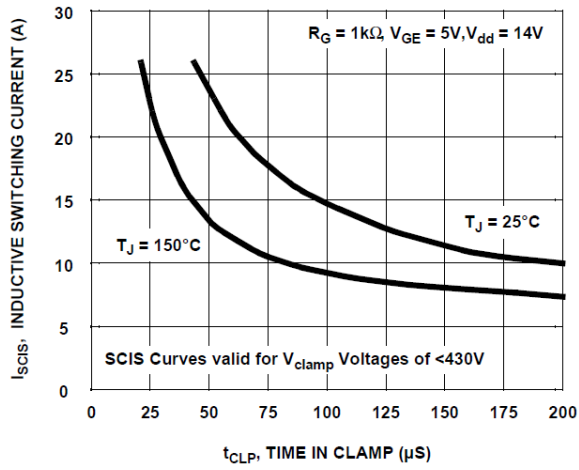


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

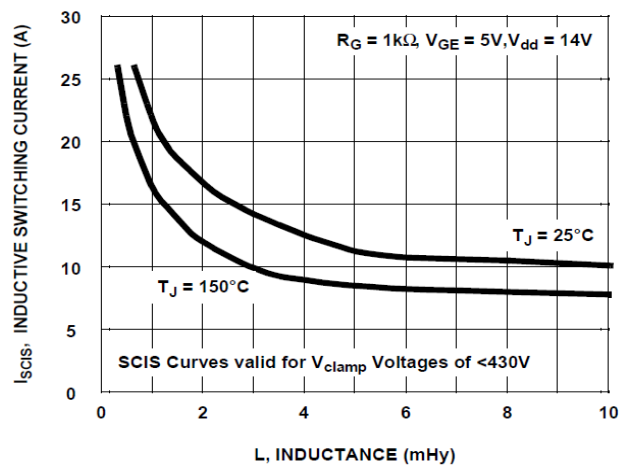


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

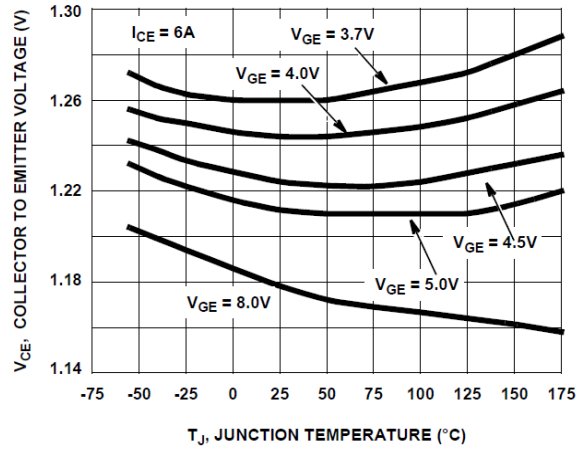


Figure 3. Collector to Emitter On-State Voltage vs. Junction Temperature

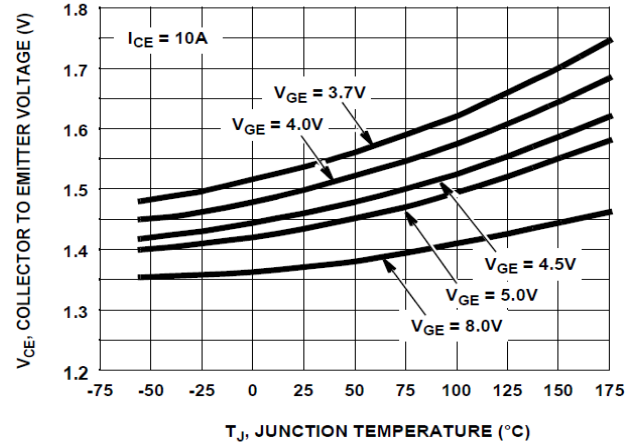


Figure 4. Collector to Emitter On-State Voltage vs. Junction Temperature

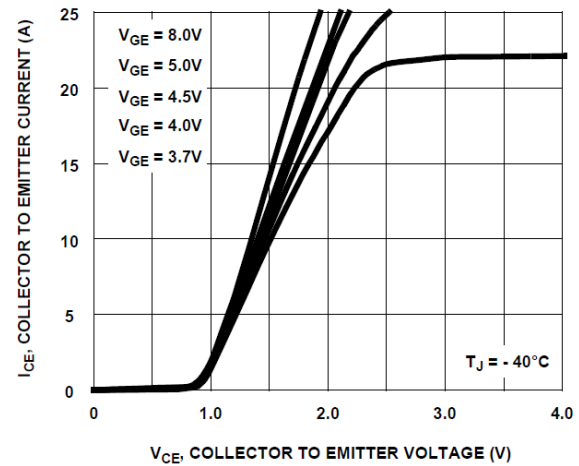


Figure 5. Collector to Emitter On-State Voltage vs. Collector Current

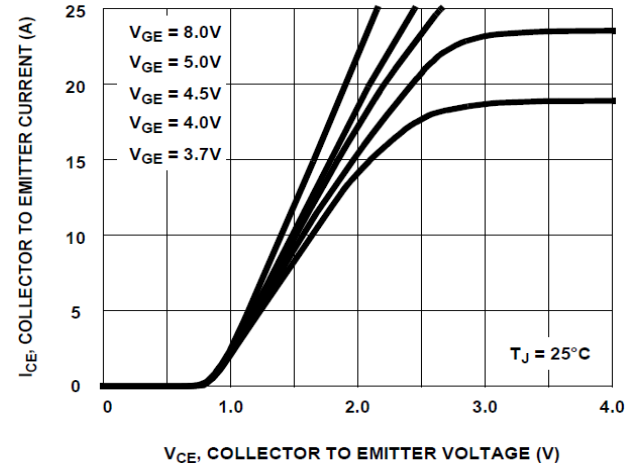


Figure 6. Collector to Emitter On- State Voltage vs. Collector Current

TYPICAL CHARACTERISTICS (continued)

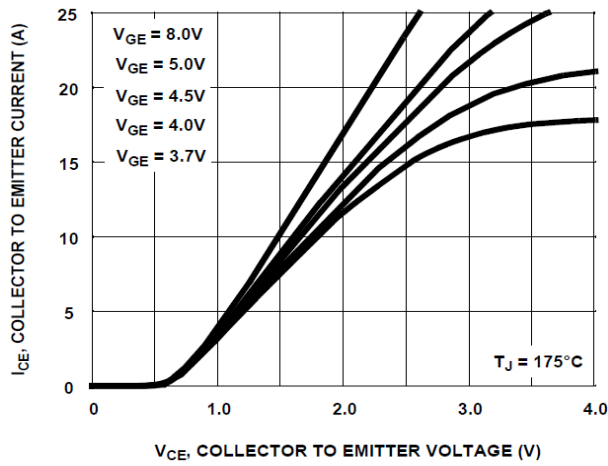


Figure 7. Collector to Emitter On-State Voltage vs. Collector Current

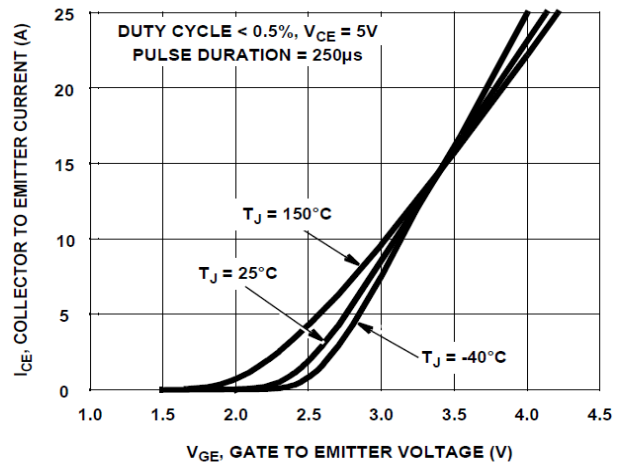


Figure 8. Transfer Characteristics

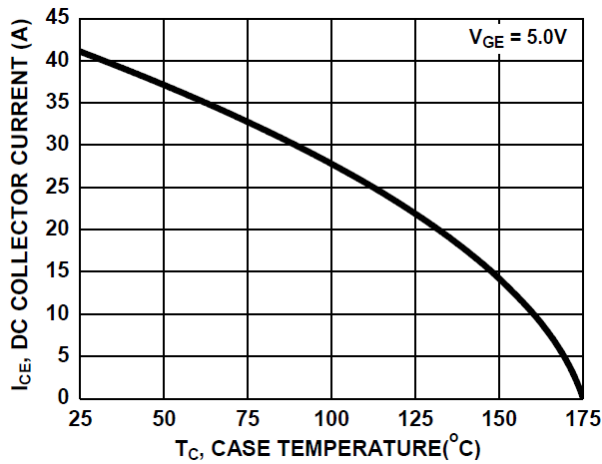


Figure 9. DC Collector Current vs. Case Temperature

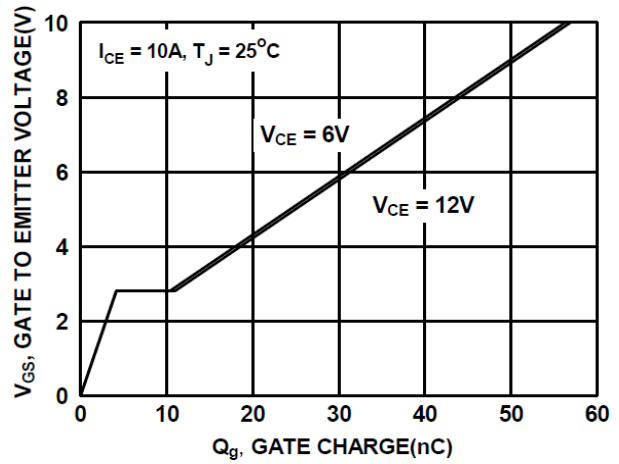


Figure 10. Gate Charge

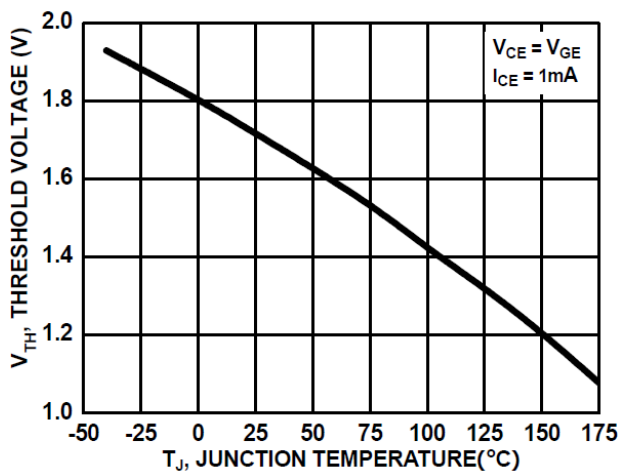


Figure 11. Threshold Voltage vs. Junction Temperature

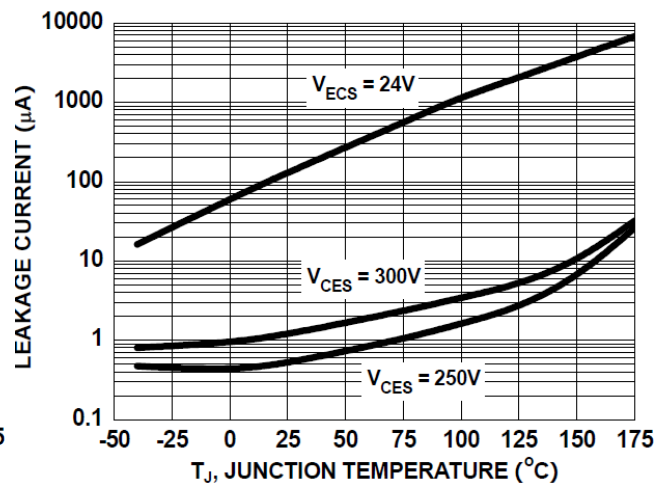
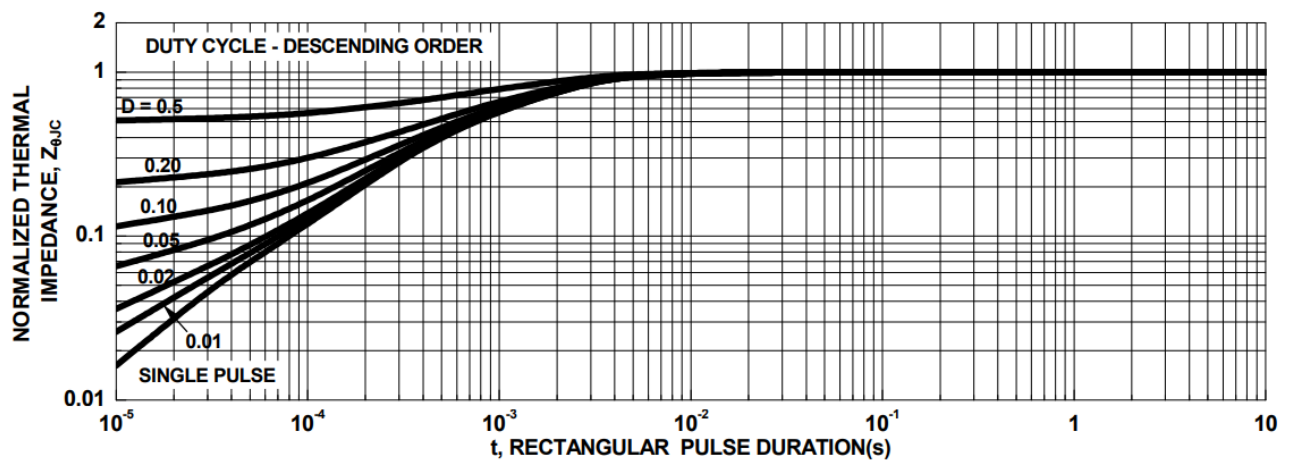
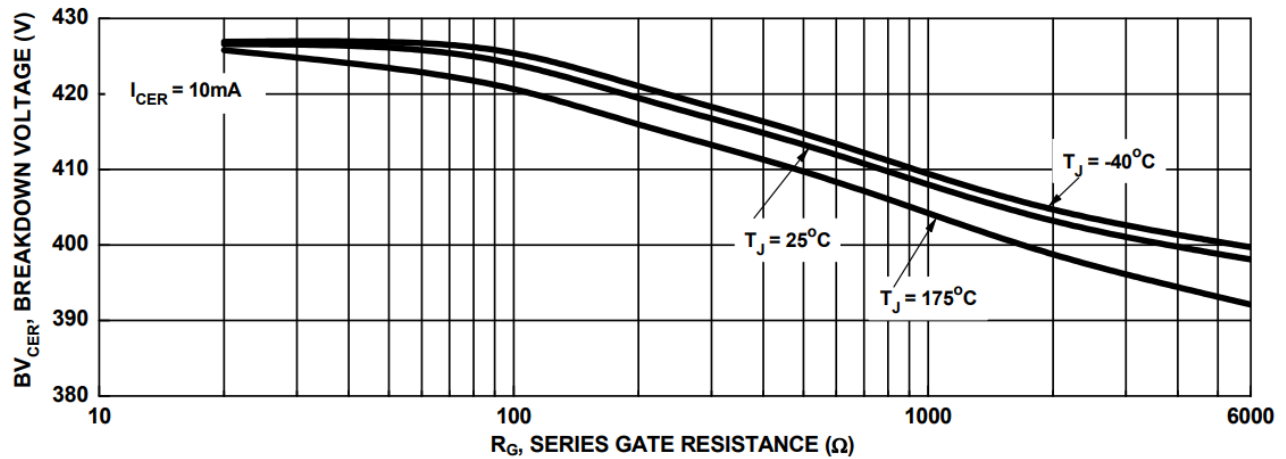
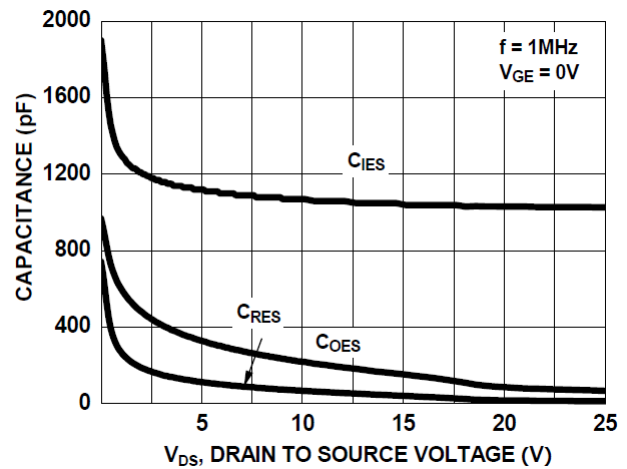
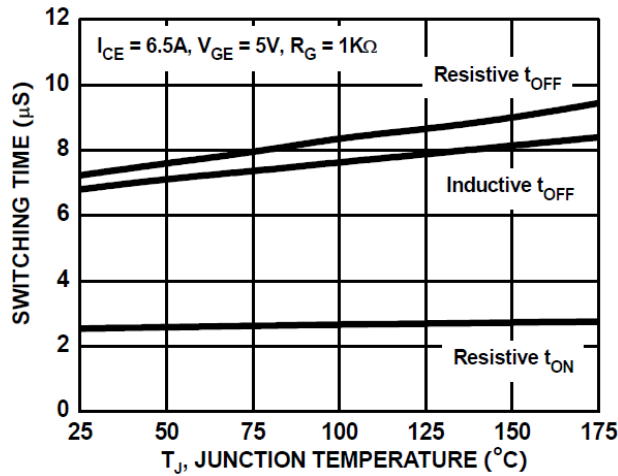


Figure 12. Leakage Current vs. Junction Temperature

ISL9V3040D3STV

TYPICAL CHARACTERISTICS (continued)



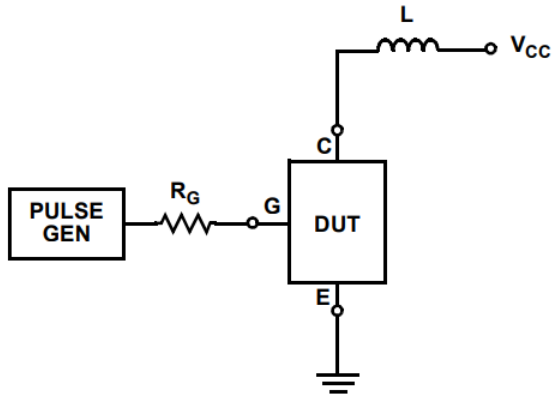


Figure 17. Inductive Switching Test Circuit

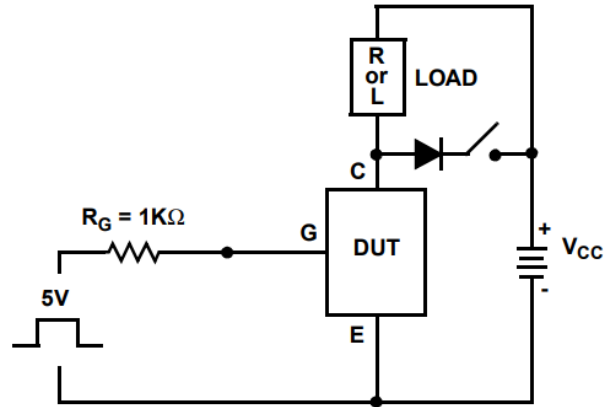


Figure 18. t_{ON} and t_{OFF} Switching Test Circuit

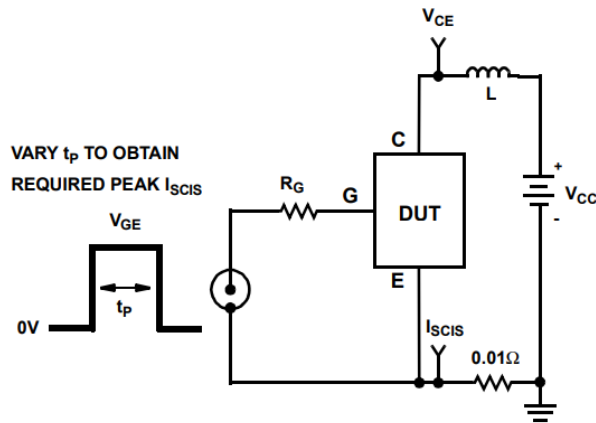


Figure 19. Energy Test Circuit

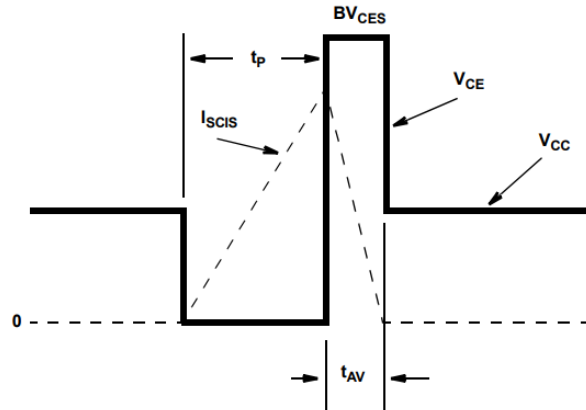
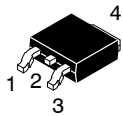


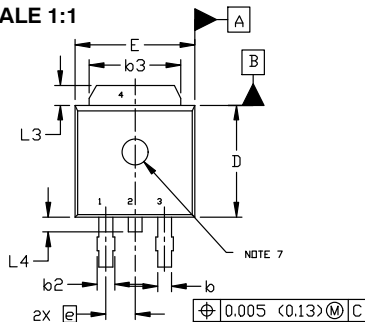
Figure 20. Energy Waveforms



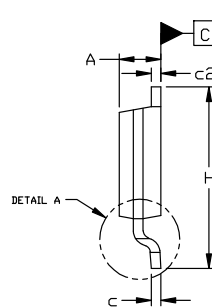
DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

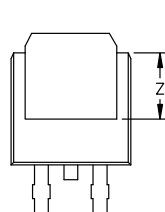
SCALE 1:1



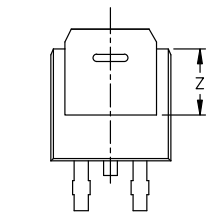
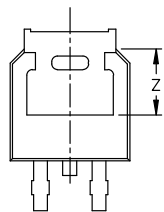
TOP VIEW



SIDE VIEW

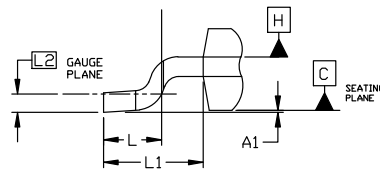
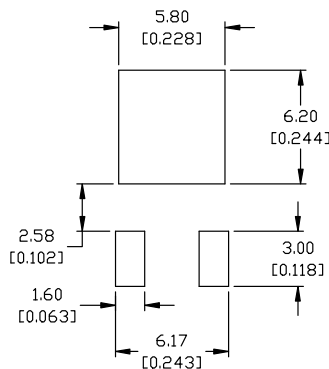


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE
CONSTRUCTIONS



DETAIL A
ROTATED 90° CW

NOTES:

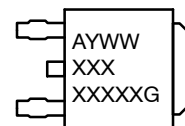
1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	----	0.040	---	1.01
Z	0.155	----	3.93	---

GENERIC
MARKING DIAGRAM*



IC



Discrete

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 3: PIN 1. ANODE 2. CATHODE 3. ANODE 4. CATHODE	STYLE 4: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE	STYLE 5: PIN 1. GATE 2. ANODE 3. CATHODE 4. ANODE
STYLE 6: PIN 1. MT1 2. MT2 3. GATE 4. MT2	STYLE 7: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 8: PIN 1. N/C 2. CATHODE 3. ANODE 4. CATHODE	STYLE 9: PIN 1. ANODE 2. CATHODE 3. RESISTOR ADJUST 4. CATHODE	STYLE 10: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. ANODE

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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