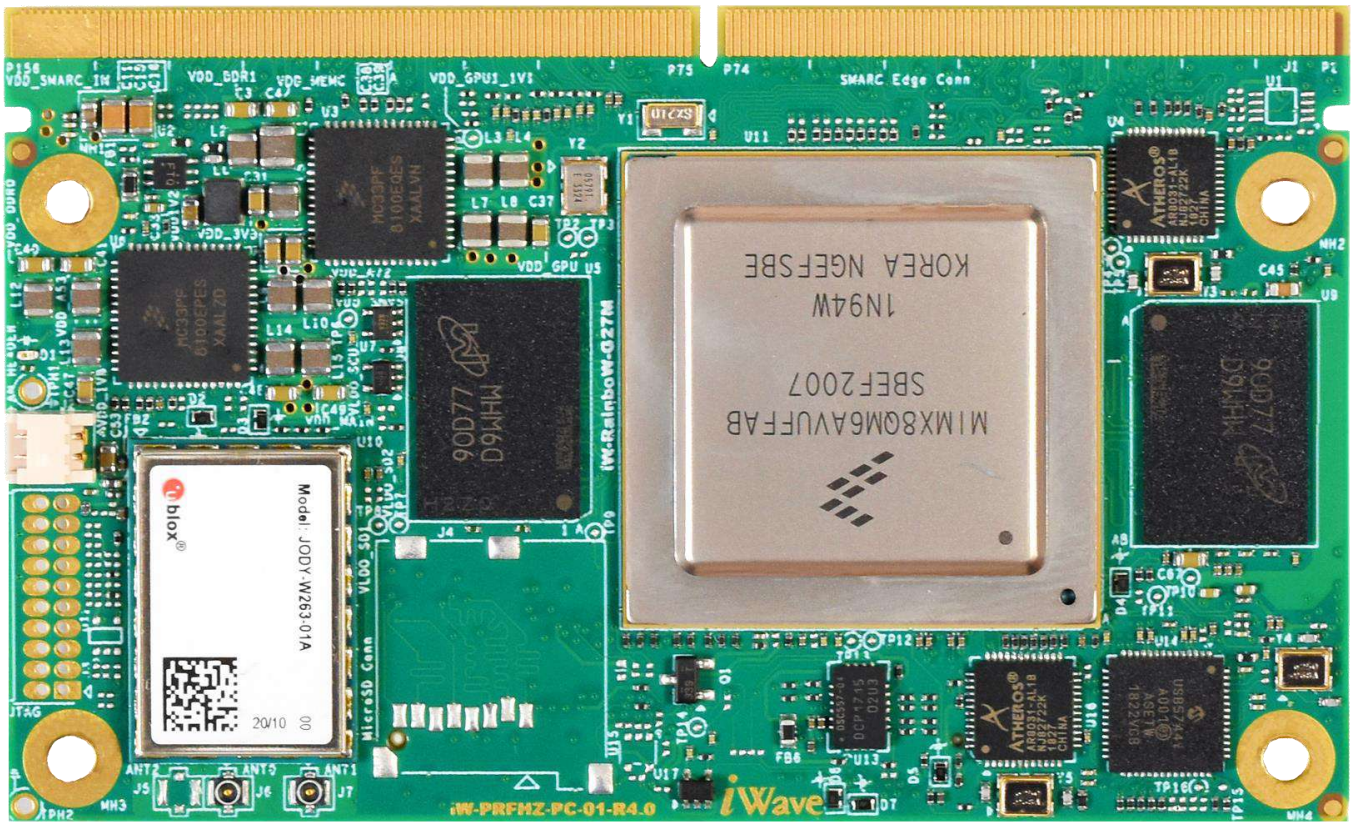
iW-RainboW-G27M
i.MX8 QuadMax/QuadPlus
SMARC System On Module
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the SMARC V2.1.1 SOM based on the NXP's i.MX8 QM/QP (QuadMax/QuadPlus) Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX8 SMARC SOM from a Hardware Systems perspective.

1.2 SMARC SOM Overview

The SMARC V2.1.1 ("Smart Mobility ARChitecture version 2.1.1") is a versatile small form factor computer Module definition targeting application that require low power, low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, GBE and dual channel LVDS/MIPI display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

NXP's i.MX8 SoC based SMARC System on Module is rich with i.MX8 features along with on SOM LPDDR4, eMMC, Dual Ethernet PHY, USB3.0 Hub, Wi-Fi & BT module and comes in compact 82mm x 50mm form factor. The Module PCB has 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CAN	Controller Area Network
CODEC	Coder-Decoder
CPU	Central Processing Unit
CSI	Camera Serial Interface
CTS	Clear to Send
DP	Display Port
DRAM	Dynamic Random Access Memory
DSI	Display Serial Interface
eDP	embedded Display Port
eMMC	Enhanced Multi Media Card

Acronyms	Abbreviations
EMS	Electronics manufacturing services
ESAI	Enhanced Serial Audio Interface
FIFO	First In First Out
FLEXCAN	Flexible Control Area Network
FlexSPI	Flexible Serial Peripheral Interface
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
MLB	Media Local Bus
OTG	On-The-Go
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMI	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SDIO	Secure Digital Input Output
SMARC	Smart Mobility ARChitecture
SoC	System on Chip
SOM	System On Module
SPDIF	The Sony/Philips Digital Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VPU	Video Processing Unit
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
HCSL	High speed Current Steering Logic
LVDS	Low Voltage Differential Signal
HDMI	High-Definition Multimedia Interface Differential Signal
DP	Display Port Differential Signal
GBE	Gigabit Ethernet Signal
PCIe	PCIe differential pair signals
SATA	Serial Advanced Technology Attachment differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SMARC SOM.

1.5 References

- iMX8QMAEC_ Rev. 0.pdf
- iMX8QM_RM_Rev_F.pdf
- SMARC Specification V2.1.1

1.6 Important Note

In this document, wherever i.MX8 CPU signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET1_RGMII_TXC

  In this signal, ***ENET1_RGMII_TXC*** pad is used for same functionality.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_05)

  In this signal, ***BCONFIG_0*** is the GPIO functionality and ***GPIO1_05*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX8 SMARC SOM features and Hardware architecture with high level block diagram.

2.1 i.MX8 QM/QP SMARC SOM Block Diagram

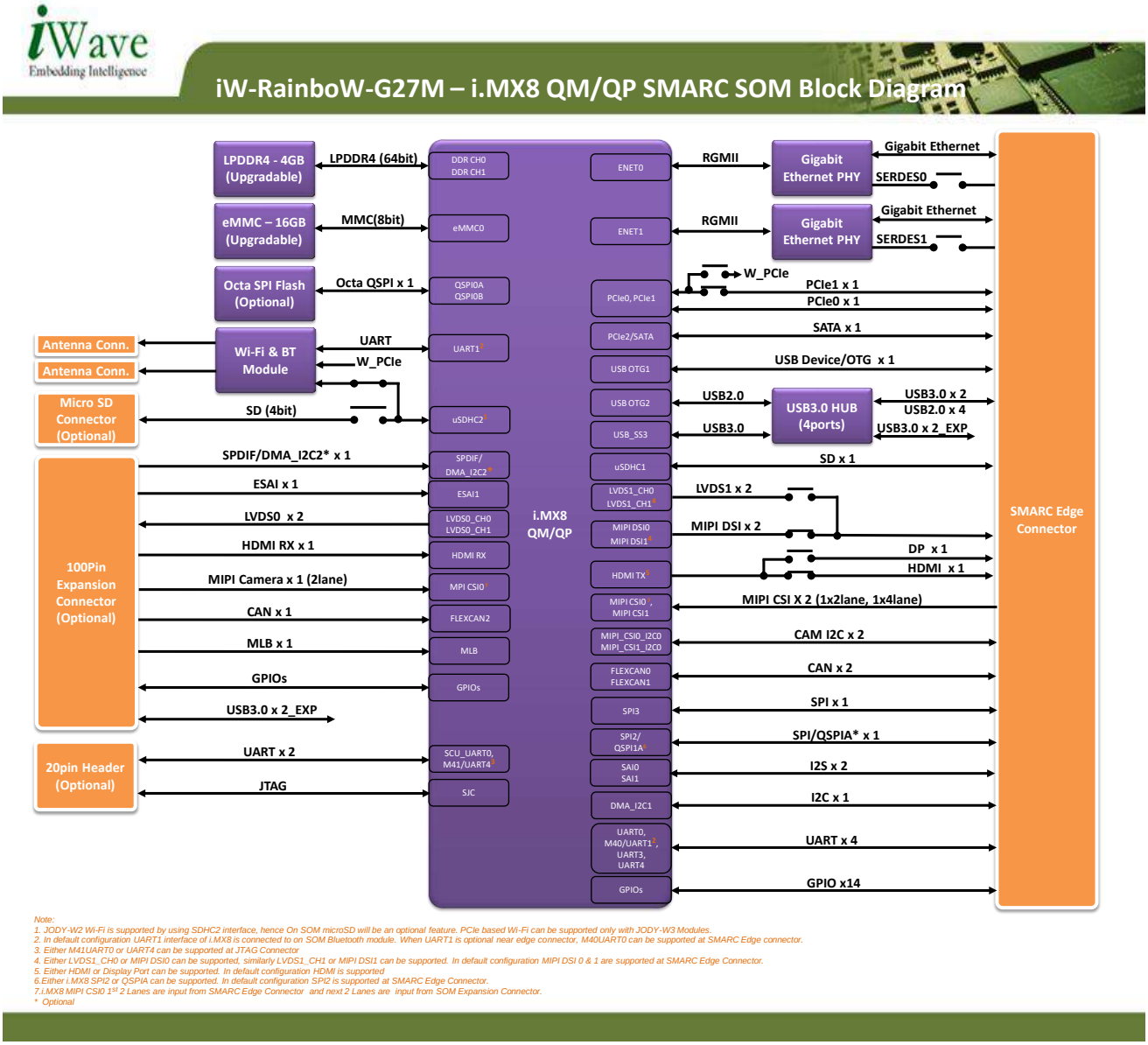

Figure 1: i.MX8 QM/QP SMARC SOM Block Diagram

2.2 i.MX8 QM/QP SMARC SOM Features

i.MX8 QM/QP SMARC SOM supports the following features.

CPU

- i.MX8 QM/QP Processor[1]:
  - i.MX8 QuadMax : 2 x Cortex-A72, 4 x Cortex-A53 & 2 x Cortex-M4F
  - i.MX8 QuadPlus : 1 x Cortex-A72, 4 x Cortex-A53 & 2 x Cortex-M4F

Power

- PF8100 PMIC x 2

Memory

- LPDDR4 - 4GB (Expandable up to 8GB)[2,3]
- eMMC Flash - 16GB (Expandable)[3,4]
- Micro SD Connector (Optional)[5]
- FlexSPI Flash (Optional)

Other On-SOM Features

- WiFi 802.11a/b/g/n/ac + BT 5.0 Module[5,6]
- Gigabit Ethernet PHY Transceiver x 2
- USB 3.0 High Speed 4-Port Hub
- FAN Header
- Debug UART & JTAG Header (Optional)

SMARC PCB Edge Interfaces

- Gigabit Ethernet x 2 Ports (through On-SOM Gigabit Ethernet PHY transceiver)
- SERDES x 2Ports (Optional. Either Gigabit Ethernet or SERDES can be supported)
- SD (4bit) x 1 Port
- USB 2.0 OTG x 1 Port
- USB3.0 Host x 2 Ports (through On-SOM USB Hub)
- USB 2.0 Host x 4Ports (through On-SOM USB Hub)
- PCIe x 2 Ports
- SATA x 1 Port
- MIPI CSI x 2 Channel (1x2lane and 1x4lane)
- HDMI/DP Transmitter x 1 Port[7]
- LVDS/MIPI DSI x 2 Channel[8]
- SAI/I2S (Audio Interface) x 2 Port
- SPI x 2 Port

- Data UART (with CTS & RTS) x 1 Port[9]
- Data UART (without CTS & RTS) x 2 Port (One port can be used as Debug Port)
- SMARC GPIO x 14[10]
- CAN x 2 Port
- I2C x 4 Ports

Expansion Connector Interfaces (Optional)

- LVDS x 2 Channel
- CAN x 1 Port
- USB3.0 Host x 2 Ports (through On-SOM USB Hub)
- ESAI x 1 Port
- SPDIF x 1 Port
- MLB x 1 Port
- HDMI Receiver x 1 Port
- GPIOs

General Specification

- Power Supply : 5V, 6A
- Form Factor : 82mm X 50mm (SMARC V2.1.1 Specification)

1. *There are two configurations of i.MX8 Processor, hence in this document i.MX8 is used to represent either i.MX8QM or i.MX8QP based on SOM Part Number.*
2. *The i.MX8 can support up to 16GB RAM but considering the available LPDDR4 configuration, it can support 8GB RAM by using two 4GB LPDDR4 chips. If 8GB (64Gb) LPDDR4 chips are available then 16GB RAM can be supported on Board.*
3. *Memory Size will differ based on iWave's SOM Product Part Number.*
4. *16GB and 32GB eMMC are already validated on i.MX8 QM platform.*
5. *JODY-W2 Wi-Fi is supported by using SDIO interface, hence On SOM microSD will be an optional feature.*
6. *802.11ax (Wi-Fi 6) can be supported by changing from JODY-W2 to JODY-W3*
7. *The i.MX8 support HDMI or Display Port through same pins, hence any one can be supported at a time based on SOM part Number.*
8. *The i.MX8 support MIPI_DSI and LVDS interface, but in SMARC Specification LVDS and MIPI_DSI interface pins are multiplexed hence any one can be supported at a time based on SOM part Number.*
9. *UART1 interface of i.MX8 is connected to on SOM Bluetooth module in the default configuration. One more UART can be supported with CTS and RTS if Bluetooth is not supported*
10. *In default configuration 12 GPIOs are supported, SMARC GPIO_12 and SMARC GPIO_13 are Optionally supported.*

2.3 i.MX8 CPU

iW-RainboW-G27M SMARC SOM can support i.MX8 CPUs from NXP. The i.MX 8 Family consists of two processors: i.MX 8QuadMax & iMX 8QuadPlus. The Major Difference between i.MX8 CPUs are:

- i.MX8 QuadMax : 2 x Cortex-A72 @ 1.6 GHz, 4 x Cortex-A53 @ 1.2 GHz & 2 x Cortex-M4F @ 264 MHz
- i.MX8 QuadPlus : 1 x Cortex-A72 @ 1.6 GHz, 4 x Cortex-A53 @ 1.2 GHz & 2 x Cortex-M4F@ 264 MHz

The i.MX8 QM/QP processors along with ARM core it supports dual 32-core GPU subsystems, 4K, H.265 capable VPU, and dual failover-ready display controllers, 2× 4K displays, supporting multiple display output options, including MIPI-DSI, HDMI 2.0, eDP/DP, and LVDS. Memory interfaces supporting LPDDR4, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, SD 3.0 and a wide range of peripheral I/Os such as PCIe 3.0 provide wide flexibility.

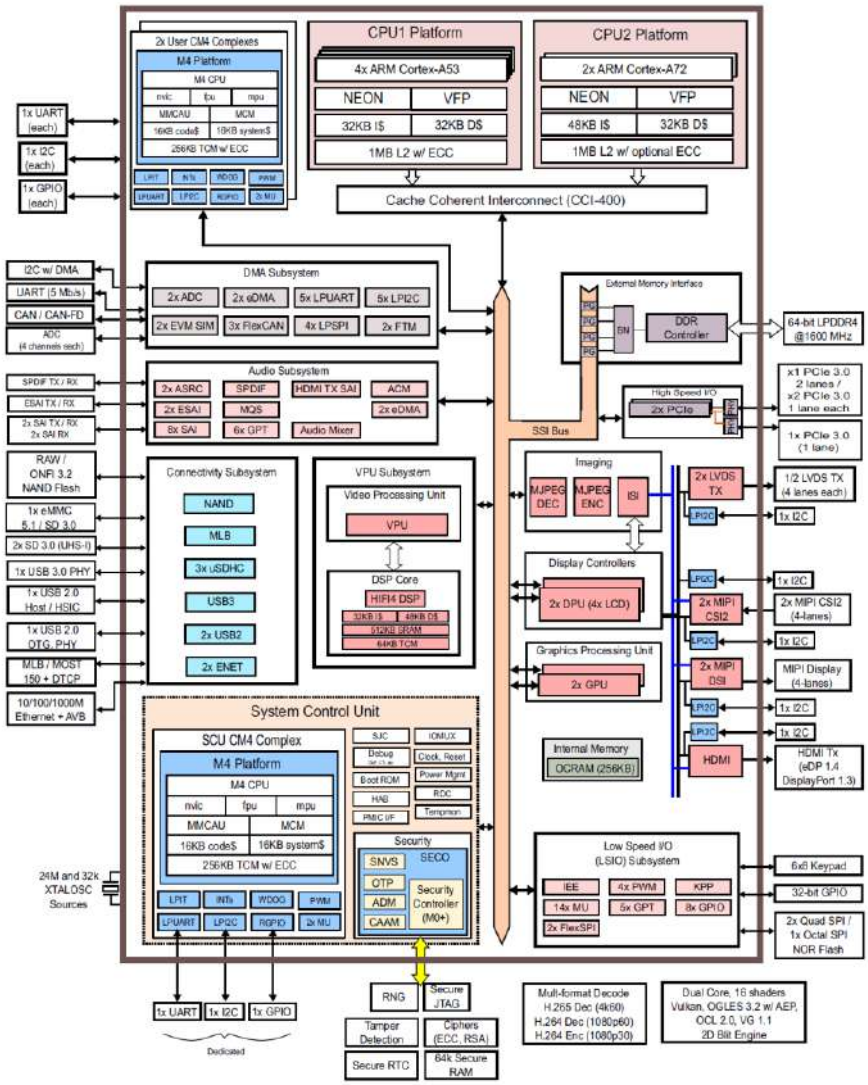

Figure 2: i.MX8 Block Diagram

Note: The i.MX8 QM/QP processor offers numerous advanced features, please refer the latest i.MX8 Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PF8100 PMIC

i.MX8 QM/QP SMARC SOM uses two PF8100/PF8200 PMIC for SOM Power management. Both the PF8100 PMIC are programmed with custom Sequence code EP and EQ from NXP.

The PF8100 is a power management integrated circuit (PMIC) features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals. Built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed 3.4 MHz I2C after start up offering flexibility for different system states. The PF8100 PMIC U6 (EP) & U3 (EQ) comes in 56pin 8x8 QFN Packages and are placed on the Top side of the SOM.

2.5 Memory

2.5.1 LPDDR4 RAM

The i.MX8 QM/QP SMARC SOM supports 4GB RAM using two 32bit 2GB LPDDR4 IC connected to DDR_CH0 and DDR_CH1 channels of CPU to support LPDDR4 up to 1.6 GHz. Both the LPDDR4 parts U5 and U9 are placed on Top side of the SOM. LPDDR4 memory size can be customised based on the requirement by contacting iWave support team.

2.5.2 eMMC Flash

The i.MX8 QM/QP SMARC SOM supports 16GB eMMC as default boot and storage device. This is connected to eMMC0 version 5.1 controller of the i.MX8 CPU and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash (U39) memory is physically located on bottom side of the SMARC SOM. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 Micro SD Connector (Optional)

The i.MX8 QM/QP SMARC SOM optionally supports Micro SD connector which can be used to connect Micro SD card as optional boot device as well as Mass storage device. Micro SD card connector (J4) is connected to the USDHC2 controller of the i.MX8 CPU. The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX8 SMARC SOM supports configurable I/O voltage levels for USDHC2 lines through LDO2OUT of PMIC1/PMIC2. The I/O voltage level of USDHC2 lines can be set 1.8V or 3.3V based on PMIC configuration. And the micro SD Connector is physically located on Top side of the i.MX8 SMARC SOM.

Note: In default configuration USDHC2 is used for on board Wi-Fi module. Contact iWave Support team if microSD feature is required or refer Application Note: "AN2703-i.MX8 QM SMARC SOM-Enabling On SOM Micro SD Support-Application Note-R4.0-REL1.0.pdf"

2.5.4 FlexSPI Flash (Optional)

The i.MX8 QM/QP SMARC SOM optionally supports FlexSPI using Micron's 512MB Xccela™ Flash Memory as a storage and can be used as optional boot device. FlexSPI is connected to QSPI0 controller of the i.MX8 processor and operates at 1.8V Voltage levels. The Xccela™ Flash (U37) memory is physically located on Bottom side of the SMARC SOM. The FlexSPI can be supported with customised memory size based on the requirement by contacting iWave Support Team.

Note: If FlexSPI Flash feature is required, contact iWave Support Team or refer Application Note: "AN2706-i.MX8 QM SMARC SOM-Enabling On SOM Octa SPI Support-Application Note-R4.0-REL1.0 .pdf"

2.6 Network & Communiation

2.6.1 Wi-Fi and Bluetooth Interface

The i.MX8 QM/QP SMARC SOM is integrated with u-blox's "JODY-W263" based Wi-Fi & Bluetooth module. The JODY-W2 series are compact modules based on the Marvell 88W8987 AEC-Q100 compliant chipset. They enable Wi-Fi, Bluetooth, and Bluetooth low energy communication. The JODY-W2 modules can be operated in the following modes:

• Wi-Fi 1x1 802.11a/b/g/n/ac in 2.4 GHz or 5 GHz

• Dual-mode Bluetooth 5, including audio, can be operated fully simultaneous with Wi-Fi

The JODY-W2 undergoes extended automotive qualification according to ISO 16750-4 and is manufactured in line with ISO/TS 16949. Connection to a host processor is through SDIO, or High-Speed UART interfaces. The i.MX8 SMARC SOM uses processor's UART1 interface for Bluetooth and USDHC2 interface for Wi-Fi in a default configuration.

In i.MX8 QM/QP SMARC SOM, antenna pins of JODY-W263 Bluetooth and Wi-Fi are connected to J6 and J7 connector respectively.

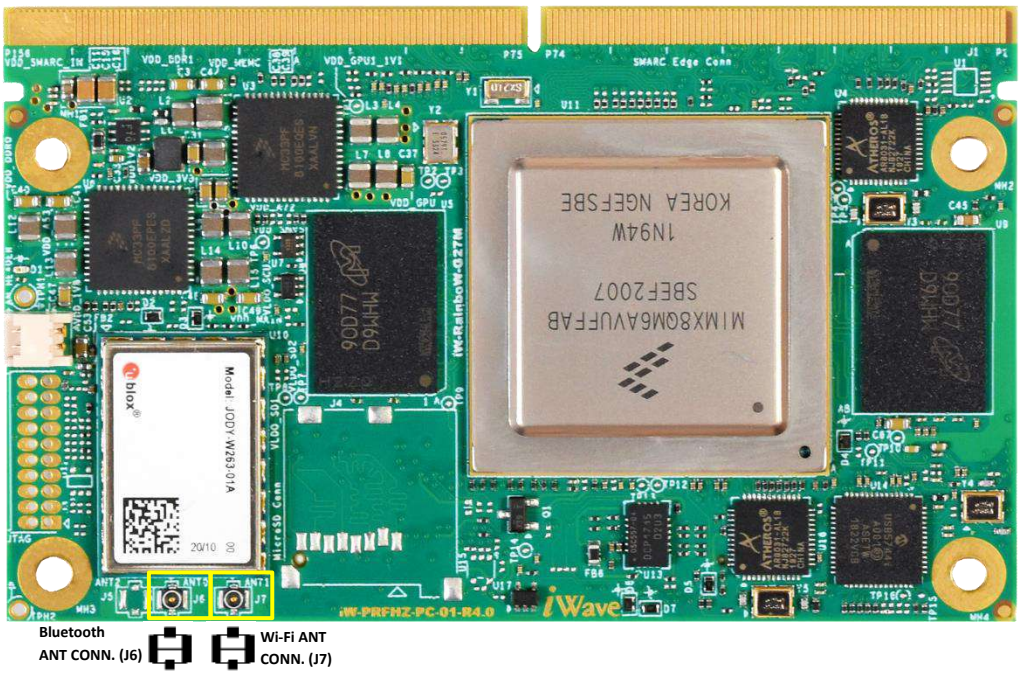

Figure 3: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : MM4829-2702RA4 from Murata Electronics.

Antenna Part Number - : 2042811100 from Molex / FXP830.24.0100B from Taoglas Limited

Note: In default configuration 802.11ax (Wi-Fi 6) is not supported, but 802.11ax can be supported by changing Wi-Fi module from JODY-W2 to JODY-W3, contact iWave Support Team for further information.

2.7 SMARC PCB Edge Connector

SMARC PCB edge connector (J1) has standard pinout as per SMARC Specification V2.1.1. The interfaces which are available at 314pin SMARC Edge connector are explained in the following sections.

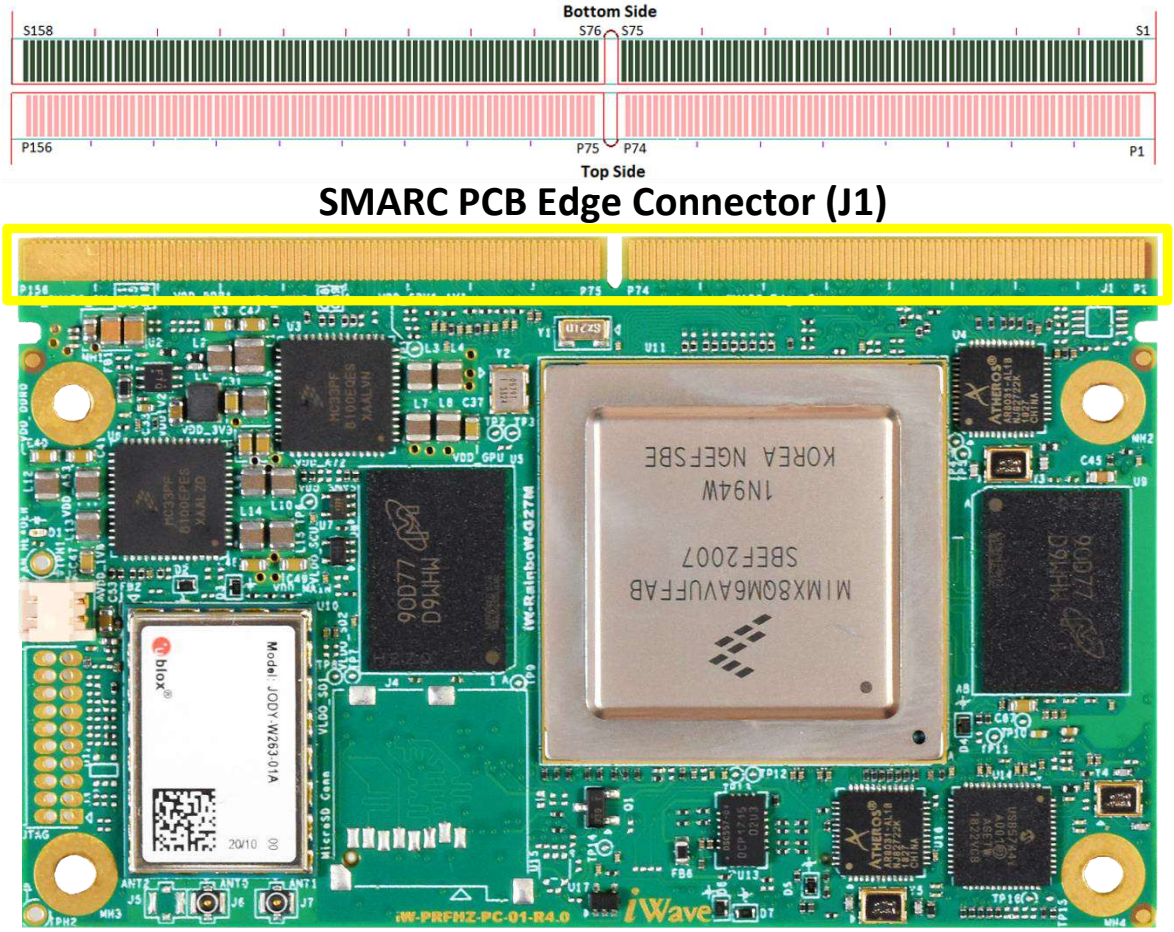

Figure 4: SMARC Edge Connector

Number of Pins - : 314

Connector Part - : Not Applicable (On Board PCB Edge connector)

Mating Connector - : 91782-3140M-001 from Aces

Table 3: SMARC Edge Connector Pinouts

Signal	SMARC Pin (Top)	SMARC Pin (Bottom)	Signal
SMB_ALERT(GPIO0_16)	**P1**	**S1**	MIPI_CSI1_I2C0_SCL
GND	**P2**	**S2**	MIPI_CSI1_I2C0_SDA
MIPI_CSI1_CLK_P	**P3**	**S3**	GND
MIPI_CSI1_CLK_N	**P4**	**S4**	NC
NC *(Note: Optionally* GBE1_PPS_SDP*)*	**P5**	**S5**	MIPI_CSI0_I2C0_SCL
NC *(Note: Optionally* GBE0_PPS_SDP*)*	**P6**	**S6**	MIPI_CSI0_MCLK_OUT
MIPI_CSI1_DATA0_P	**P7**	**S7**	MIPI_CSI0_I2C0_SDA
MIPI_CSI1_DATA0_N	**P8**	**S8**	MIPI_CSI0_CLK_P
GND	**P9**	**S9**	MIPI_CSI0_CLK_N
MIPI_CSI1_DATA1_P	**P10**	**S10**	GND
MIPI_CSI1_DATA1_N	**P11**	**S11**	MIPI_CSI0_DATA0_P
GND	**P12**	**S12**	MIPI_CSI0_DATA0_N
MIPI_CSI1_DATA2_P	**P13**	**S13**	GND
MIPI_CSI1_DATA2_N	**P14**	**S14**	MIPI_CSI0_DATA1_P
GND	**P15**	**S15**	MIPI_CSI0_DATA1_N
MIPI_CSI1_DATA3_P	**P16**	**S16**	GND
MIPI_CSI1_DATA3_N	**P17**	**S17**	GBE1_MDI0+
GND	**P18**	**S18**	GBE1_MDI0-
GBE0_MDI3-	**P19**	**S19**	GBE1_LINK100#
GBE0_MDI3+	**P20**	**S20**	GBE1_MDI1+
GBE0_LINK100#	**P21**	**S21**	GBE1_MDI1-
GBE0_LINK1000#	**P22**	**S22**	GBE1_LINK1000#
GBE0_MDI2-	**P23**	**S23**	GBE1_MDI2+
GBE0_MDI2+	**P24**	**S24**	GBE1_MDI2-
GBE0_LINK_ACT#	**P25**	**S25**	GND
GBE0_MDI1-	**P26**	**S26**	GBE1_MDI3+
GBE0_MDI1+	**P27**	**S27**	GBE1_MDI3-
VPHY0_DVDDL	**P28**	**S28**	VPHY1_DVDDL
GBE0_MDI0-	**P29**	**S29**	NC *(Note: Optionally SERDES0_TX+)*
GBE0_MDI0+	**P30**	**S30**	NC *(Note: Optionally SERDES0_TX-)*
SPI3_CS1	**P31**	**S31**	GBE1_LINK_ACT#
GND	**P32**	**S32**	NC *(Note: Optionally SERDES0_RX+)*
GPIO_SDC1_WP(GPIO1_22)	**P33**	**S33**	NC *(Note: Optionally SERDES0_RX+)*
USDHC1_CMD	**P34**	**S34**	GND

Signal	SMARC Pin (Top)	SMARC Pin (Bottom)	Signal
GPIO_SDC1_CD(GPIO1_23)	**P35**	**S35**	USB_HUB4OUT_DP
USDHC1_CLK	**P36**	**S36**	USB_HUB4OUT_DM
GPIO_SDC1_PWR_EN(GPIO1_19)	**P37**	**S37**	NC
GND	**P38**	**S38**	MCLK_OUT0
USDHC1_DATA0	**P39**	**S39**	SAI1_TXFS
USDHC1_DATA1	**P40**	**S40**	SAI1_TXD
USDHC1_DATA2	**P41**	**S41**	SAI1_RXD
USDHC1_DATA3	**P42**	**S42**	SAI1_TXC
SPI3_CS0	**P43**	**S43**	NC
SPI3_SCLK	**P44**	**S44**	NC
SPI3_MISO	**P45**	**S45**	NC *(Note: Optionally SMARC_MDIO_CLK)*
SPI3_MOSI	**P46**	**S46**	NC *(Note: Optionally SMARC_MDIO_DATA)*
GND	**P47**	**S47**	GND
PCIE_SATA0_TX0_P	**P48**	**S48**	DMA_I2C1_SCL
PCIE_SATA0_TX0_N	**P49**	**S49**	DMA_I2C1_SDA
GND	**P50**	**S50**	AUD_SAI0_TXFS(SPI2_CS1)
PCIE_SATA0_RX0_P	**P51**	**S51**	AUD_SAI0_TXD
PCIE_SATA0_RX0_N	**P52**	**S52**	AUD_SAI0_RXD
GND	**P53**	**S53**	AUD_SAI0_TXC
SPI2_CS0 *(Note: Optionally QSPI1A_SS0)*	**P54**	**S54**	SATA_ACT#(GPIO1_18)
QSPI1A_SS1	**P55**	**S55**	NC
SPI2_SCLK *(Note: Optionally QSPI1A_SCLK)*	**P56**	**S56**	QSPI1A_DATA2
SPI2_MISO *(Note: Optionally QSPI1A_DATA0)*	**P57**	**S57**	QSPI1A_DATA3
SPI2_MOSI *(Note: Optionally QSPI1A_DATA1)*	**P58**	**S58**	QSPI1A_RESET(GPIO4_22)
GND	**P59**	**S59**	NC
USB_OTG1_DP	**P60**	**S60**	NC
USB_OTG1_DM	**P61**	**S61**	GND
USB_OTG1_PWR(GPIO4_03)	**P62**	**S62**	USB3_HUB2_TXP
VBUS_OTG1	**P63**	**S63**	USB3_HUB2_TXM
USB_OTG_ID	**P64**	**S64**	GND
USB_HUB3OUT_DP	**P65**	**S65**	USB3_HUB2_RXP
USB_HUB3OUT_DM	**P66**	**S66**	USB3_HUB2_RXM
USB_HUB3_OC	**P67**	**S67**	GND
GND	**P68**	**S68**	USB_HUB2OUT_DP
USB_HUB1OUT_DP	**P69**	**S69**	USB_HUB2OUT_DM

Signal	SMARC Pin (Top)	SMARC Pin (Bottom)	Signal
USB_HUB1OUT_DM	**P70**	**S70**	GND
USB_HUB1_OC	**P71**	**S71**	USB3_HUB1_TXP
NC	**P72**	**S72**	USB3_HUB1_TXM
NC	**P73**	**S73**	GND
USB_HUB2_OC	**P74**	**S74**	USB3_HUB1_RXP
		S75	USB3_HUB1_RXM
Key			Key
PCIE_A_RST_B(GPIO4_29)	**P75**	**S76**	PCIE_B_RST_B(GPIO5_00)
USB_HUB4_OC	**P76**	**S77**	NC
NC *(Note: Optionally* PCIE_B_CKREQ_B*)*	**P77**	**S78**	NC *(Note: Optionally SERDES1_RX+)*
NC *(Note: Optionally* PCIE_A_CKREQ_B*)*	**P78**	**S79**	NC *(Note: Optionally SERDES1_RX-)*
GND	**P79**	**S80**	GND
NC	**P80**	**S81**	NC *(Note: Optionally SERDES1_TX+)*
NC	**P81**	**S82**	NC *(Note: Optionally SERDES1_TX-)*
GND	**P82**	**S83**	GND
PCIE_A_REFCLK_P	**P83**	**S84**	PCIE_B_REFCLK_P
PCIE_A_REFCLK_N	**P84**	**S85**	PCIE_B_REFCLK_N
GND	**P85**	**S86**	GND
PCIE0_A_RX0_P	**P86**	**S87**	PCIE1_B_RX0_P
PCIE0_A_RX0_N	**P87**	**S88**	PCIE1_B_RX0_N
GND	**P88**	**S89**	GND
PCIE0_A_TX0_P	**P89**	**S90**	PCIE1_B_TX0_P
PCIE0_A_TX0_N	**P90**	**S91**	PCIE1_B_TX0_N
GND	**P91**	**S92**	GND
HDMI_TX0_DATA2_P	**P92**	**S93**	NC *(Note: Optionally DP0_P)*
HDMI_TX0_DATA2_N	**P93**	**S94**	NC *(Note: Optionally DP0_N)*
GND	**P94**	**S95**	GPIO(GPIO3_23)
HDMI_TX0_DATA1_P	**P95**	**S96**	NC *(Note: Optionally DP1_P)*
HDMI_TX0_DATA1_N	**P96**	**S97**	NC *(Note: Optionally DP1_N)*
GND	**P97**	**S98**	NC *(Note: Optionally DP0_HPD)*
HDMI_TX0_DATA0_P	**P98**	**S99**	NC *(Note: Optionally DP2_P)*
HDMI_TX0_DATA0_N	**P99**	**S100**	NC *(Note: Optionally DP2_N)*
GND	**P100**	**S101**	GND
HDMI_TX0_CLK_P	**P101**	**S102**	NC *(Note: Optionally DP3_P)*
HDMI_TX0_CLK_N	**P102**	**S103**	NC *(Note: Optionally DP3_N)*

Signal	SMARC Pin (Top)	SMARC Pin (Bottom)	Signal
GND	**P103**	**S104**	NC *(Note: Optionally USB_OTG1_ID)*
HDMI_TX_HPD	**P104**	**S105**	NC *(Note: Optionally DP_AUX_P)*
HDMI_TX0_CTRL_CLK	**P105**	**S106**	NC *(Note: Optionally DP_AUX_N)*
HDMI_TX0_CTRL_DAT	**P106**	**S107**	LCD1_BKLT_EN(GPIO1_15)
NC *(Note: Optionally HDMI_TX0_CEC)*	**P107**	**S108**	LVDS1/DSI1_CH1_CLK_P
GPIO_0(GPIO1_27)	**P108**	**S109**	LVDS1/DSI1_CH1_CLK_N
GPIO_1(GPIO1_30)	**P109**	**S110**	GND
GPIO_2(GPIO1_28)	**P110**	**S111**	LVDS1/DSI1_CH1_TX0_P
GPIO_3(GPIO1_31)	**P111**	**S112**	LVDS1/DSI1_CH1_TX0_N
GPIO_4(GPIO4_11)	**P112**	**S113**	DSI1_TE(GPIO3_24)
GPIO_5(GPIO0_19)	**P113**	**S114**	LVDS1/DSI1_CH1_TX1_P
GPIO_6(GPIO0_00)	**P114**	**S115**	LVDS1/DSI1_CH1_TX1_N
GPIO_7(GPIO0_01)	**P115**	**S116**	LCD1_VDD_EN(GPIO1_14)
GPIO_8(GPIO0_02)	**P116**	**S117**	LVDS1/DSI1_CH1_TX2_P
GPIO_9(GPIO0_03)	**P117**	**S118**	LVDS1/DSI1_CH1_TX2_N
GPIO_10(GPIO0_04)	**P118**	**S119**	GND
GPIO_11(GPIO0_05)	**P119**	**S120**	LVDS1/DSI1_CH1_TX3_P
GND	**P120**	**S121**	LVDS1/DSI1_CH1_TX3_N
NC *(Note: Optionally SM_PMIC_I2C_SCL)*	**P121**	**S122**	LCD1_BL_PWM(GPIO1_10)
NC *(Note: Optionally SM_PMIC_I2C_SDA)*	**P122**	**S123**	NC *(Note: Optionally GPIO_13(GPIO1_29))*
BOOT_SEL0#	**P123**	**S124**	GND
BOOT_SEL1#	**P124**	**S125**	LVDS1/DSI0_CH0_TX0_P
BOOT_SEL2#	**P125**	**S126**	LVDS1/DSI0_CH0_TX0_N
RESET_OUT	**P126**	**S127**	LCD0_1_EN(GPIO1_08)
RESET_IN#	**P127**	**S128**	LVDS1/DSI0_CH0_TX1_P
ON_OFF_BUTTON	**P128**	**S129**	LVDS1/DSI0_CH0_TX1_N
UART0_TX	**P129**	**S130**	GND
UART0_RX	**P130**	**S131**	LVDS1/DSI0_CH0_TX2_P
UART0_RTS_B	**P131**	**S132**	LVDS1/DSI0_CH0_TX2_N
UART0_CTS_B	**P132**	**S133**	LCD0_VDD_EN(GPIO1_09)
GND	**P133**	**S134**	LVDS1/DSI0_CH0_CLK_P
UART3_TX	**P134**	**S135**	LVDS1/DSI0_CH0_CLK_N
UART3_RX	**P135**	**S136**	GND
NC*(Note: Optionally UART1_TX)*	**P136**	**S137**	LVDS1/DSI0_CH0_TX3_P
NC*(Note: Optionally UART1_RX)*	**P137**	**S138**	LVDS1/DSI0_CH0_TX3_N
NC *(Note: Optionally UART1_RTS_B)*	**P138**	**S139**	LVDS_I2C_SCL
NC *(Note: Optionally UART1_CTS_B)*	**P139**	**S140**	LVDS_I2C_SDA

Signal	SMARC Pin (Top)	SMARC Pin (Bottom)	Signal
UART4_TX	**P140**	**S141**	LCD0_BL_PWM(GPIO1_04)
UART4_RX	**P141**	**S142**	NC (Note: Optionally GPIO_12(GPIO2_24))
GND	**P142**	**S143**	GND
FLEXCAN0_TX	**P143**	**S144**	DSI0_TE(GPIO3_25)
FLEXCAN0_RX	**P144**	**S145**	NC (*Note: Optionally SCU_WDOG_OUT)*
FLEXCAN1_TX	**P145**	**S146**	PCIE_A_WAKE_B(GPIO4_28)
FLEXCAN1_RX	**P146**	**S147**	VDD_RTC
VDD_IN	**P147**	**S148**	NC
VDD_IN	**P148**	**S149**	NC
VDD_IN	**P149**	**S150**	VIN_PWR_BAD#
VDD_IN	**P150**	**S151**	NC
VDD_IN	**P151**	**S152**	NC
VDD_IN	**P152**	**S153**	CARRIER_STBY#
VDD_IN	**P153**	**S154**	CARRIER_PWR_ON
VDD_IN	**P154**	**S155**	FORCE_RECOV#
VDD_IN	**P155**	**S156**	NC
VDD_IN	**P156**	**S157**	TEST_MODE_SELECT
		S158	GND

2.7.1 Gigabit Ethernet

The i.MX8 QM/QP SMARC SOM supports two Gigabit Ethernet using two on SOM Ethernet PHY “AR8031” from Atheros, Qualcomm. ENET0 and ENET1 of i.MX8 are connected to GBE0 and GBE1 ports of SMARC edge connector respectively. The AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements.

For more details on GBE0 pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P6	GBE0_PPS_SDP	NA	IO, 3.3V CMOS	NC. *Note: Optionally connected to GBE0_PPS_SDP*
P19	GBE0_MDI3-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 negative.

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P20	GBE0_MDI3+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 positive.
P21	GBE0_LINK100#	NA	O, 3.3V CMOS	100Mbps Ethernet link status LED. *Note: Connect to Cathode of LED.*
P22	GBE0_LINK1000#	NA	O, 3.3V CMOS 68K PD	Gigabit Ethernet link status LED. *Note: Connect to Cathode of LED.*
P23	GBE0_MDI2-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 negative.
P24	GBE0_MDI2+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 positive.
P25	GBE0_LINK_ACT#	NA	O, 3.3V CMOS 68K PD	Gigabit Ethernet activity status *Note: Connect to Cathode of LED.*
P26	GBE0_MDI1-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 negative.
P27	GBE0_MDI1+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 positive.
P28	VPHY0_DVDDL	NA	Power	Power for the Centre Tap of Mack Jack connector
P29	GBE0_MDI0-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 negative.
P30	GBE0_MDI0+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 positive.

For more details on GBE1 pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P5	GBE1_PPS_SDP	NA	IO, 3.3V CMOS	NC. *Note: Optionally connected to GBE1_PPS_SDP*
S17	GBE1_MDI0+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 positive.
S18	GBE1_MDI0-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 0 negative.
S19	GBE1_LINK100#	NA	O, 3.3V CMOS	100Mbps Ethernet link status LED *Note: Connect to Cathode of LED.*
S20	GBE1_MDI1+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 positive.
S21	GBE1_MDI1-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 1 negative.
S22	GBE1_LINK1000#	NA	O, 3.3V CMOS 68K PD	1000Mbps Ethernet link status LED *Note: Connect to Cathode of LED.*
S23	GBE1_MDI2+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 2 positive.
S24	GBE1_MDI2-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair2 negative.
S26	GBE1_MDI3+	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 positive.

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S27	GBE1_MDI3-	NA	IO, GBE	Second Gigabit Ethernet MDI differential pair 3 negative.
S28	VPHY1_DVDDL	NA	Power	Power for the Centre Tap of Mack Jack connector.
S31	GBE1_LINK_ACT#	NA	O, 3.3V CMOS 68K PD	Ethernet Activity status LED. *Note: Connect to Cathode of LED.*

2.7.2 SERDES and MDIO Interface (Optional)

The i.MX8 QM/QP SMARC SOM optionally supports two SERDES interface support on the SMARC Edge using the two on SOM Ethernet PHY "AR8031" from Atheros, Qualcomm and a MDIO support from the ENET MDIO (Either ENET0 or ENET1) of the i.MX8 processor on the SMARC Edge connector. SERDES0 and SERDES1 are from the first and second Ethernet PHY and are optionally connected to SERDES0 and SERDES1 of SMARC edge connector respectively.

For more details on SERDES and MDIO pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S29	SERDES0_TX+	NA	O, PCIE	NC. *Note: Optionally connected to SERDES0_SO_P*
S30	SERDES0_TX-	NA	O, PCIE	NC. *Note: Optionally connected to SERDES0_SO_N*
S32	SERDES0_RX+	NA	I, PCIE	NC. *Note: Optionally connected to SERDES0_SI_P*
S33	SERDES0_RX-	NA	I, PCIE	NC. *Note: Optionally connected to SERDES0_SI_N*
S45	SMARC_MDIO_CLK	NA	O, 1.8V CMOS	NC. *Note: Optionally connected to ENET0_MDC or ENET1_MDC*
S46	SMARC_MDIO_DATA	NA	IO, 1.8V CMOS	NC. *Note: Optionally connected to ENET0_MDC or ENET1_MDC*
S78	SERDES1_RX+	NA	I, PCIE	NC. *Note: Optionally connected to SERDES1_SI_P*
S79	SERDES1_RX-	NA	I, PCIE	NC. *Note: Optionally connected to SERDES1_SI_N*
S81	SERDES1_TX+	NA	O, PCIE	NC. *Note: Optionally connected to SERDES1_SO_P*
S82	SERDES1_TX-	NA	O, PCIE	NC. *Note: Optionally connected to SERDES1_SO_N*

2.7.3 SD Interface

The i.MX8 SMARC SOM supports 4bit SD interface over SMARC PCB Edge connector which can be used to connect SD card as Mass storage or optional boot device. uSDHC1 controller of the i.MX8 CPU is used to support SMARC SD interface. uSDHC1 operates both in 3.3V and 1.8V IO level and supports maximum of 208 Mbit/s per line with 1.8V IO voltage in SDR mode. Whereas Controlling GPIOs like Write Protect and Card detect signals are of 3.3V IO level.

For more details on SD pinouts, refer below Table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P33	GPIO_SDC1_WP (GPIO1_22)	MIPI_DSI1_GPIO0_00/ BM24	I, 3.3V CMOS 10K PU	SD write Protect.
P34	USDHC1_CMD	USDHC1_CMD/ G41	IO, 1.8/3.3V CMOS	SD command. *Note: 10K pullup option is provided.*
P35	GPIO_SDC1_CD (GPIO1_23)	MIPI_DSI1_GPIO0_01/ BK24	I, 3.3V/CMOS 10K PU	SD Card Detect.
P36	USDHC1_CLK	USDHC1_CLK/ J39	O, 1.8/3.3V CMOS	SD Clock *Note: 1K pullup option is provided.*
P37	GPIO_SDC1_PWR_EN (GPIO1_19)	MIPI_DSI0_GPIO0_01/BD28	O, 3.3V CMOS	SD Power enable.
P39	USDHC1_DATA0	USDHC1_DATA0 / E37	IO, 1.8/3.3V CMOS	SD data 0 *Note: 10K pullup option is provided.*
P40	USDHC1_DATA1	USDHC1_DATA1 / F38	IO, 1.8/3.3V CMOS	SD data 1. *Note: 10K pullup option is provided*
P41	USDHC1_DATA2	USDHC1_DATA2 / E39	IO, 1.8/3.3V CMOS	SD data 2. *Note: 10K pullup option is provided*
P42	USDHC1_DATA3	USDHC1_DATA3 / F40	IO, 1.8/3.3V CMOS	SD data 3. *Note: 10K pullup option is provided*

2.7.4 USB Interface

The i.MX8 CPU supports two USB2.0 OTG and one USB_SS3. In i.MX8 SMARC SOM USB_OTG1 goes to SMARC OTG connector and USB_OTG2 goes to on SOM USB3.0 hub USB5744-I/2G from Microchip along with CPUs USB_SS3 lines. USB Hub feature's controller IC with 4 USB 3.1 Gen 1 / USB 2.0 downstream ports. The Downstream ports of Hub are connected to SMARC Edge connector and Expansion connector.

For more details on USB pinouts near SMARC edge connector, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P60	USB_OTG1_DP	USB_OTG1_DP / B40	IO, USB	USB2.0 Port0 Data Plus.
P61	USB_OTG1_DM	USB_OTG1_DM / C39	IO, USB	USB2.0 Port0 Data Minus.

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P62	USB_OTG1_PWR (GPIO4_03)	USB_SS3_TC0/ J9	IO, 3.3V CMOS	USB Port0 Power Enable/ Over Current Indicator.
P63	VBUS_OTG1	USB_OTG1_VBUS/ A39	5V, Power	USB host power detection, when this port is used as a device.
P64	USB_OTG_ID	USB_OTG1_ID/ A37	I, 3.3V CMOS	USB0 OTG ID. *Note: 1.8V to 3.3V level translator is used to match SMARC specification.*
P65	USB_HUB3OUT_DP	NA	IO, USB	USB2.0 Port1 Data Plus. *Note: Connected to USB Hub.*
P66	USB_HUB3OUT_DM	NA	IO, USB	USB2.0 Port1 Data Minus. *Note: Connected to USB Hub.*
P67	USB_HUB3_OC	NA	IO, 3.3V CMOS 10K PU	USB Port1 Over Current Indicator. *Note: Connected to USB Hub.*
P69	USB_HUB1OUT_DP	NA	IO, USB	USB2.0 Port2 Data Plus. *Note: Connected to USB Hub.*
P70	USB_HUB1OUT_DM	NA	IO, USB	USB2.0 Port2 Data Minus. *Note: Connected to USB Hub.*
P74	USB_HUB2_OC	NA	IO, 3.3V CMOS 10K PU	USB Port3 Over Current Indicator. *Note: Connected to USB Hub.*
P76	USB_HUB4_OC	NA	IO, 3.3V CMOS 10K PU	USB Port4 Over Current Indicator. *Note: Connected to USB Hub.*
S62	USB3_HUB2_TXP	NA	O, USB SS	USB3.0 Port3 Transmit Plus. *Note: Connected to USB Hub.*
S63	USB3_HUB2_TXM	NA	O, USB SS	USB3.0 Port3 Transmit Minus. *Note: Connected to USB Hub.*
S65	USB3_HUB2_RXP	NA	I, USB SS	USB3.0 Port3 Receive Plus. *Note: Connected to USB Hub.*
S66	USB3_HUB2_RXM	NA	I, USB SS	USB3.0 Port3 Receive Minus. *Note: Connected to USB Hub.*
S68	USB_HUB2OUT_DP	NA	IO, USB	USB2.0 Port3 Data Plus. *Note: Connected to USB Hub.*
S69	USB_HUB2OUT_DM	NA	IO, USB	USB2.0 Port3 Data Minus. *Note: Connected to USB Hub.*
S71	USB3_HUB1_TXP	NA	O, USB SS	USB3.0 Port2 Transmit Plus. *Note: Connected to USB Hub.*
S72	USB3_HUB1_TXM	NA	O, USB SS	USB3.0 Port2 Transmit Minus. *Note: Connected to USB Hub.*
S74	USB3_HUB1_RXP	NA	I, USB SS	USB3.0 Port2 Receive Plus. *Note: Connected to USB Hub.*
S75	USB3_HUB1_RXM	NA	I, USB SS	USB3.0 Port2 Receive Minus. *Note: Connected to USB Hub.*

For more details on USB3.0 pinouts near Expansion connector(J8), refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
2	USB3_HUB3_TXP	NA	O, USB	USB3.0 Hub Transmit channel 3 Plus.
4	USB3_HUB3_TXM	NA	O, USB	USB3.0 Hub Transmit channel 3 Minus.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
8	USB3_HUB3_RXP	NA	I, USB	USB3.0 Hub Receive channel 3 Plus.
10	USB3_HUB3_RXM	NA	I, USB	USB3.0 Hub Receive channel 3 Minus.
14	USB3_HUB4_TXP	NA	O, USB SS	USB3.0 Hub Transmit channel 4 Plus.
16	USB3_HUB4_TXM	NA	O, USB SS	USB3.0 Hub Transmit channel 4 Minus.
20	USB3_HUB4_RXP	NA	I, USB SS	USB3.0 Hub Receive channel 4 Plus.
22	USB3_HUB4_RXM	NA	I, USB SS	USB3.0 Hub Receive channel 4 Minus.

2.7.5 PCIe Interface

The i.MX8 CPU supports two Lane PCI Express -3.0 (PCIe gen3: 8GHz to get 8GHz baud clock) channels. In i.MX8 SMARC SOM PCIe0 and PCIe1 lane are connected to PCIeA and PCIeB lanes of SMARC Edge connector respectively and as per SMARC specification TX lines are AC coupled with 0.22uF capacitors. Also, 100MHz reference clock is provided for both Channel A & Channel B from a single 100MHz Oscillator.

For more details on PCIe pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P75	PCIE_A_RST_B (GPIO4_29)	PCIE_CTRL0_ PERST_B/D20	O, 3.3V CMOS	PCIe Channel-A Reset Out.
P77	PCIE_B_CKREQ_B	NA	I,3.3V CMOS	NC. *Note: Optionally connected to PCIE_B_CKREQ_B*
P78	PCIE_A_CKREQ_B	NA	I,3.3V CMOS	NC. *Note: Optionally connected to PCIE_B_CKREQ_A*
P83	PCIE_A_REFCLK_P	NA	O, PCIe	PCIe Channel-A Clock Positive. *Note: From External Oscillator.*
P84	PCIE_A_REFCLK_N	NA	O, PCIe	PCIe Channel-A Clock Negative. *Note: From External Oscillator.*
P86	PCIE0_A_RX0_P	PCIE0_RX0_P/ A29	I, PCIe	PCIe Channel-A Receive Positive.
P87	PCIE0_A_RX0_N	PCIE0_RX0_N/ B30	I, PCIe	PCIe Channel-A Receive Negative.
P89	PCIE0_A_TX0_P	PCIE0_TX0_P/ B26	O, PCIe / 0.22uF AC Couple	PCIe Channel-A Transmit Positive.
P90	PCIE0_A_TX0_N	PCIE0_TX0_N/ C27	O, PCIe / 0.22uF AC Couple	PCIe Channel-A Transmit Negative.
S76	PCIE_B_RST_B (GPIO5_00)	PCIE_CTRL1_ PERST_B/G25	O, 3.3V CMOS	PCIe Channel-B RESET OUT.
S84	PCIE_B_REFCLK_P	NA	O, PCIe	PCIe Channel-B Clock Positive. *Note: From External Oscillator.*
S85	PCIE_B_REFCLK_N	NA	O, PCIe	PCIe Channel-B Clock Negative. *Note: From External Oscillator.*
S87	PCIE1_B_RX0_P	PCIE1_RX0_P/ A21	I, PCIe	PCIe Channel-B Receiver Positive.

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S88	PCIE1_B_RX0_N	PCIE1_RX0_N/ B22	I, PCIe	PCIe Channel-B Receiver Negative.
S90	PCIE1_B_TX0_P	PCIE1_TX0_P/ B24	O, PCIe / 0.22uF AC Couple	PCIe Channel-B Transmitter Positive.
S91	PCIE1_B_TX0_N	PCIE1_TX0_N/ C25	O, PCIe / 0.22uF AC Couple	PCIe Channel-B Transmitter Negative.

2.7.6 SATA Interface

The i.MX8 CPU supports SATA-3(Gen3: 6GHz to get 6GHz baud clock). This is in addition to the standard PCIe 3.0 and connected to SMARC SATA Edge connector pins via 0.022uF AC coupled capacitors on both TX an RX lines.

For more details on SATA pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P48	PCIE_SATA0_TX0_P	PCIE_SATA0_ TX0_P/ B16	O, SATA / 0.022uF AC Couple	SATA Transmit Lane Positive
P49	PCIE_SATA0_TX0_N	PCIE_SATA0_ TX0_N/ C17	O, SATA / 0.022uF AC Couple	SATA Transmit Lane Negative
P51	PCIE_SATA0_RX0_P	PCIE_SATA0_ RX0_P/ A19	I, SATA / 0.022uF AC Couple	SATA Receive Lane Positive
P52	PCIE_SATA0_RX0_N	PCIE_SATA0_ RX0_N/ B20	I, SATA / 0.022uF AC Couple	SATA Receive Lane Negative
S54	SATA_ACT# (GPIO1_18)	MIPI_DSI0_ GPIO0_00/BD30	O, 3.3V CMOS	GPIO used as SATA Activity indication

2.7.7 MIPI CSI Camera

The i.MX8 CPU supports two 4-lane camera interfaces, the CSI-2 Rx Controller Core implements all three layers defined by the CSI-2 Specification: Pixel to Byte Packing, Low Level Protocol, and Lane Management. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The Local Interface is an easy to use pixel-based interface that supports 1 to 4 virtual channels and all data types. The Local interface runs at the User Interface clock rate for all implementations. The CSI-2 Rx Controller Core takes care of all packet formatting details and transmission over the MIPI bus. The i.MX8 SMARC SOM supports one two lane and one four lane MIPI CSI camera interface via SMARC Edge connector along with the other controlling signals. Here all CSI1 lane [3:0] are connected to SMARC edge connector, but only CSI0 lane [1:0] are connected to SMARC edge connector whereas CSI0 lane [3:2] are connected to expansion connector.

For more details on MIPI CSI0 SMARC pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S5	MIPI_CSI0_I2C0_SCL	MIPI_CSI0_I2C0 _SCL/ BH24	O, 1.8V CMOS/ 2.2K PU	MIPI CSI0 I2C Clock.

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S6	MIPI_CSI0_MCLK_OUT	MIPI_CSI0_MCLK_OUT /BJ23	O, 1.8V CMOS	Master Clock for Camera.
S7	MIPI_CSI0_I2C0_SDA	MIPI_CSI0_I2C0_SDA /BN19	IO, 1.8V CMOS/ 2.2K PU	MIPI CSI0 I2C Data.
S8	MIPI_CSI0_CLK_P	MIPI_CSI0_CLK_P /BF20	I, MIPI	MIPI CSI0 differential Clock positive.
S9	MIPI_CSI0_CLK_N	MIPI_CSI0_CLK_N /BE21	I, MIPI	MIPI CSI0 differential Clock negative.
S11	MIPI_CSI0_DATA0_P	MIPI_CSI0_DATA0_P/ BF22	I, MIPI	MIPI CSI0 differential data lane 0 positive.
S12	MIPI_CSI0_DATA0_N	MIPI_CSI0_DATA0_N/BE23	I, MIPI	MIPI CSI0 differential data lane 0 negative.
S14	MIPI_CSI0_DATA1_P	MIPI_CSI0_DATA1_P/BE19	I, MIPI	MIPI CSI0 differential data lane 1 positive.
S15	MIPI_CSI0_DATA1_N	MIPI_CSI0_DATA1_N/BF18	I, MIPI	MIPI CSI0 differential data lane 1 negative.

For more details on MIPI CSI0 signal connection on Expansion connector, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
80	MIPI_CSI0_DATA2_P	MIPI_CSI0_DATA2_P/BF24	I, MIPI	MIPI CSI0 differential data lane 2 positive.
82	MIPI_CSI0_DATA2_N	MIPI_CSI0_DLN2_M/BE25	I, MIPI	MIPI CSI0 differential data lane 2 negative.
86	MIPI_CSI0_DATA3_P	MIPI_CSI0_DLN3_P/BF16	I, MIPI	MIPI CS0 differential data lane 3 positive.
88	MIPI_CSI0_DATA3_N	MIPI_CSI0_DLN3_M/BE17	I, MIPI	MIPI CSI0 differential data lane 3 negative.

For more details on MIPI CSI1 SMARC pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S1	MIPI_CSI1_I2C0_SCL	MIPI_CSI1_I2C0_SCL/BN17	O, 1.8V CMOS/ 2.2K PU	MIPI CSI1 I2C Clock.
S2	MIPI_CSI1_I2C0_SDA	MIPI_CSI1_I2C0_SDA /BE15	IO, 1.8V CMOS/ 2.2K PU	MIPI CSI1 I2C Data.
P3	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/BJ17	I, MIPI	MIPI CSI1 differential clock positive.
P4	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/BH16	I, MIPI	MIPI CSI1 differential clock negative.
P7	MIPI_CSI1_DATA0_P	MIPI_CSI1_DATA0_P/BH18	I, MIPI	MIPI CSI1 differential data lane 0 positive.
P8	MIPI_CSI1_DATA0_N	MIPI_CSI1_DATA0_N /BJ19	I, MIPI	MIPI CSI1 differential data lane 0 negative.

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P10	MIPI_CSI1_DATA1_P	MIPI_CSI1_ DATA1_P/BJ15	I, MIPI	MIPI CSI1 differential data lane 1 positive.
P11	MIPI_CSI1_DATA1_N	MIPI_CSI1_ DATA1_N/BH14	I, MIPI	MIPI CSI1 differential data lane 1 negative.
P13	MIPI_CSI1_DATA2_P	MIPI_CSI1_ DATA2_P/BJ21	I, MIPI	MIPI CSI1 differential data lane 2 positive.
P14	MIPI_CSI1_DATA2_N	MIPI_CSI1_ DATA2_N/BH20	I, MIPI	MIPI CSI1 differential data lane 2 negative.
P16	MIPI_CSI1_DATA3_P	MIPI_CSI1_ DATA3_P/BJ13	I, MIPI	MIPI CSI1 differential data lane 3 positive.
P17	MIPI_CSI1_DATA3_N	MIPI_CSI1_ DATA3_N/BH12	I, MIPI	MIPI CSI1 differential data lane 3 negative.

2.7.8 HDMI/Display Port Interface

The i.MX8 CPU's HD Display Transmitter Controller IP offers multi-protocol support of standards such as High Definition Multimedia Interface (HDMI), DisplayPort, embedded DisplayPort (eDP), with one of these standards supported at a time. These protocols enable switching between the modes to be applied on a system level and performed by means of software configuration. i.MX8 CPU supports HDMI 1.4 Specification, HDMI 2.0a Specification, DisplayPort Specification Version 1.3 and eDP Specification Version 1.4 protocols.

In i.MX8 SMARC SOM, HDMI Display Transmitter output is connected to HDMI pins of SMARC edge connector and also optionally connected to Display Port0 (DP0) pins of SMARC Edge connector. For more details on HDMI pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P92	HDMI_TX0_DATA2_P	HDMI_TX0_DATA2 _EDP0_P/BL9	O, HDMI	HDMI differential data lane 2 Positive
P93	HDMI_TX0_DATA2_N	HDMI_TX0_DATA2 _EDP0_N/BM8	O, HDMI	HDMI differential data lane 2 Negative
P95	HDMI_TX0_DATA1_P	HDMI_TX0_DATA1 _EDP1_P/BL7	O, HDMI	HDMI differential data lane 1 Positive
P96	HDMI_TX0_DATA1_N	HDMI_TX0_DATA1 _EDP1_N/BM6	O, HDMI	HDMI differential data lane 1 Negative
P98	HDMI_TX0_DATA0_P	HDMI_TX0_DATA0 _EDP2_P/BL5	O, HDMI	HDMI differential data lane 0 Positive
P99	HDMI_TX0_DATA0_N	HDMI_TX0_DATA0 _EDP2_N/BM4	O, HDMI	HDMI differential data lane 0 Negative
P101	HDMI_TX0_CLK_P	HDMI_TX0_CLK _EDP3_P/BL3	O, HDMI	HDMI differential CLK Positive
P102	HDMI_TX0_CLK_N	HDMI_TX0_CLK _EDP3_N/BK2	O, HDMI	HDMI differential CLK Negative
P104	HDMI_TX_HPD	HDMI_TX_HPD / BH8	I, 1.8V CMOS	HDMI Hot Plug Detect

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P105	HDMI_TX0_CTRL_CLK	HDMI_TX0_DDC _SCL /BG1 Or EDP_AUX_P/BH2	O, 1.8V CMOS/ 100K PU	HDMI DDC I2C Clock *Note: Optionally connected to CPU ball BH2.*
P106	HDMI_TX0_CTRL_DAT	HDMI_TX0_DDC _SDA /BN5 Or EDP_AUX_N/BG3	IO, 1.8V CMOS/ 100K PU	HDMI DDC I2C DATA *Note: Optionally connected to CPU ball BG3.*

Note: In default configuration HDMI is supported, contact iWave support team if eDP or DP supported SOM is required or refer Application Note: "AN2701-i.MX8 QM SMARC SOM-Enabling DP Support in SMARC Edge-Application Note-R4.0-REL1.0.pdf"

For more details on DP pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S93	DP0_P	HDMI_TX0_DATA2 _EDP0_P/ BL9	O, DP	NC. *Note: Optionally connected to Display Port Lane 0 Positive*
S94	DP0_N	HDMI_TX0_DATA2 _EDP0_N/ BM8	O, DP	NC. *Note: Optionally connected to Display Port Lane 0 Negative*
S95	DP0_AUX_SEL (GPIO3_23)	ADC_IN5/ AR7	IO, 1.8V CMOS	GPIO3_23 is connected for Display Port AUX Select.
S96	DP1_P	HDMI_TX0_DATA1 _EDP1_P/ BL7	O, DP	NC. *Note: Optionally connected to Display Port Lane 1 Positive*
S97	DP1_N	HDMI_TX0_DATA1 _EDP1_N/ BM6	O, DP	NC. *Note: Optionally connected to Display Port Lane 1 Negative*
S98	DP0_HPD	HDMI_TX_HPD / BH8 or GPIO3_22/ AN9	I, 1.8V CMOS	NC. *Note: Optionally connected to Display Port Hot Plug Detect.* *Note: Also Optionally connected to GPIO3_22 GPIO*
S99	DP2_P	HDMI_TX0_DATA0 _EDP2_P/ BL5	O, DP	NC. *Note: Optionally connected to Display Port Lane 2 Positive*
S100	DP2_N	HDMI_TX0_DATA0 _EDP2_N/ BM4	O, DP	NC. *Note: Optionally connected to Display Port Lane 2 Negative*
S102	DP3_P	HDMI_TX0_CLK _EDP3_P/ BL3	O, DP	NC. *Note: Optionally connected to Display Port Lane 3 Positive*
S103	DP3_N	HDMI_TX0_CLK _EDP3_N/ BK2	O, DP	NC. *Note: Optionally connected to Display Port Lane 3 Negative*

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S105	DP_AUX_P	EDP_AUX_P/BH2 Or HDMI_TX0_DDC _SCL /BG1	O, 1.8V CMOS/ 0.1uF AC Couple	NC. *Note: Optionally connected to Display Port AUX Positive*
S106	DP_AUX_N	EDP_AUX_N/BG3 Or HDMI_TX0_DDC _SDA /BN5	IO, 1.8V CMOS/ 0.1uF AC Couple	NC. *Note: Optionally connected to Display Port AUX Negative*

2.7.9 MIPI DSI/LVDS Display Interface

SMARC Specification supports two display interfaces over edge connector, which can be either LVDS or MIPI DSI display. The i.MX8 CPU supports two MIPI DSI and four LVDS display channels. An option is provided on i.MX8 SMARC SOM to support either LVDS or MIPI DSI over the edge connector and in default configuration MIPI DSI is supported.

The i.MX8 CPU MIPI_DSI standard controller is a flexible, high-performance, and easy-to-use digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals. The MIPI DSI D-PHY is a high frequency, low power, low-cost, source-synchronous, physical layer supporting the MIPI Alliance standard for D-PHY.

For more details on DSI pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S107	LCD1_BKLT_EN (GPIO1_15)	LVDS1_I2C1_SDA/ BN35	O, 1.8V CMOS	LCD1 Backlight Enable
S108	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK _P /BG31 or LVDS1_CH1_CLK _P/ BM34	O, MIPI	MIPI DSI1 differential Clock positive *Note: Optionally connected to LVDS1_CH1 differential Clock positive*
S109	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK _N /BH30 or LVDS1_CH1_CLK _N/ BK34	O, MIPI	MIPI DSI1 differential Clock negative *Note: Optionally connected to LVDS1_CH1 differential Clock negative*
S111	MIPI_DSI1_TX0_P	MIPI_DSI1_DATA0 _P /BG33 or LVDS1_CH1_TX0 _P/ BN37	O, MIPI	MIPI DSI1 differential data lane 0 positive *Note: Optionally connected to LVDS1_CH1 differential data lane 0 positive*
S112	MIPI_DSI1_TX0_N	MIPI_DSI1_DATA0 _N/ BH32 or LVDS1_CH1_TX0 _N/ BL37	O, MIPI	MIPI DSI1 differential data Lane 0 negative *Note: Optionally connected to LVDS1_CH1 differential data Lane 0 negative*

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S114	MIPI_DSI1_TX1_P	MIPI_DSI1_DATA1_P /BG29 or LVDS1_CH1_TX1_P/ BM38	O, MIPI	MIPI DSI1 differential data lane 1 positive *Note: Optionally connected to LVDS1_CH1 differential data lane 1 positive*
S115	MIPI_DSI1_TX1_N	MIPI_DSI1_DATA1_N/BH28 or LVDS1_CH1_TX1_N/ BK32	O, MIPI	MIPI DSI1 differential data lane 1 negative *Note: Optionally connected to LVDS1_CH1 differential data lane 1 negative*
S116	LCD1_VDD_EN (GPIO1_14)	LVDS1_I2C1_SCL/ BD32	O, 1.8V CMOS	LCD1Power Enable
S117	MIPI_DSI1_TX2_P	MIPI_DSI1_DATA2_P /BG35 or LVDS1_CH1_TX2_P/ BN31	O, MIPI	MIPI DSI1 differential data lane 2 positive *Note: Optionally connected to LVDS1_CH1 differential data lane 2 positive*
S118	MIPI_DSI1_TX2_N	MIPI_DSI1_DATA2_N/BH34 or LVDS1_CH1_TX2_N/ BL31	O, MIPI	MIPI DSI1 differential data lane 2 negative *Note: Optionally connected to LVDS1_CH1 differential data lane 2 negative*
S120	MIPI_DSI1_TX3_P	MIPI_DSI1_DATA3_P /BG27 or LVDS1_CH1_TX3_P/ BM30	O, MIPI	MIPI DSI1 differential data lane 3 positive *Note: Optionally connected to LVDS1_CH1 differential data lane 3 positive*
S121	MIPI_DSI1_TX3_N	MIPI_DSI1_DATA3_N/ BH26 or LVDS1_CH1_TX3_N/ BK30	O, MIPI	MIPI DSI1 differential data lane 3 negative *Note: Optionally connected to LVDS1_CH1 differential data lane 3 negative*
S122	LCD1_BL_PWM (GPIO1_10)	LVDS1_GPIO00/ BD34	O, 1.8V CMOS	LCD0 Back Light Brightness control PWM
S125	MIPI_DSI0_TX0_P	MIPI_DSI0_DATA0_P /BK28 or LVDS1_CH0_TX0_P/ BN37	O, MIPI	MIPI DSI0 differential data lane 0 positive *Note: Optionally connected to LVDS1_CH0 differential data lane 0 positive*
S126	MIPI_DSI0_TX0_N	MIPI_DSI0_DATA0_N/ BM28 or LVDS1_CH0_TX0_N/ BL37	O, MIPI	MIPI DSI0 differential data lane 0 negatives *Note: Optionally connected to LVDS1_CH0 differential data lane 0 negative*
S127	LCD0_1_EN (GPIO1_08)	LVDS0_I2C1_SCL/ BE37	O, 1.8V CMOS	LCD0 Backlight Enable
S128	MIPI_DSI0_TX1_P	MIPI_DSI0_DATA1_P /BK26 or	O, MIPI	MIPI DSI0 differential data lane 1 positive

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
		LVDS1_CH0_TX1 _P/ BM38		*Note: Optionally connected to LVDS1_CH0 differential data lane 1 positive*
S129	MIPI_DSI0_TX1_N	MIPI_DSI0_DATA1 _N/ BM26 or LVDS1_CH0_TX1 _N/ BK38	O, MIPI	MIPI DSI0 differential data lane 1 negative *Note: Optionally connected to LVDS1_CH0 differential data lane 1 negative*
S131	MIPI_DSI0_TX2_P	MIPI_DSI0_DATA2 _P /BL29 or LVDS1_CH0_TX2 _P/ BN39	O, MIPI	MIPI DSI0 differential data lane 2 positive *Note: Optionally connected to LVDS1_CH0 differential data lane 2 positive*
S132	MIPI_DSI0_TX2_N	MIPI_DSI0_DATA2 _N/ BN29 or LVDS1_CH0_TX2 _N/ BL39	O, MIPI	MIPI DSI0 differential data lane 2 negative *Note: Optionally connected to LVDS1_CH0 differential data lane 2 negative*
S133	LCD0_VDD_EN (GPIO1_09)	LVDS0_I2C1_SDA/ BE35	O, 1.8V CMOS	LCD0 Power Enable
S134	MIPI_DSI0__CLK_P	MIPI_DSI0_CLK _P /BL27 or LVDS1_CH0_CLK _P/ BM36	O, MIPI	MIPI DSI0 differential Clock positive *Note: Optionally connected to LVDS1_CH0 differential Clock positive*
S135	MIPI_DSI0_CLK_N	MIPI_DSI0_CLK _N /BN27 or LVDS1_CH0_CLK _N/ BK36	O, MIPI	MIPI DSI0 differential Clock negative *Note: Optionally connected to LVDS1_CH0 differential Clock negative*
S137	MIPI_DSI0_TX3_P	MIPI_DSI0_DATA3 _P /BL25 or LVDS1_CH0_TX3 _P/ BM40	O, MIPI	MIPI DSI0 differential data lane 3 positive *Note: Optionally connected to LVDS1_CH0 differential data lane 3 positive*
S138	MIPI_DSI0_TX3_N	MIPI_DSI0_DATA3 _N/BN25 or LVDS1_CH0_TX3 _N/ BK40	O, MIPI	MIPI DSI0 differential data lane 3 negative *Note: Optionally connected to LVDS1_CH0 differential data lane 3 negative*
S139	LCD_I2C_SCL	LVDS0_I2C0_SCL/ BD38	O, 1.8V CMOS/ 2.2K PU	I2C CLK for Display and Touch
S140	LCD_I2C_SDA	LVDS0_I2C0_SDA/ BD36	IO, 1.8V CMOS/ 2.2K PU	I2C DATA for Display and Touch
S141	LCD0_BL_PWM (GPIO1_04)	LVDS0_GPIO00/ BE39	O, 1.8V CMOS	LCD0 Back Light Brightness control PWM

Note: Contact iWave support team if LVDS supported SOM is required or refer Application note: "AN2702-i.MX8 QM SMARC SOM-Enabling LVDS Support in SMARC Edge-Application Note-R4.0-REL1.0.pdf"

2.7.10Audio Interface

The i.MX8 SMARC SOM supports I2S0 and I2S1 channels of SMARC Edge connector from CPU's SAI0 and SAI1 channels respectively. The SAI peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, AC97 and other audio CODEC/DSP interfaces. The SAI general features are including Transmitter section with independent bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits and Supports graceful restart after FIFO error. Only Transmitter Clock and Transmitter Left-Right Clock (LRCK) is supported as per SMARC specification.

In i.MX8 SMARC SOM the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For more details on SMARC Edge SD pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S38	MCLK_OUT0	MCLK_OUT0/ BD4	O, 1.8V CMOS	Master Clock for Audio codec
S39	SAI1_TXFS	SAI1_TXFS/ AV2	O, 1.8V CMOS	Serial Audio Interface Channel1 Frame Sync /Left Right Clock
S40	SAI1_TXD	SAI1_TXD/ AU1	O, 1.8V CMOS	Serial Audio Interface Channel1 Data Output
S41	SAI1_RXD	SAI1_RXD/ AV4	I, 1.8V CMOS	Serial Audio Interface Channel1 Data Input
S42	SAI1_TXC	SAI1_TXC/ AU5	O, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel1 Clock
S50	AUD_SAI0_TXFS	SPI2_CS1/ AY2	O, 1.8V CMOS	Serial Audio Interface Channel0 Left Right Clock
S51	AUD_SAI0_TXD	SPI0_SDO / AY6	O, 1.8V CMOS	Serial Audio Interface Channel0 Data Output
S52	AUD_SAI0_RXD	SPI0_SDI /BA5	I, 1.8V CMOS	Serial Audio Interface Channel0 Data Input
S53	AUD_SAI0_TXC	SPI0_CS1 / BA3	O, 1.8V CMOS/ 33E Series	Serial Audio Interface Channel0 Clock

2.7.11 SPI Interface

The i.MX8 CPU supports low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave with maximum clock speed of 40MHz. The i.MX8 SMARC SOM supports SPI0 channels of the SMARC Edge connector with SPI3 of CPU side.

For more details on SPI pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P43	SPI3_CS0	SPI3_CS0/BG5	O, 1.8V CMOS	SPI0 Chip Select 0
P44	SPI3_SCLK	SPI3_SCLK/BF6	O, 1.8V CMOS/ 33E Series	SPI0 Clock
P45	SPI3_MISO	SPI3_MISO/BE5	I, 1.8V CMOS	SPI0 Master IN Slave Out

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P46	SPI3_MOSI	SPI3_MOSI/ BF2	O, 1.8V CMOS	SPI0 Master Out Slave In

The i.MX8 SMARC SOM supports 2nd SPI channels of the SMARC Edge connector with SPI2 or QSPI1A of CPU interface. But in default configuration SPI2 is connected over ESPI pins. QSPI1A maximum clock speed very from 60MHz to 200MHZ in different mode which can be supported over SPI pins by contacting iWave support team.

For more details on 2nd SPI pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P54	SPI2_CS0	SPI2_CS0/ AW1 or QSPI1A_SS0/ J11	O, 1.8V CMOS	SPI2 Chip Select 0. *Note: Optionally connected to QSPI1A_ Chip Select 0*
P55	QSPI1A_SS1	QSPI1A_SS1/ G11	O, 1.8V CMOS	QSPI1A_ Chip Select 1 *Note: Can be used as GPIO4_20*
P56	SPI2_SCLK	SPI2_SCK/ AW5 or QSPI1A_SCLK/ F10	O, 1.8V CMOS/ 33E Series	SPI2 Clock *Note: Optionally connected to QSPI1A_ Clock*
P57	SPI2_MISO	SPI2_SDI/ AY4 or QSPI1A_DATA0/ D12 or QSPI1A_DATA1/ D14	IO, 1.8V CMOS	SPI2 Master In Slave Out. *Note: Optionally connected to QSPI1A_DATA0 and QSPI1A_DATA1*
P58	SPI2_MOSI	SPI2_SDO/ BA1 or QSPI1A_DATA1/ D14 or QSPI1A_DATA0/ D12	IO, 1.8V CMOS	SPI2 Master Out Slave In *Note: Optionally connected to QSPI1A_DATA0 and QSPI1A_DATA1*
S56	QSPI1A_DATA2	QSPI1A_DATA2/ E13	IO, 1.8V CMOS	*QSPI1A DATA lane 2*
S57	QSPI1A_DATA3	QSPI1A_DATA3/ E11	IO, 1.8V CMOS	*QSPI1A DATA lane 3*
S58	QSPI1A_RESET(GPIO4_22)	QSPI1A_DQS/ H12	O, 1.8V CMOS	*QSPI1A RESET*

2.7.12 Data UART

SMARC V2.1.1 supports four UART channels where two channels SER0 & SER2 are with CTS and RTS and two channels SER1 & SER3 are without. The i.MX8 CPU's UART0 and UART3 connected SER0 and SER1 channels of SMARC Edge connector respectively. Whereas SER2 channel of SMARC Edge connector optionally connected to UART1 and M40.UART0 of i.MX8 CPU. In default configuration UART1 is connected to on SOM Bluetooth module. SER0, SER1 & SER2 can be used for any data commination. UART4 of the CPU is connected to SER3 channel of SMARC Edge connector and used as Debug UART.

For more details on UART pinouts, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P129	UART0_TX	UART0_TX/ AV50	O, 1.8V CMOS	UART0 Transmitter.
P130	UART0_RX	UART0_RX/ AV48	I, 1.8V CMOS	UART0 Receiver.
P131	UART0_RTS_B	UART0_RTS_B/ AU45	O, 1.8V CMOS	UART0 Request to Send.
P132	UART0_CTS_B	UART0_CTS_B/ AW49	I, 1.8V CMOS	UART0 Clear to Send.
P134	UART3_TX	UART3_TX/ AU47	O, 1.8V CMOS	UART3 Transmitter.
P135	UART3_RX	UART3_RX/ AP44	I, 1.8V CMOS	UART3 Receiver.
P136	NC.	M40_I2C0_SDA/ AU51 or UART1_TX/ AY48	O, 1.8V CMOS 100K PU/PD*	NC. *Note: AU51 can be used as M4 Core-0 UART0.TX but also used for board configuration, hence termination can change between PU and PD based on board configuration number.* *Note: Optionally connect to UART1_TX.*
P137	NC	M40_I2C0_SCL/ AM44 or UART1_RX/ AT44	I, 1.8V CMOS 100K PU/PD*	NC. *Note: AM44 can be used as M4 Core-0 UART0.RX but is also used for board configuration, hence termination can change between PU and PD based on board configuration number* *Note: Optionally connect to* UART1_RX.
P138	NC	UART1_RTS_B/ AR43	O, 1.8V CMOS	NC. *Note: Optionally connect to* UART1_RTS_B
P139	NC	UART1_CTS_B/ AV46	I, 1.8V CMOS	NC. *Note: Optionally connect to* UART1_CTS_B.
P140	UART4_TX	UART4_TX/ AU53	O, 1.8V CMOS	Debug UART Transmitter.
P141	UART4_RX	UART4_RX/ AR47	I, 1.8V CMOS	Debug UART Receiver.

2.7.13 SMARC GPIOs

SMARC V2.1.1 supports 14 GPIOs, which can be used for any general-purpose application and are listed below. But, if extra GPIO are required then refer **"i.MX8 Pin Multiplexing on SMARC Edge"** table, which gives all optional GPIO supported via Edge connector.

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P108	GPIO_0(GPIO1_27)	MIPI_CSI0_GPIO0 _00/BL23	IO, 1.8V CMOS	SMARC General Purpose Input/output 0.
P109	GPIO_1(GPIO1_30)	MIPI_CSI1_GPIO0 _00/BN15	IO, 1.8V CMOS	SMARC General Purpose Input/output 1.
P110	GPIO_2(GPIO1_28)	MIPI_CSI0_GPIO0 _01/BM22	IO, 1.8V CMOS	SMARC General Purpose Input/output 2.
P111	GPIO_3(GPIO1_31)	MIPI_CSI1_GPIO0 _01/BN13	IO, 1.8V CMOS	SMARC General Purpose Input/output 3.
P112	GPIO_4(GPIO4_11)	USDHC2_WP/ D8	IO, 1.8V CMOS	SMARC General Purpose Input/output 4.
P113	GPIO_5(GPIO0_19)	GPT1_COMPARE/ BA51	IO, 1.8V CMOS	SMARC General Purpose Input/output 5.
P114	GPIO_6(GPIO0_00)	SIM0_CLK/ AL45	IO, 1.8V CMOS	SMARC General Purpose Input/output 6.
P115	GPIO_7(GPIO0_01)	SIM0_RST/ AP48	IO, 1.8V CMOS	SMARC General Purpose Input/output 7.
P116	GPIO_8(GPIO0_02)	SIM0_IO/ AN45	IO, 1.8V CMOS	SMARC General Purpose Input/output 8.
P117	GPIO_9(GPIO0_03)	SIM0_PD/ AL43	IO, 1.8V CMOS	SMARC General Purpose Input/output 9.
P118	GPIO_10(GPIO0_04)	SIM0_POWER_EN/ AT48	IO, 1.8V CMOS	SMARC General Purpose Input/output 10.
P119	GPIO_11(GPIO0_05)	SIM0_GPIO0_00/ AP46	IO, 1.8V CMOS	SMARC General Purpose Input/output 11.
S123	GPIO_13(GPIO1_29)	MIPI_CSI1_MCLK_OUT/ BN23	IO, 1.8V CMOS	NC. *Optionally SMARC General Purpose Input/output 13.*
S142	GPIO_12(GPIO2_24)	ESAI0_SCKR/BB8	IO, 1.8V CMOS	NC. *Optionally SMARC General Purpose Input/output 12.*

2.7.14 CAN Interface

The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification.

The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported by the FlexCAN module.

The i.MX8 CPU Supports three CAN interface and CAN0 and CAN1 are connected to SMARC Edge connector and CAN3 is connected to Board Expansion connector.

For more details of CAN pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P143	FLEXCAN0_TX	FLEXCAN0_TX/ H6	O, 1.8V CMOS	CAN 0 Transmitter.
P144	FLEXCAN0_RX	FLEXCAN0_RX/ C5	I, 1.8V CMOS	CAN 0 Receiver.
P145	FLEXCAN1_TX	FLEXCAN1_TX/ G7	O, 1.8V CMOS	CAN 1 Transmitter.
P146	FLEXCAN1_RX	FLEXCAN1_RX/ E5	I, 1.8V CMOS	CAN 1 Receiver.

2.7.15 I2C Interface

SMARC Specification V2.1.1 supports Five I2C but i.MX 8QM SOM supports only four I2C in default configuration and fifth I2C as optional which are listed down:

- One General Purpose I2C
- Two Camera I2C (can be used for General Purpose)
- One LCD Display ID I2C (can be used for General Purpose)
- One Power Management I2C (optional)

For more details of I2C pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S48	I2C_GP_CK	DMA_I2C1_SCL/ AY52	O, 1.8V CMOS 2.2K PU	General Purpose I2C Clock.
S49	I2C_GP_DAT	DMA_I2C1_SDA/ AV52	IO, 1.8V CMOS 2.2K PU	General Purpose I2C Data.
S1	I2C_CAM1_CK	MIPI_CSI1_I2C0_SCL/ BN17	O, 1.8V CMOS 2.2K PU	Secondary Camera Purpose I2C Clock.
S2	I2C_CAM1_DAT	MIPI_CSI1_I2C0_SDA/ BE15	IO, 1.8V CMOS 2.2K PU	Secondary Camera Purpose I2C Data.
S5	I2C_CAM0_CK	MIPI_CSI0_I2C0_SCL/ BH24	O, 1.8V CMOS 2.2K PU	Primary Camera Purpose I2C Clock.
S7	I2C_CAM0_DAT	MIPI_CSI0_I2C0_SDA/ BN19	IO, 1.8V CMOS 2.2K PU	Primary Camera Purpose I2C Clock.
S139	I2C_LCD_CK	LVDS_I2C_SCL/ BD38	O, 1.8V CMOS 2.2K PU	Display Purpose I2C Clock.
S140	I2C_LCD_DAT	LVDS_I2C_SDA/ BD36	IO, 1.8V CMOS 2.2K PU	Display Purpose I2C Clock.
P121	NC *(I2C_PM_CK)*	PMIC_I2C_SCL/ AY46	O, 1.8V CMOS 2.2K PU	NC.*Note: Optionally connected to PMIC_I2C_SCL*

P122	NC *(I2C_PM_DAT)*	PMIC_I2C_SDA/ BG51	IO, 1.8V CMOS 2.2K PU	NC. *Note: Optionally connected to PMIC_I2C_ SDA*

2.7.16 Control Signals

SMARC V2.1.1 specification supports control Signals, for more details on SMARC Control Signals pinouts on SMARC Edge connector, refer below table:

SMARC Pin No.	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P123	BOOT_SEL0#	NA	I, 1.8V CMOS 10K PU	**Boot Media Select [2:0]#** **000**-FlexSPI (Optional) **001**-eMMC (Default) **011**-microSD **110**-Standard SD **0**-Floating & **1**-GND
P124	BOOT_SEL1#	NA	I, 1.8V CMOS 10K PU	
P125	BOOT_SEL2#	NA	I, 1.8V CMOS 10K PU	
P126	RESET_OUT(GPIO0_10)	M41_I2C0_SCL/ AR45	I, 1.8V CMOS	RESET OUT from CPU to all other peripherals.
P127	RESET_IN#	POR_B/ BE49	I, 1.8V CMOS 100K PU	Hard RESET Input to SOM.
P128	ON_OFF_BUTTON	ON_OFF_ BUTTON/ BE47	I, 1.8V CMOS	Power ON /OFF Input to SOM.
S150	VIN_PWR_BAD#	NA	I, 5V CMOS 10K PU	Power bad indication from Carrier board. Module and Carrier power supplies shall not be enabled while this signal is held low by the Carrier.
S153	CARRIER_STBY#	NA	O, 1.8V CMOS 10K PU	Carrier power should be enabled only after CARRIER_STBY# goes High.
S154	CARRIER_PWR_ON	NA	O, 1.8V CMOS 10K PU	Carrier power should be enabled only after CARRIER_PWR_ON goes High.
S155	FORCE_RECOV#	NA	I, 1.8V CMOS 10K PU	Low on this pin allows non-protected segments of Module boot device to be rewritten / restored from an external USB Host on Module USB0. The Module USB0 operates in Client Mode when in the Force Recovery function is invoked.
S157	TEST_MODE_SELECT	TEST_MODE_ SELECT/BC49	I, 1.8V CMOS 10K PU	Only for Module vendor specific use.

2.7.17Power and GND

The i.MX8M SMARC SOM works with 5V power input (VCC) from SMARC PCB Edge Connector and generates all other required powers internally On-SOM itself. i.MX8M SMARC SOM also supports coin cell power input (VDD_RTC) from SMARC PCB Edge Connector to On-SOM RTC controller for real time clock.

For more details on Power & GND Signals pinouts on SMARC PCB Edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P147,P148,P149,P150, P151,P152,P153,P154, P155,P156	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage.
P2,P9,P12,P15,P18,P32, P38,P47,P50,P53,P59, P68,P79,P82,P85,P88, P91,P94,P97,P100, P103,P120,P133,P142, S3,S10,S13,S16,S25,S34, S47,S61,S64,S67,S70, S73,S80,S83,S86,S89, S92,S101,S110,S119, S124,S130,S136,S143, S158	GND	GND	NA	Power	Ground.
S147	VDD_RTC	VDD_RTC	NA	I, 3V Power	3V coin cell input for RTC.

2.8 Expansion Connector (Optional)

The i.MX8 SMARC SOM supports an 100pin Expansion connector (J8) as a optional feature to utilise extra interfaces which is not covered under SMARC specification V2.1.1. edge connector. The SOM Expansion connector is placed on the bottom side of the SOM.

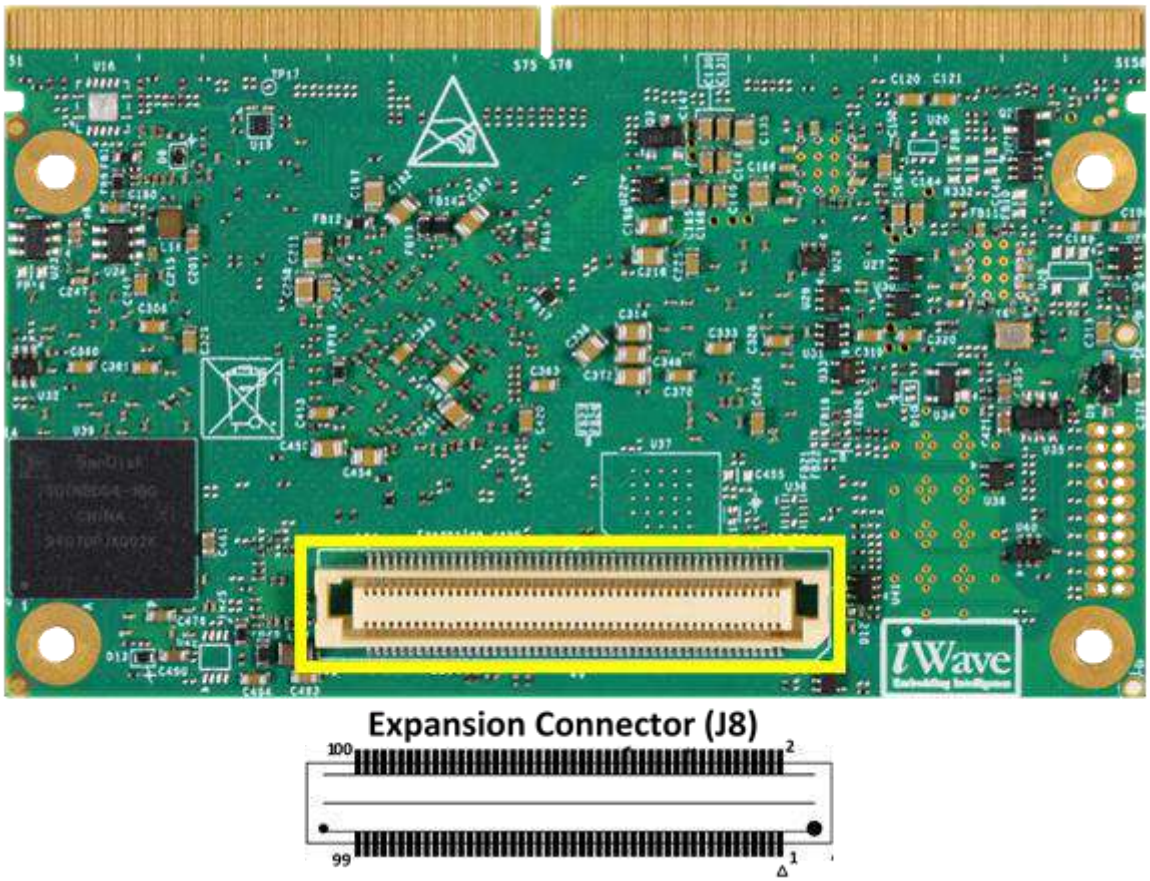

Figure 5: SMARC Expansion Connector

Number of Pins - : 100

Connector Part - : FX8C-100S-SV(68) from Hirose

Mating Connector - : FX8C-100P-SV(91) from Hirose

Note: In default configuration Expansion connector is optional, contact iWave Support Team for further information.

Table 4: Expansion Connector Pinouts

Signal	Expansion Connector Pin	Expansion Connector Pin	Signal
HDMI_RX0_CLK_N	1	2	USB3_HUB3_TXP
HDMI_RX0_CLK_P	3	4	USB3_HUB3_TXM
GND	5	6	GND
HDMI_RX0_ARC_N	7	8	USB3_HUB3_RXP
HDMI_RX0_ARC_P	9	10	USB3_HUB3_RXM
GND	11	12	GND
HDMI_RX0_DATA0_N	13	14	USB3_HUB4_TXP
HDMI_RX0_DATA0_P	15	16	USB3_HUB4_TXM
GND	17	18	GND
HDMI_RX0_DATA1_N	19	20	USB3_HUB4_RXP
HDMI_RX0_DATA1_P	21	22	USB3_HUB4_RXM
GND	23	24	GND
HDMI_RX0_DATA2_N	25	26	LVDS0_CH0_CLK_P
HDMI_RX0_DATA2_P	27	28	LVDS0_CH0_CLK_N
GND	29	30	GND
LVDS0_CH1_TX3_N	31	32	LVDS0_CH0_TX2_P
LVDS0_CH1_TX3_P	33	34	LVDS0_CH0_TX2_N
GND	35	36	GND
LVDS0_CH1_TX2_N	37	38	LVDS0_CH0_TX3_P
LVDS0_CH1_TX2_P	39	40	LVDS0_CH0_TX3_N
GND	41	42	GND
LVDS0_CH1_TX1_N	43	44	LVDS0_CH0_TX0_P
LVDS0_CH1_TX1_P	45	46	LVDS0_CH0_TX0_N
GND	47	48	GND
LVDS0_CH1_TX0_P	49	50	LVDS0_CH0_TX1_P
LVDS0_CH1_TX0_N	51	52	LVDS0_CH0_TX1_N
GND	53	54	GND
LVDS0_CH1_CLK_N	55	56	VHDMI_RX_5V
LVDS0_CH1_CLK_P	57	58	SNVS_TAMPER_IN0
GND	59	60	GND
SNVS_TAMPER_IN1	61	62	MLB_DATA_P
SNVS_TAMPER_OUT1	63	64	MLB_DATA_N
ESAI1_FST	65	66	GND
HDMI_RX0_CEC	67	68	MLB_CLK_P
HDMI_RX_HPD	69	70	MLB_CLK_N
HDMI_RX0_DDC_SDA	71	72	GND
SNVS_TAMPER_OUT0	73	74	MLB_SIG_P
ESAI1_SCKR	75	76	MLB_SIG_N
ESAI1_FSR	77	78	GND
HDMI_RX0_DDC_SCL	79	80	MIPI_CSI0_DATA2_P

Signal	Expansion Connector Pin	Expansion Connector Pin	Signal
ESAI1_TX0	**81**	**82**	MIPI_CSI0_DATA2_N
SPDIF_ETX_CLK/DMA_I2C2_SCL*	**83**	**84**	GND
SPDIF_TX/DMA_I2C2_SDA*	**85**	**86**	MIPI_CSI0_DATA3_P
ESAI1_TX1	**87**	**88**	MIPI_CSI0_DATA3_N
ESAI1_TX4_RX1	**89**	**90**	GND
FLEXCAN2_RX	**91**	**92**	ESAI1_SCKT
MLB_DATA	**93**	**94**	SPDIF_RX
MLB_CLK	**95**	**96**	ESAI1_TX3_RX2
MLB_SIG	**97**	**98**	ESAI1_TX2_RX3
FLEXCAN2_TX	**99**	**100**	ESAI1_TX5_RX0

2.8.1 LVDS Interface (Optional)

The i.MX8 Processor's two four lane LVDS channels from LVDS0 interface are connected to Board Expansion connector. Processor has LVDS Display Bridge (LDB) connects to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface.

For more details on Expansion Connector LVDS pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
LVDS0 Channel0				
26	LVDS0_CH0_CLK_P	LVDS0_CH0_CLK_P/ BN41	O, LVDS	LVDS0 Channel0 Clock positive.
28	LVDS0_CH0_CLK_N	LVDS0_CH0_CLK_N/ BL41	O, LVDS	LVDS0 Channel0 Clock negative.
32	LVDS0_CH0_TX2_P	LVDS0_CH0_TX2_P/ BM44	O, LVDS	LVDS0 Channel0 Transmit Lane 2 positive.
34	LVDS0_CH0_TX2_N	LVDS0_CH0_TX2_N/ BK44	O, LVDS	LVDS0 Channel0 Transmit Lane 2 negative.
38	LVDS0_CH0_TX3_P	LVDS0_CH0_TX3_P/ BN45	O, LVDS	LVDS0 Channel0 Transmit Lane 3 positive.
40	LVDS0_CH0_TX3_N	LVDS0_CH0_TX3_N/ BL45	O, LVDS	LVDS0 Channel0 Transmit Lane 3 negative.
44	LVDS0_CH0_TX0_P	LVDS0_CH0_TX0_P/ BM42	O, LVDS	LVDS0 Channel0 Transmit Lane 0 positive.
46	LVDS0_CH0_TX0_N	LVDS0_CH0_TX0_N/ BK42	O, LVDS	LVDS0 Channel0 Transmit Lane 0 negative.
50	LVDS0_CH0_TX1_P	LVDS0_CH0_TX1_P/ BN43	O, LVDS	LVDS0 Channel0 Transmit Lane 1 positive.
52	LVDS0_CH0_TX1_N	LVDS0_CH0_TX1_N/ BL43	O, LVDS	LVDS0 Channel0 Transmit Lane 1 negative.
LVDS0 Channel1				
55	LVDS0_CH1_CLK_N	LVDS0_CH1_CLK_N/ BG45	O, LVDS	LVDS0 Channel1 Clock negative.
57	LVDS0_CH1_CLK_P	LVDS0_CH1_CLK_P/ BH46	O, LVDS	LVDS0 Channel1 Clock positive.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
51	LVDS0_CH1_TX0_N	LVDS0_CH1_TX0_N/ BG43	O, LVDS	LVDS0 Channel1 Transmit Lane 0 negative.
49	LVDS0_CH1_TX0_P	LVDS0_CH1_TX0_P/ BH44	O, LVDS	LVDS0 Channel1 Transmit Lane 0 positive.
43	LVDS0_CH1_TX1_N	LVDS0_CH1_TX1_N/ BG41	O, LVDS	LVDS0 Channel1 Transmit Lane 1 negative.
45	LVDS0_CH1_TX1_P	LVDS1_CH1_TX1_P/ BH42	O, LVDS	LVDS0 Channel1 Transmit Lane 1 positive.
37	LVDS0_CH1_TX2_N	LVDS0_CH1_TX2_N/ BG39	O, LVDS	LVDS0 Channel1 Transmit Lane 2 negative.
39	LVDS0_CH1_TX2_P	LVDS0_CH1_TX2_P/ BH40	O, LVDS	LVDS0 Channel1 Transmit Lane 2 positive.
31	LVDS0_CH1_TX3_N	LVDS0_CH1_TX3_N/ BG37	O, LVDS	LVDS0 Channel1 Transmit Lane 3 negative.
33	LVDS0_CH1_TX3_P	LVDS0_CH1_TX3_P/ BH38	O, LVDS	LVDS0 Channel1 Transmit Lane 3 positive.

2.8.2 CAN Interface (Optional)

The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. CAN0 and CAN1 of CPU are connected to SMARC edge connector and CAN2 is connected to expansion connector.

For more details on Expansion Connector CAN pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
91	FLEXCAN2_RX	FLEXCAN2_RX/ C3	I, 1.8V CMOS	CAN Receiver.
99	FLEXCAN2_TX	FLEXCAN2_TX/ E7	O, 1.8V CMOS	CAN Transmitter.

2.8.3 USB3.0 Interface (Optional)

On SOM USB3.0 hub USB5744-I/2G from Microchip Hub Feature Controller IC with 4 USB 3.1 Gen 1 / USB 2.0 downstream ports. The upstream ports are connected to SMARC Edge connector and Expansion connector.

For more details on USB expansion signals on expansion connector, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
2	USB3_HUB3_TXP	NA	O, USB SS	USB3.0 Hub Transmit channel 3 Plus.
4	USB3_HUB3_TXM	NA	O, USB SS	USB3.0 Hub Transmit channel 3 Minus.
8	USB3_HUB3_RXP	NA	I, USB SS	USB3.0 Hub Receive channel 3 Plus.
10	USB3_HUB3_RXM	NA	I, USB SS	USB3.0 Hub Receive channel 3 Minus.
14	USB3_HUB4_TXP	NA	O, USB SS	USB3.0 Hub Transmit channel 4 Plus.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
16	USB3_HUB4_TXM	NA	O, USB SS	USB3.0 Hub Transmit channel 4 Minus.
20	USB3_HUB4_RXP	NA	I, USB SS	USB3.0 Hub Receive channel 4 Plus.
22	USB3_HUB4_RXM	NA	I, USB SS	USB3.0 Hub Receive channel 4 Minus.

2.8.4 ESAI Interface (Optional)

The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, the ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. ESAI has three basic operating modes and many data/operation formats. ESAI operating mode are selected by the ESAI control registers.

ESAI1 of i.MX8 Processor is connected to board expansion connector, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
65	ESAI1_FST	ESAI1_FST/ BF12	O, 1.8V CMOS	ESAI1 Frame Sync Output.
75	ESAI1_SCKR	ESAI1_SCKR/ BD12	I, 1.8V CMOS	ESAI1 Clock Input.
77	ESAI1_FSR	ESAI1_FSR/ BE11	I, 1.8V CMOS	ESAI1 Frame Sync Input.
81	ESAI1_TX0	ESAI1_TX0/ BF10	O, 1.8V CMOS	ESAI1 Transmit 0.
87	ESAI1_TX1	ESAI1_TX1/ BA11	IO, 1.8V CMOS	ESAI1 Transmit 1.
89	ESAI1_TX4_RX1	ESAI1_TX4_RX1/ AY12	IO, 1.8V CMOS	ESAI1 Transmit 4 or Receive 1.
92	ESAI1_SCKT	ESAI1_SCKT/ AY10	O, 1.8V CMOS	ESAI1 Clock Out.
96	ESAI1_TX3_RX2	ESAI1_TX3_RX2/ AV10	IO, 1.8V CMOS	ESAI1 Transmit 3 or Receive 2.
98	ESAI1_TX2_RX3	ESAI1_TX2_RX3/ AU11	IO, 1.8V CMOS	ESAI1 Transmit 2 or Receive 3.
100	ESAI1_TX5_RX0	ESAI1_TX5_RX0/ AT10	IO, 1.8V CMOS	ESAI1 Transmit 5 or Receive 0.

2.8.5 SPDIF Interface (Optional)

The Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF is composed of two parts: SPDIF Receiver and SPDIF Transmitter.

The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs. The Channel Status and User Bits are also extracted from each frame and placed in the corresponding registers. The SPDIF receiver also provides a bypass option for direct transfer of the SPDIF input signal to the SPDIF transmitter.

For the SPDIF transmitter, the audio data is provided by the processor via the SPDIFTxLeft and SPDIFTxRight registers. The Channel Status bits are also provided via the corresponding registers. The SPDIF transmitter generates a SPDIF output bitstream in the bi-phase mark format (IEC60958), which consists of audio data, channel status and user bits.

For more details on SPDIF Expansion Connector pinout, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
83	SPDIF_ETX_CLK	SPDIF_ETX_CLK/ BD6	O, 1.8V CMOS	Sony/Philips Digital Interface Clock. *Note: Optionally connected to DMA_I2C2_SCL*
85	SPDIF_TX	SPDIF_TX/BC9	O, 1.8V CMOS	Sony/Philips Digital Interface Transmit. *Note: Optionally connected to DMA_I2C2_SDA*
94	SPDIF_RX	SPDIF_RX/BC7	I, 1.8V CMOS	Sony/Philips Digital Interface Receive.

2.8.6 MLB Interface (Optional)

Media Local Bus Device functionality is implemented with an MediaLB 3-pin interface (single ended) or MediaLB 6-pin interface (differential), however only one interface can be active at a time. The MediaLB interfaces are capable of exchanging data at speeds up to 1024xFs in 3-pin mode or 6144xFs in 6-pin mode. Both MediaLB interfaces provide real-time access to all network data types including streaming, packet, control, and isochronous data.

For more details of MLB on Expansion Connector, refer below table.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
62	MLB_DATA_P	MLB_DATA_P/ F34	IO, MLB	Media Local Bus DATA positive.
64	MLB_DATA_N	MLB_DATA_N/ E35	IO, MLB	Media Local Bus DATA negative.
68	MLB_CLK_P	MLB_CLK_P/ D32	O, MLB	Media Local Bus Clock positive.
70	MLB_CLK_N	MLB_CLK_N/ E33	O, MLB	Media Local Bus Clock negative.
74	MLB_SIG_P	MLB_SIG_P/ D30	O, MLB	Media Local Bus Signal positive.
76	MLB_SIG_N	MLB_SIG_N/ E31	O, MLB	Media Local Bus Signal negative.
93	MLB_DATA	MLB_DATA/ E3	IO, 1.8V CMOS	Media Local Bus Data.
95	MLB_CLK	MLB_CLK/ D2	O, 1.8V CMOS	Media Local Bus Clock.
97	MLB_SIG	MLB_SIG/E1	O, 1.8V CMOS	Media Local Bus Signal.

2.8.7 MIPI CSI0 (Optional)

The I.MX8 processor supports two four lane MIPI CSI camera interface whereas SMARAC edge connector support one two lane and one four lane MIPI CSI, hence data2 and data3 lane of CSI0 channel are connected to board expansion connector.

For more details on MIPI CSI expansion signals, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
80	MIPI_CSI0_DATA2_P	MIPI_CSI0_DATA2_P/BF24	I, MIPI	MIPI CSI0 differential data lane 2 positive.
82	MIPI_CSI0_DATA2_N	MIPI_CSI0_DLN2_M/BE25	I, MIPI	MIPI CSI0 differential data lane 2 negative
86	MIPI_CSI0_DATA3_P	MIPI_CSI0_DLN3_P/BF16	I, MIPI	MIPI CS0 differential data lane 3 positive.
88	MIPI_CSI0_DATA3_N	MIPI_CSI0_DLN3_M/BE17	I, MIPI	MIPI CSI0 differential data lane 3 negative.

2.8.8 HDMI Receiver (Optional)

The i.MX8 Processor supports HDMI-RX HDMI 2.0a with HDCP 2.2 and 1.4. In SOM, since SMARC Edge connector support only HDMI TX interface HDMI RX interface is supported via board expansion connector. The HDMI_RX Controller Supports up to 4K2K at 60Hz resolution and Compliant with HDCP2.2 (and backward compatible with HDCP1.4) with up to 600Mhz pixel clock and supports up to 8 (Status and Control Data Channel) SCDC slave addresses.

Note: Currently HDMI Receiver is not supported by NXP.

For more details on Expansion Connector HDMI RX pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	HDMI_RX0_CLK_N	HDMI_RX0_CLK_N/BL11	I, HDMI	HDMI RX0 differential Clock negative.
3	HDMI_RX0_CLK_P	HDMI_RX0_CLK_P/BM12	I, HDMI	HDMI RX0 differential Clock positive.
7	HDMI_RX0_ARC_N	HDMI_RX0_ARC_N/BL13	I, HDMI	HDMI RX0 differential Audio Return Channel negative.
9	HDMI_RX0_ARC_P	HDMI_RX0_ARC_P/BM14	I, HDMI	HDMI RX0 differential Audio Return Channel positive.
13	HDMI_RX0_DATA0_N	HDMI_RX0_DATA0_N/BL15	I, HDMI	HDMI RX0 differential data lane 0 negative.
15	HDMI_RX0_DATA0_P	HDMI_RX0_DATA0_P/BM16	I, HDMI	HDMI RX0 differential data lane 0 positive.
19	HDMI_RX0_DATA1_N	HDMI_RX0_DATA1_N/BL17	I, HDMI	HDMI RX0 differential data lane 1 negative.
21	HDMI_RX0_DATA1_P	HDMI_RX0_DATA1_P/BM18	I, HDMI	HDMI RX0 differential data lane 1 positive.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
25	HDMI_RX0_DATA2_N	HDMI_RX0_DATA2_N/BL19	I, HDMI	HDMI RX0 differential data lane 2 negative.
27	HDMI_RX0_DATA2_P	HDMI_RX0_DATA2_P/BM20	I, HDMI	HDMI RX0 differential data lane 2 positive.
56	VHDMI_RX_5V	HDMI_RX0_MON_5V/BN11	Power	VHDMI_RX_5V.
67	HDMI_RX0_CEC	HDMI_RX0_CEC/BJ9	IO, 3.3V CMOS	HDMI Consumer Electronics Control.
69	HDMI_RX_HPD	HDMI_RX_HPD/BF14	O, 5V CMOS	HDMI RX0 Hot Plug Detect.
71	HDMI_RX0_DDC_SDA	HDMI_RX0_DDC_SDA/BE13	IO, 5V CMOS	HDMI RX0 I2C Data.
79	HDMI_RX0_DDC_SCL	HDMI_RX0_DDC_SCL/BH10	I, 5V CMOS	HDMI RX0 I2C Clock.

2.8.9 GPIO (Optional)

Refer GPIO Column under **"i.MX8 Pin Multiplexing on Expansion Connector"** for details on GPIO options available from Expansion connector.

2.9 Other Features

2.9.1 Fan Header

The i.MX8 SMARC SOM supports a Fan Header to connect cooling Fan if required. This Fan Header (J2) is physically located at the top of the board as shown below.

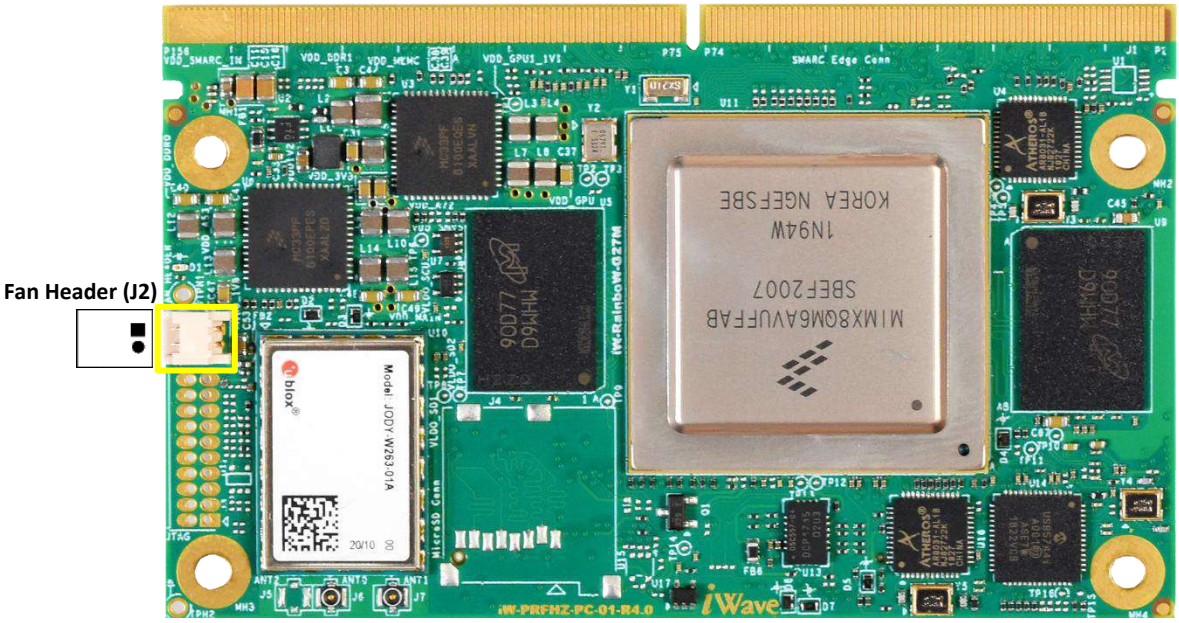

Figure 6: Fan Header

Number of Pins - 2

Connector Part - 0530480210 from Molex

Mating Connector - 51021-0200 from Molex

Compatible FAN (Example) - 109P0405J602 from Sanyo Denki America Inc.

Table 5: FAN Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN.
2	GND	Power	Ground.

2.9.2 Debug Header (Optional)

The i.MX8 SMARC SOM optionally supports one JTAG interface and/or UART interface for CPU debug purpose over a customized 20-pin connector (J3). Even though this JTAG connector pinout is fully compatible with “ARM JTAG 20” connector, the physical dimension of connector is made smaller because of space constraint. i.MX8 CPU’s JTAG pins are 1.8V tolerant and so 1.8V reference power is provided to pin 1 of the connectors to allow JTAG tool to automatically configure the logic signals for the right voltage.

The i.MX8 CPU’s SCU_UART0 and M4 Core1 UART or UART4 can be taken out from J3 header and using 1.8V voltage level FTDI’s UART to USB smart cable (*TTL-232RG-VREG1V8-WE)* UART can be directly connected to Host PC for debugging.

Debug Header (J3) is physically located on topside of the SOM. This is the optional feature and will not be populated in default configuration.

Number of Pins - 20

Connector Part - GRPB102MWCN-RC from Sullins Connector Solutions

Mating Connector - LPPB102CFFN-RC from Sullins Connector Solutions

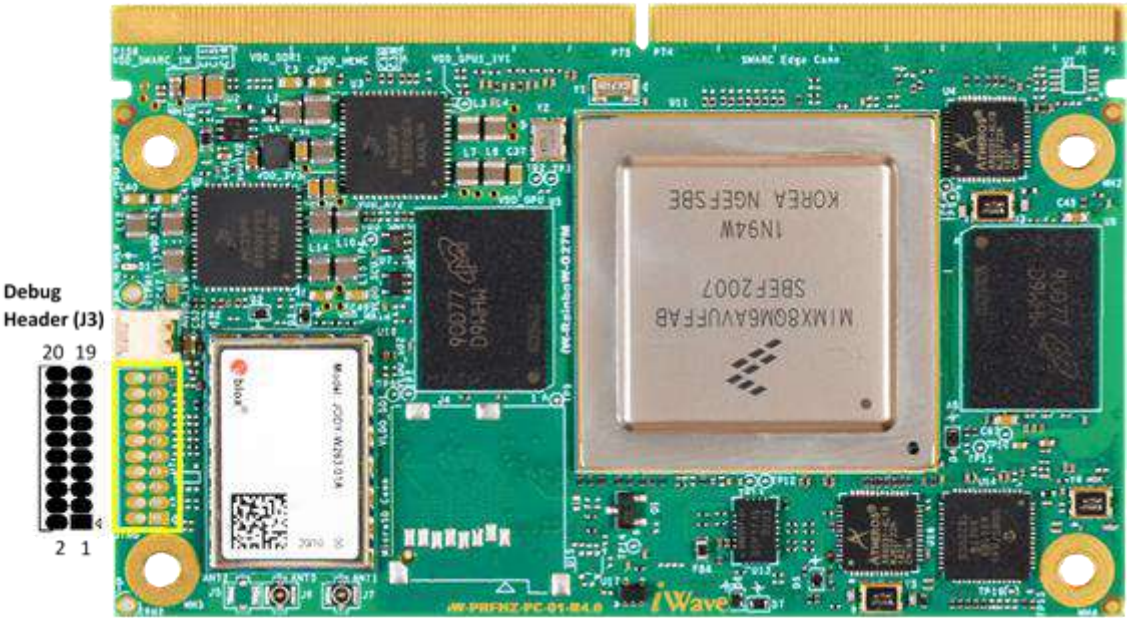

Figure 7: Debug Header

Table 6: Debug Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VREF	O, 1.8V Power	VTREF Voltage Reference.
2	VSUPPLY	O, 1.8V Power	Supply Voltage.
3	JTAG_TRSTB	I, 1.8V CMOS/ 10K PU	JTAG test reset signal.
4	GND	Power	Ground. *Note: Optionally connected to SCU_UART0_TX*
5	JTAG_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data input.
6	GND	Power	Ground. *Note: Optionally connected to SCU_UART0_RX*
7	JTAG_TMS	I, 1.8V CMOS/ 10K PU	JTAG test mode select.
8	GND	Power	Ground. *Note: Optionally connected to M41.UART0.TX and UART4_TX.*
9	JTAG_TCK	I, 1.8V CMOS/ 10K PD	JTAG test Clock.
10	GND	Power	Ground. *Note: Optionally connected to M41.UART0.RX and UART4_RX.*
11	-	-	Only pull down is provided.
12	GND	Power	Ground.
13	JTAG_TDO	O, 1.8V CMOS	JTAG test data output.
14	GND	Power	Ground.
15	JTAG_RESETB	I, 1.8V CMOS/ 10K PU	Reset input.
16	GND	Power	Ground.
17	-	-	Only pull up is provided.
18	GND	Power	Ground.
19	-	-	Only pull down is provided.
20	GND	Power	Ground.

2.10 i.MX8 Pin Multiplexing on SMARC Edge

The i.MX8 CPU IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX8 CPU's IO pins can be configured as GPIO if required. The below table provides the details of i.MX8 CPU pin connections to the SMARC edge connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX8 Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the SMARC SOM Edge connector for iWave's BSP reusability and to have compatible SMARC modules in future for upgradability.

Table 7: i.MX8 CPU IOMUX for SMARC Edge Connector interfaces

Interface/ Function	SMARC Edge Pin Number	i.MX8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
MIPI CSI0	S9	BE21	MIPI_CSI0.CKN					MIPI_CSI0.CKN
	S8	BF20	MIPI_CSI0.CKP					MIPI_CSI0.CKP
	S12	BE23	MIPI_CSI0.DN0					MIPI_CSI0.DN0
	S11	BF22	MIPI_CSI0.DP0					MIPI_CSI0.DP0
	S15	BE19	MIPI_CSI0.DN1					MIPI_CSI0.DN1
	S14	BF18	MIPI_CSI0.DP1					MIPI_CSI0.DP1
	S6	BJ23	MIPI_CSI0.ACM.MCLK_OUT			LSIO.GPIO1.IO24	GPIO1_24	MIPI_CSI0.ACM.MCLK_ OUT
	S5	BH24	MIPI_CSI0.I2C0.SCL			LSIO.GPIO1.IO25	GPIO1_25	MIPI_CSI0.I2C0.SCL
	S7	BN19	MIPI_CSI0.I2C0.SDA			LSIO.GPIO1.IO26	GPIO1_26	MIPI_CSI0.I2C0.SDA
MIPI CSI1	P4	BH16	MIPI_CSI1.CKN					MIPI_CSI1.CKN
	P3	BJ17	MIPI_CSI1.CKP					MIPI_CSI1.CKP
	P8	BH18	MIPI_CSI1.DN0					MIPI_CSI1.DN0
	P7	BJ19	MIPI_CSI1.DP0					MIPI_CSI1.DP0
	P11	BH14	MIPI_CSI1.DN1					MIPI_CSI1.DN1
	P10	BJ15	MIPI_CSI1.DP1					MIPI_CSI1.DP1
	P14	BH20	MIPI_CSI1.DN2					MIPI_CSI1.DN2
	P13	BJ21	MIPI_CSI1.DP2					MIPI_CSI1.DP2
	P17	BH12	MIPI_CSI1.DN3					MIPI_CSI1.DN3
	P16	BJ13	MIPI_CSI1.DP3					MIPI_CSI1.DP3
	S1	BN17	MIPI_CSI1.I2C0.SCL			LSIO.GPIO2.IO00	GPIO2_00	MIPI_CSI1.I2C0.SCL
	S2	BE15	MIPI_CSI1.I2C0.SDA			LSIO.GPIO2.IO01	GPIO2_01	MIPI_CSI1.I2C0.SDA

Interface/ Function	SMARC Edge Pin Number	i.MX8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
MIPI DSI0	S135	BN27	MIPI_DSI0.CKN					MIPI_DSI0.CKN
	S134	BL27	MIPI_DSI0.CKP					MIPI_DSI0.CKP
	S126	BM28	MIPI_DSI0.DN0					MIPI_DSI0.DN0
	S125	BK28	MIPI_DSI0.DP0					MIPI_DSI0.DP0
	S129	BM26	MIPI_DSI0.DN1					MIPI_DSI0.DN1
	S128	BK26	MIPI_DSI0.DP1					MIPI_DSI0.DP1
	S132	BN29	MIPI_DSI0.DN2					MIPI_DSI0.DN2
	S131	BL29	MIPI_DSI0.DP2					MIPI_DSI0.DP2
	S138	BN25	MIPI_DSI0.DN3					MIPI_DSI0.DN3
	S137	BL25	MIPI_DSI0.DP3					MIPI_DSI0.DP3
	S139	BA53	GPT1_CLK	DMA.I2C2.SCL	LSIO.KPP0.COL7	LSIO.GPIO0.IO17	GPIO0_10	DMA.I2C2.SCL
	S140	AY50	GPT1_CAPTURE	DMA.I2C2.SDA	LSIO.KPP0.ROW4	LSIO.GPIO0.IO18	GPIO0_11	DMA.I2C2.SDA
	S141	BE39	LVDS0.GPIO0.IO00	LVDS0.PWM0.OUT		LSIO.GPIO1.IO04	GPIO1_04	GPIO1_04
	S127	BE37	LVDS0.I2C1.SCL	DMA.UART2.TX		LSIO.GPIO1.IO08	GPIO1_08	GPIO1_08
	S133	BE35	LVDS0.I2C1.SDA	DMA.UART2.RX		LSIO.GPIO1.IO09	GPIO1_09	GPIO1_09
MIPI DSI1	S109	BH30	MIPI_DSI1.CKN					MIPI_DSI1.CKN
	S108	BG31	MIPI_DSI1.CKP					MIPI_DSI1.CKP
	S112	BH32	MIPI_DSI1.DN0					MIPI_DSI1.DN0
	S111	BG33	MIPI_DSI1.DP0					MIPI_DSI1.DP0
	S115	BH28	MIPI_DSI1.DN1					MIPI_DSI1.DN1
	S114	BG29	MIPI_DSI1.DP1					MIPI_DSI1.DP1
	S118	BH34	MIPI_DSI1.DN2					MIPI_DSI1.DN2
	S117	BG35	MIPI_DSI1.DP2					MIPI_DSI1.DP2
	S121	BH26	MIPI_DSI1.DN3					MIPI_DSI1.DN3
	S120	BG27	MIPI_DSI1.DP3					MIPI_DSI1.DP3
	S122	BD34	LVDS1.GPIO0.IO00	LVDS1.PWM0.OUT		LSIO.GPIO1.IO10	GPIO1_10	LVDS1.PWM0.OUT
	S116	BD32	LVDS1.I2C1.SCL	DMA.UART3.TX		LSIO.GPIO1.IO14	GPIO1_14	LSIO.GPIO1.IO14
	S107	BN35	LVDS1.I2C1.SDA	DMA.UART3.RX		LSIO.GPIO1.IO15	GPIO1_15	LSIO.GPIO1.IO15
HDMI	P102	BK2	HDMI_TX0.TX_M_LN_3					HDMI_TX0.TX_M_LN_3
	P101	BL3	HDMI_TX0.TX_P_LN_3					HDMI_TX0.TX_P_LN_3
	P99	BM4	HDMI_TX0.TX_M_LN_2					HDMI_TX0.TX_M_LN_2

Interface/ Function	SMARC Edge Pin Number	i.MX8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	P98	BL5	HDMI_TX0.TX_P_LN_2					HDMI_TX0.TX_P_LN_2
	P96	BM6	HDMI_TX0.TX_M_LN_1					HDMI_TX0.TX_M_LN_1
	P95	BL7	HDMI_TX0.TX_P_LN_1					HDMI_TX0.TX_P_LN_1
	P93	BM8	HDMI_TX0.TX_M_LN_0					HDMI_TX0.TX_M_LN_0
	P92	BL9	HDMI_TX0.TX_P_LN_0					HDMI_TX0.TX_P_LN_0
	P104	BH8	HDMI_TX0.HPD					HDMI_TX0.HPD
	P105	BG1	HDMI_TX0.DDC_SCL					HDMI_TX0.DDC_SCL
	P106	BN5	HDMI_TX0.DDC_SDA					HDMI_TX0.DDC_SDA
SD Interface	P36	J39	CONN.USDHC1.CLK					CONN.USDHC1.CLK
	P34	G41	CONN.USDHC1.CMD			LSIO.GPIO5.IO14	GPIO5_14	CONN.USDHC1.CMD
	P39	E37	CONN.USDHC1.DATA0	CONN.NAND.RE_N		LSIO.GPIO5.IO15	GPIO5_15	CONN.USDHC1.DATA0
	P40	F38	CONN.USDHC1.DATA1	CONN.NAND.RE_P		LSIO.GPIO5.IO16	GPIO5_16	CONN.USDHC1.DATA1
	P41	E39	CONN.USDHC1.DATA2	CONN.NAND.DQS_N		LSIO.GPIO5.IO17	GPIO5_17	CONN.USDHC1.DATA2
	P42	F40	CONN.USDHC1.DATA3	CONN.NAND.DQS_P		LSIO.GPIO5.IO18	GPIO5_18	CONN.USDHC1.DATA3
	P37	BD28	MIPI_DSI0.GPIO0.IO01			LSIO.GPIO1.IO19	GPIO1_19	LSIO.GPIO1.IO19
	P33	BM24	MIPI_DSI1.GPIO0.IO00	MIPI_DSI1.PWM0.OUT		LSIO.GPIO1.IO22	GPIO1_22	LSIO.GPIO1.IO22
	P35	BK24	MIPI_DSI1.GPIO0.IO01			LSIO.GPIO1.IO23	GPIO1_23	LSIO.GPIO1.IO23
QSPI	P54	AW1	DMA.SPI2.CS0			LSIO.GPIO3.IO10	GPIO3_10	DMA.SPI2.CS0
		J11	LSIO.QSPI1A.SS0_B			LSIO.GPIO4.IO19	GPIO4_19	
	P55	G11	LSIO.QSPI1A.SS1_B			LSIO.GPIO4.IO20	GPIO4_20	LSIO.GPIO4.IO20
	P56	AW5	DMA.SPI2.SCK			LSIO.GPIO3.IO07	GPIO3_07	DMA.SPI2.SCK
		F10	LSIO.QSPI1A.SCLK			LSIO.GPIO4.IO21	GPIO4_21	
	S58	H12	LSIO.QSPI1A.DQS			LSIO.GPIO4.IO22	GPIO4_22	LSIO.GPIO4.IO22
	S56	E11	LSIO.QSPI1A.DATA3			LSIO.GPIO4.IO23	GPIO4_23	LSIO.QSPI1A.DATA3
	S57	E13	LSIO.QSPI1A.DATA2			LSIO.GPIO4.IO24	GPIO4_24	LSIO.QSPI1A.DATA2
	P58	BA1	DMA.SPI2.SDO			LSIO.GPIO3.IO08	GPIO3_08	DMA.SPI2.SDO
		D14	LSIO.QSPI1A.DATA1			LSIO.GPIO4.IO25	GPIO4_25	
	P57	AY4	DMA.SPI2.SDI			LSIO.GPIO3.IO09	GPIO3_09	DMA.SPI2.SDI
		D12	LSIO.QSPI1A.DATA0			LSIO.GPIO4.IO26	GPIO4_26	
SPI	P44	BF6	DMA.SPI3.SCK			LSIO.GPIO2.IO17	GPIO2_17	DMA.SPI3.SCK
	P45	BE5	DMA.SPI3.SDI	DMA.FTM.CH1		LSIO.GPIO2.IO19	GPIO2_19	DMA.SPI3.SDI
	P46	BF2	DMA.SPI3.SDO	DMA.FTM.CH0		LSIO.GPIO2.IO18	GPIO2_18	DMA.SPI3.SDO

Interface/ Function	SMARC Edge Pin Number	i.MX8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	P43	BG5	DMA.SPI3.CS0	DMA.FTM.CH2		LSIO.GPIO2.IO20	GPIO2_20	DMA.SPI3.CS0
	P31	BD8	DMA.SPI3.CS1			LSIO.GPIO2.IO21	GPIO2_21	DMA.SPI3.CS1
USB OTG1	P62	A39	CONN.USB_OTG1.VBUS					CONN.USB_OTG1.VBUS
	P64	A37	CONN.USB_OTG1.ID					CONN.USB_OTG1.ID
	P60	B40	CONN.USB_OTG1.DP					CONN.USB_OTG1.DP
	P61	C39	CONN.USB_OTG1.DN					CONN.USB_OTG1.DN
PCIe	P89	B26	PCIE0_TX0_P					PCIE0_TX0_P
	P90	C27	PCIE0_TX0_N					PCIE0_TX0_N
	P86	A29	PCIE0_RX0_P					PCIE0_RX0_P
	P87	B30	PCIE0_RX0_N					PCIE0_RX0_N
	S90	B24	PCIE1_TX0_P					PCIE1_TX0_P
	S91	C25	PCIE1_TX0_N					PCIE1_TX0_N
	S87	A21	PCIE1_RX0_P					PCIE1_RX0_P
	S88	B22	PCIE1_RX0_N					PCIE1_RX0_N
	S146	A15	HSIO.PCIE0.WAKE_B			LSIO.GPIO4.IO28	GPIO4_28	LSIO.GPIO4.IO28
	P75	D20	HSIO.PCIE0.PERST_B			LSIO.GPIO4.IO29	GPIO4_29	LSIO.GPIO4.IO29
	S76	G25	HSIO.PCIE1.PERST_B			LSIO.GPIO5.IO00	GPIO5_00	LSIO.GPIO5.IO00
SATA	P48	B16	PCIE_SATA0_TX0_P					PCIE_SATA0_TX0_P
	P49	C17	PCIE_SATA0_TX0_N					PCIE_SATA0_TX0_N
	P51	A19	PCIE_SATA0_RX0_P					PCIE_SATA0_RX0_P
	P52	B20	PCIE_SATA0_RX0_N					PCIE_SATA0_RX0_N
	S54	BD30	MIPI_DSI0.GPIO0.IO00	MIPI_DSI0.PWM0.OUT		LSIO.GPIO1.IO18	GPIO1_18	LSIO.GPIO1.IO18
UART0	P130	AV50	DMA.UART0.RX			LSIO.GPIO0.IO20	GPIO0_20	DMA.UART0.RX
	P129	AV48	DMA.UART0.TX			LSIO.GPIO0.IO21	GPIO0_21	DMA.UART0.TX
	P132	AU45	DMA.UART0.RTS_B	LSIO.PWM0.OUT	DMA.UART2.RX	LSIO.GPIO0.IO22	GPIO0_22	DMA.UART0.RTS_B
	P131	AW49	DMA.UART0.CTS_B	LSIO.PWM1.OUT	DMA.UART2.TX	LSIO.GPIO0.IO23	GPIO0_23	DMA.UART0.CTS_B
UART1	P136	AU51	M40.I2C0.SDA	M40.UART0.TX	M40.GPIO0.IO03	LSIO.GPIO0.IO07	GPIO0_07	
		AY48	DMA.UART1.TX	DMA.SPI3.SCK		LSIO.GPIO0.IO24	GPIO0_24	
	P137	AM44	M40.I2C0.SCL	M40.UART0.RX	M40.GPIO0.IO02	LSIO.GPIO0.IO06	GPIO0_06	
		AT44	DMA.UART1.RX	DMA.SPI3.SDO		LSIO.GPIO0.IO25	GPIO0_25	
	P138	AR43	DMA.UART1.RTS_B	DMA.SPI3.SDI	DMA.UART1.CTS_B	LSIO.GPIO0.IO26	GPIO0_26	
	P139	AV46	DMA.UART1.CTS_B	DMA.SPI3.CS0	DMA.UART1.RTS_B	LSIO.GPIO0.IO27	GPIO0_27	

Interface/ Function	SMARC Edge Pin Number	i.MX8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
UART3	P135	AP44	M41.TPM0.CH0	M41.TPM0.CH0	DMA.UART3.RX	LSIO.GPIO0.IO12	GPIO0_12	DMA.UART3.RX
	P134	AU47	M41.TPM0.CH1	M41.TPM0.CH1	DMA.UART3.TX	LSIO.GPIO0.IO13	GPIO0_13	DMA.UART3.TX
UART4	P141	AR47	M40.GPIO0.IO00	M40.TPM0.CH0	DMA.UART4.RX	LSIO.GPIO0.IO08	GPIO0_08	DMA.UART4.RX
	P140	AU53	M40.GPIO0.IO01	M40.TPM0.CH1	DMA.UART4.TX	LSIO.GPIO0.IO09	GPIO0_09	DMA.UART4.TX
Audio SAI0	S51	AY6	DMA.SPI0.SDI	AUD.SAI0.TXD		LSIO.GPIO3.IO03	GPIO3_04	AUD.SAI0.TXD
	S52	BA5	DMA.SPI0.SDI	AUD.SAI0.RXD		LSIO.GPIO3.IO04	GPIO3_04	AUD.SAI0.RXD
	S53	BA3	DMA.SPI0.CS1	AUD.SAI0.TXC		LSIO.GPIO3.IO06	GPIO3_06	AUD.SAI0.TXC
	S50	AY2	DMA.SPI2.CS1	AUD.SAI0.TXFS		LSIO.GPIO3.IO11	GPIO3_11	AUD.SAI0.TXFS
Audio SAI1	S41	AV4	AUD.SAI1.RXD	AUD.SAI0.TXFS		LSIO.GPIO3.IO13	GPIO3_13	AUD.SAI1.RXD
	S42	AU5	AUD.SAI1.TXC	AUD.SAI0.TXC		LSIO.GPIO3.IO15	GPIO3_15	AUD.SAI1.TXFS
	S40	AU1	AUD.SAI1.TXD	AUD.SAI1.RXC		LSIO.GPIO3.IO16	GPIO3_16	AUD.SAI1.TXFS
	S39	AV2	AUD.SAI1.TXFS	AUD.SAI1.RXFS		LSIO.GPIO3.IO17	GPIO3_17	AUD.SAI1.TXFS
	S38	BD4	AUD.ACM.MCLK_OUT0	AUD.ESAI0.TX_HF_CLK		LSIO.GPIO3.IO01	GPIO3_01	AUD.ACM.MCLK_OUT0
CAN	P144	C5	DMA.FLEXCAN0.RX			LSIO.GPIO3.IO29	GPIO3_29	DMA.FLEXCAN0.RX
	P143	H6	DMA.FLEXCAN0.TX			LSIO.GPIO3.IO30	GPIO3_30	DMA.FLEXCAN0.TX
	P146	E5	DMA.FLEXCAN1.RX			LSIO.GPIO3.IO31	GPIO3_31	DMA.FLEXCAN1.RX
	P145	G7	DMA.FLEXCAN1.TX			LSIO.GPIO4.IO00	GPIO4_00	DMA.FLEXCAN1.TX
GPIO	P108	BL23	MIPI_CSI0.GPIO0.IO00	DMA.I2C0.SCL		LSIO.GPIO1.IO27	GPIO1_27	LSIO.GPIO1.IO27
	P109	BN15	MIPI_CSI1.GPIO0.IO00	DMA.UART4.RX		LSIO.GPIO1.IO30	GPIO1_30	LSIO.GPIO1.IO30
	P110	BM22	MIPI_CSI0.GPIO0.IO01	DMA.I2C0.SDA		LSIO.GPIO1.IO28	GPIO1_28	LSIO.GPIO1.IO28
	P111	BN13	MIPI_CSI1.GPIO0.IO01	DMA.UART4.TX		LSIO.GPIO1.IO31	GPIO1_31	LSIO.GPIO1.IO31
	P112	D8	CONN.USDHC2.WP			LSIO.GPIO4.IO11	GPIO4_11	LSIO.GPIO4.IO11
	P113	BA51	LSIO.GPT1.COMPARE	LSIO.PWM2.OUT	LSIO.KPP0.ROW5	LSIO.GPIO0.IO19	GPIO0_19	LSIO.GPIO0.IO19
	P114	AL45	DMA.SIM0.CLK			LSIO.GPIO0.IO00	GPIO0_00	LSIO.GPIO0.IO00
	P115	AP48	DMA.SIM0.RST			LSIO.GPIO0.IO01	GPIO0_01	LSIO.GPIO0.IO01
	P116	AN45	DMA.SIM0.IO			LSIO.GPIO0.IO02	GPIO0_02	LSIO.GPIO0.IO02
	P117	AL43	DMA.SIM0.PD	DMA.I2C3.SCL		LSIO.GPIO0.IO03	GPIO0_03	LSIO.GPIO0.IO03
	P118	AT48	DMA.SIM0.POWER_EN	DMA.I2C3.SDA		LSIO.GPIO0.IO04	GPIO0_04	LSIO.GPIO0.IO04
	P119	AP46	DMA.SIM0.POWER_EN			LSIO.GPIO0.IO05	GPIO0_05	LSIO.GPIO0.IO05
I2C	S48	AY52	LSIO.GPT0.CLK	DMA.I2C1.SCL	LSIO.KPP0.COL4	LSIO.GPIO0.IO14	GPIO0_14	DMA.I2C1.SCL
	S49	AV52	LSIO.GPT0.CAPTURE	DMA.I2C1.SDA	LSIO.KPP0.COL5	LSIO.GPIO0.IO15	GPIO0_15	DMA.I2C1.SDA
	P126	AR45	M41.I2C0.SCL	M41.UART0.RX	M41.GPIO0.IO02	LSIO.GPIO0.IO10	GPIO0_10	LSIO.GPIO0.IO10

Interface/ Function	SMARC Edge Pin Number	i.MX8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
Control Signal	S145	BC53	SCU.GPIO0.IOXX_PMIC_MEMC_ON					SCU.GPIO0.IOXX_PMIC_MEMC_ON
	S157	BC49	SCU.TCU.TEST_MODE_SELECT					SCU.TCU.TEST_MODE_SELECT

2.11 i.MX8 Pin Multiplexing on Expansion Connector

The below table provides the details of i.MX8 Processor pin connections to the Expansion connector with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX8 Hardware User's Manual.

Table 8: i.MX8 Pin Multiplexing on Expansion Connector interfaces

Interface/ Function	Expansion Connector Pin Number	i.MX8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
LVDS0 Channel0	28	BL41	LVDS0_CH0_CLK_N					LVDS0_CH0_CLK_N
	26	BN41	LVDS0_CH0_CLK_P					LVDS0_CH0_CLK_P
	46	BK42	LVDS0_CH0_TX0_N					LVDS0_CH0_TX0_N
	44	BM42	LVDS0_CH0_TX0_P					LVDS0_CH0_TX0_P
	52	BL43	LVDS0_CH0_TX1_N					LVDS0_CH0_TX1_N
	50	BN43	LVDS0_CH0_TX1_P					LVDS0_CH0_TX1_P
	34	BK44	LVDS0_CH0_TX2_N					LVDS0_CH0_TX2_N
	32	BM44	LVDS0_CH0_TX2_P					LVDS0_CH0_TX2_P
	40	BL45	LVDS0_CH0_TX3_N					LVDS0_CH0_TX3_N
	38	BN45	LVDS0_CH0_TX3_P					LVDS0_CH0_TX3_P
LVDS0 Channel1	55	BG45	LVDS0_CH1_CLK_N					LVDS0_CH1_CLK_N
	57	BH46	LVDS0_CH1_CLK_P					LVDS0_CH1_CLK_P
	51	BG43	LVDS0_CH1_TX0_N					LVDS0_CH1_TX0_N
	49	BH44	LVDS0_CH1_TX0_P					LVDS0_CH1_TX0_P
	43	BG41	LVDS0_CH1_TX1_N					LVDS0_CH1_TX1_N
	45	BH42	LVDS0_CH1_TX1_P					LVDS0_CH1_TX1_P
	37	BG39	LVDS0_CH1_TX2_N					LVDS0_CH1_TX2_N
	39	BH40	LVDS0_CH1_TX2_P					LVDS0_CH1_TX2_P
	31	BG37	LVDS0_CH1_TX3_N					LVDS0_CH1_TX3_N
	33	BH38	LVDS0_CH1_TX3_P					LVDS0_CH1_TX3_P
TAMPER	58	BE41	SNVS_TAMPER_IN0					SNVS_TAMPER_IN0
	61	BE43	SNVS_TAMPER_IN1					SNVS_TAMPER_IN1
	73	BD46	SNVS_TAMPER_OUT0					SNVS_TAMPER_OUT0
	63	BD42	SNVS_TAMPER_OUT1					SNVS_TAMPER_OUT1
CAN2	91	C3	FLEXCAN2_RX			LSIO.GPIO4.IO01	GPIO4_01	FLEXCAN2_RX
	99	E7	FLEXCAN2_TX			LSIO.GPIO4.IO02	GPIO4_02	FLEXCAN2_TX

Interface/ Function	Expansion Connector Pin Number	i.MX8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
HDMI RX	67	BJ9	HDMI_RX0_CEC					HDMI_RX0_CEC
	1	BL11	HDMI_RX0_CLK_N					HDMI_RX0_CLK_N
	3	BM12	HDMI_RX0_CLK_P					HDMI_RX0_CLK_P
	13	BL15	HDMI_RX0_DATA0_N					HDMI_RX0_DATA0_N
	15	BM16	HDMI_RX0_DATA0_P					HDMI_RX0_DATA0_P
	19	BL17	HDMI_RX0_DATA1_N					HDMI_RX0_DATA1_N
	21	BM18	HDMI_RX0_DATA1_P					HDMI_RX0_DATA1_P
	25	BL19	HDMI_RX0_DATA2_N					HDMI_RX0_DATA2_N
	27	BM20	HDMI_RX0_DATA2_P					HDMI_RX0_DATA2_P
	7	BL13	HDMI_RX0_ARC_N					HDMI_RX0_ARC_N
	9	BM14	HDMI_RX0_ARC_P					HDMI_RX0_ARC_P
	69	BF14	HDMI_RX0_HPD					HDMI_RX0_HPD
	71	BE13	HDMI_RX0_DDC_SDA					HDMI_RX0_DDC_SDA
	79	BH10	HDMI_RX0_DDC_SCL					HDMI_RX0_DDC_SCL
	56	BN11	HDMI_RX0_MON_5V					HDMI_RX0_MON_5V
ESAI1	77	BE11	AUD.ESAI1.FSR			LSIO.GPIO2.IO04		AUD.ESAI1.FSR
	65	BF12	AUD.ESAI1.FST			LSIO.GPIO2.IO05		AUD.ESAI1.FST
	75	BD12	AUD.ESAI1.SCKR			LSIO.GPIO2.IO06		AUD.ESAI1.SCKR
	92	AY10	AUD.ESAI1.SCKT	AUD.SAI2.RXC		LSIO.GPIO2.IO07		AUD.ESAI1.SCKT
	81	BF10	AUD.ESAI1.TX0	AUD.SAI2.RXD		LSIO.GPIO2.IO08		AUD.ESAI1.TX0
	87	BA11	AUD.ESAI1.TX1	AUD.SAI2.RXFS		LSIO.GPIO2.IO09		AUD.ESAI1.TX1
	98	AU11	AUD.ESAI1.TX2_RX3			LSIO.GPIO2.IO10		AUD.ESAI1.TX2_RX3
	96	AV10	AUD.ESAI1.TX3_RX2			LSIO.GPIO2.IO11		AUD.ESAI1.TX3_RX2
	89	AY12	AUD.ESAI1.TX4_RX1			LSIO.GPIO2.IO12		AUD.ESAI1.TX4_RX1
	100	AT10	AUD.ESAI1.TX5_RX0			LSIO.GPIO2.IO13		AUD.ESAI1.TX5_RX0
SPDIF	94	BC7	AUD.SPDIF0.RX	AUD.MQS.R	AUD.ACM.MCLK_IN1	LSIO.GPIO2.IO14	GPIO2_14	AUD.SPDIF0.RX
	85	BC9	AUD.SPDIF0.TX	AUD.MQS.L	AUD.ACM.MCLK_OUT1	LSIO.GPIO2.IO15	GPIO2_15	AUD.SPDIF0.TX
		AY50	LSIO.GPT1.CAPTURE	DMA.I2C2.SDA	LSIO.KPP0.ROW4	LSIO.GPIO0.IO18		
	83	BD6	AUD.SPDIF0.EXT_CLK	DMA.DMA0.REQ_IN0		LSIO.GPIO2.IO16	GPIO2_16	AUD.SPDIF0.EXT_CLK
		BA53	LSIO.GPT1.CLK	DMA.I2C2.SCL	LSIO.KPP0.COL7	LSIO.GPIO0.IO17		
MIPI CSI0	82	BE25	MIPI_CSI0.DN2					MIPI_CSI0.DN2
	80	BF24	MIPI_CSI0.DP2					MIPI_CSI0.DP2
	88	BE17	MIPI_CSI0.DN3					MIPI_CSI0.DN3

Interface/ Function	Expansion Connector Pin Number	i.MX8 CPU Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	86	BF16	MIPI_CSI0.DP3					MIPI_CSI0.DP3
MLB	68	D32	CONN.MLB.PADP_CLK					CONN.MLB.PADP_CLK
	70	E33	CONN.MLB.PADN_CLK					CONN.MLB.PADN_CLK
	74	D30	CONN.MLB.PADP_S					CONN.MLB.PADP_S
	76	E31	CONN.MLB.PADN_S					CONN.MLB.PADN_S
	62	F34	CONN.MLB.PADP_D					CONN.MLB.PADP_D
	64	E35	CONN.MLB.PADN_D					CONN.MLB.PADN_D
	97	E1	CONN.MLB.SIG	AUD.SAI3.RXD		LSIO.GPIO3.IO26	GPIO3_28	CONN.MLB.SIG
	95	D2	CONN.MLB.CLK	AUD.SAI3.RXD		LSIO.GPIO3.IO27	GPIO3_28	CONN.MLB.CLK
	93	E3	CONN.MLB.DATA	AUD.SAI3.RXD		LSIO.GPIO3.IO28	GPIO3_28	CONN.MLB.DATA

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX8 SMARC SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the ten VDD_IN pins and returned through the numerous GND pins on the connector. A Module will withstand an indefinite exposure to an applied VDD_IN that may vary over the 4.5V to 5.25V range, without damage, and it will operate over the entire VDD_IN range of 4.5V to 5.25V. Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins.

Table 9: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VDD_IN	4.5V[1]	5V	5.25V	±50mV

[1] VDD_IN can be set as low as 3.0V with sufficient current but without a FAN. As per specification FAN need minimum of 4.5V.

3.1.1 Power Input Sequencing

The i.MX8 SMARC SOM's Power Input sequence requirement is explained below.

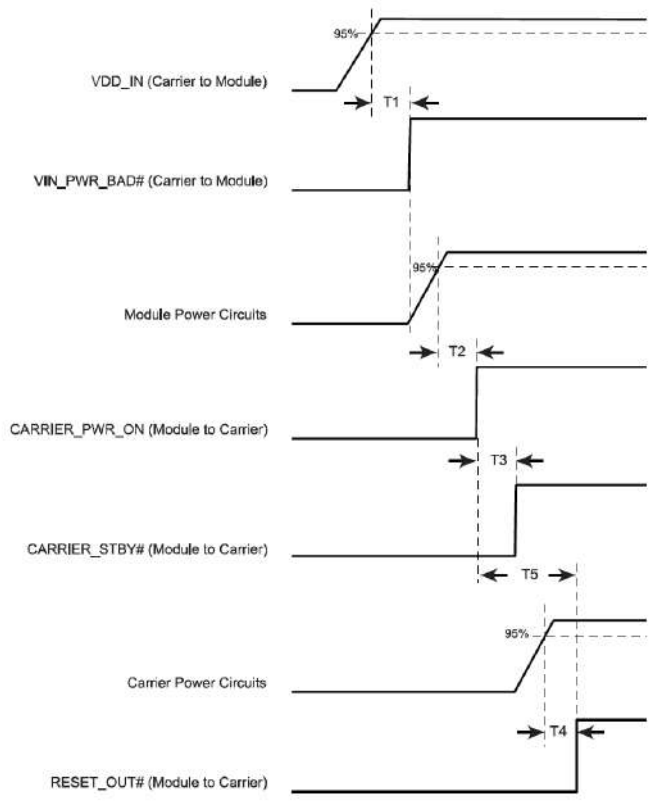

Figure 8: Power Input Sequencing

Table 10: Power Sequence Timing

Item	Description	Value
T1	VDD_IN rise time to VIN_PWR_BAD# rise time	≥ 0 ms
T2	VIN_PWR_BAD# rise time to SOM Power rise time	≥ 0 ms
T3	CARRIER_PWR_ON to CARRIER_STBY# timing	≥ 0 ms
T4	Carrier power circuits are up to RESET_OUT# rise	≥ 0 ms
T5	CARRIER_PWR_ON to CARRIER_RESET_OUT# timing	100 to 500ms

3.1.2 Power Consumption

Table 11: Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Video run in MIPI display (Gstreamer)	VDD_IN	2.14A/10.7W
Play Video run in MIPI display (Gplay)	VDD_IN	2.21A/11.05W
Camera Streaming	VDD_IN	1.73A/8.65W
Play 4K Video run in HDMI display (Gplay)	VDD_IN	2.51A/12.55W
Play Audio	VDD_IN	1.47A/7.35W
Ping Bluetooth	VDD_IN	1.45A/7.25W
Ping Wi-Fi	VDD_IN	1.47A/7.83W
Ping Ethernet (Eth0 and Eth1)	VDD_IN	1.66A/8.3W
eMMC to Standard SD file transfer	VDD_IN	1.8A/9W
eMMC to USB3.0 file transfer	VDD_IN	2.01A/10.05W
eMMC to SATA file transfer	VDD_IN	1.96A/9.8W
Bluetooth file transfer	VDD_IN	1.46A/7.3W
Wi-Fi file transfer	VDD_IN	1.47A/7.35W
Ethernet Streaming (Video Play)	VDD_IN	1.89A/9.45W
GPU Processor -Graphics 3D Test	VDD_IN	2.15A/10.75W
Dhrystone	VDD_IN	1.77A/8.85W
Maximum Power Test: • Run the below during Maximum Power Test, • Play Video run in MIPI display (Gplay) • Camera Streaming • Ethernet (eth0 & eth1) Run the ping (65500 packet size) • Wi-Fi- Run the ping teston back ground • FileTransfer - Transfer the 1GB files in storage devices • Run the dry2 application on back ground • GPU Processor -Graphics 3D Test	VDD_IN	3.9A/19.5W
Low Power Mode Power Consumption		
System Idle Mode.	VDD_IN	1.05A/5.25W
Deep Sleep Mode.	VDD_IN	0.67A/3.35W
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	5.1µA/15.3µW

[1] *Power consumption measurements are done in iWave 's i.MX8 QM CPU based SMARC Development platform with iWave 's iW-PRFHZ-SC-01-R4.0-REL0.1-Linux5.4.24.*

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX8 SMARC SOM.

Table 12: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.2.2 Heat Sink/ Heat Spreader

For any highly integrated System On Modules, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the CPU.

Heat spreader acts as thermal coupling device between Module and external thermal solution. Heat spreader also provides thermal coupling to CPU via gap filler for better heat exchange. Heat spreader is not a complete thermal solution by itself. Heat spreader has to be used with application specific thermal solutions like heat sinks, Chassis, fans, Heat pipes etc.

Note: iWave supports Heat Sink/ Heat Spreader Solution for i.MX8 SMARC SOM SOM. For more information on Heat Sink/ Heat Spreader contact iWave support team. Do not Power On the SOM without a proper thermal solution.

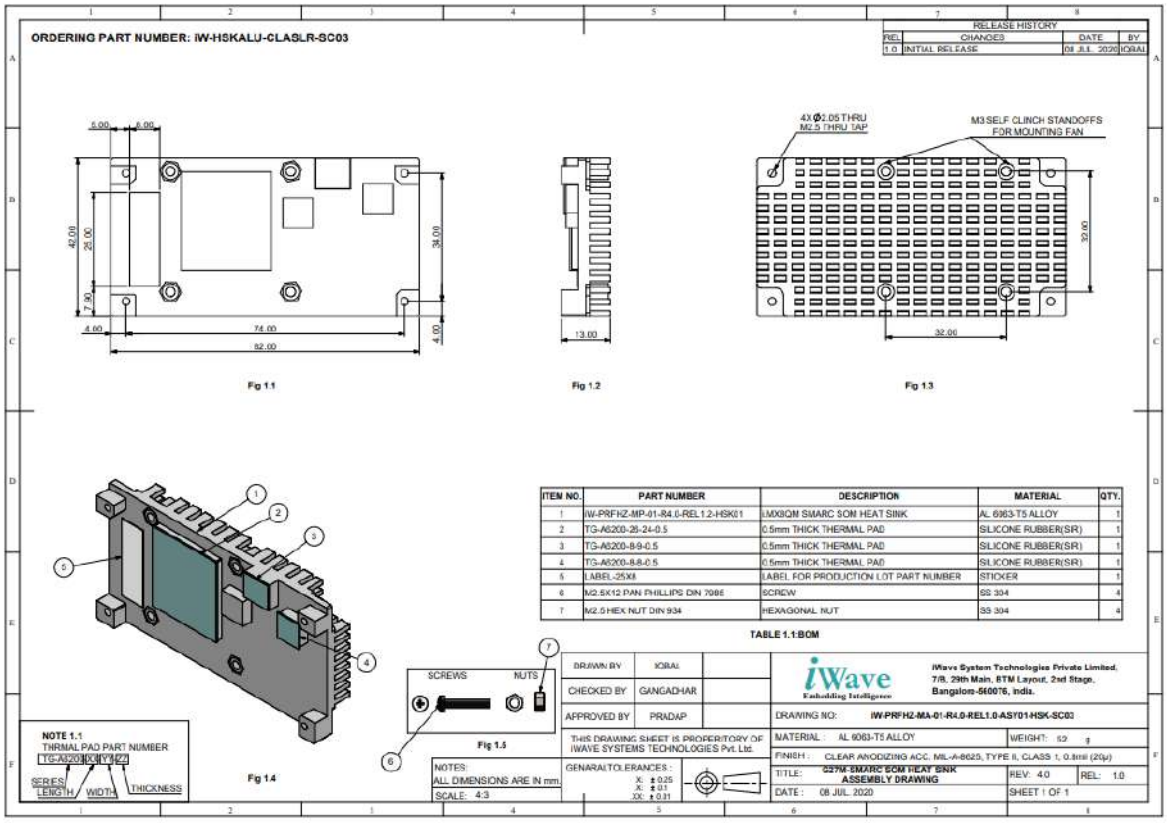

Figure 9: Mechanical dimension of Heat Sink

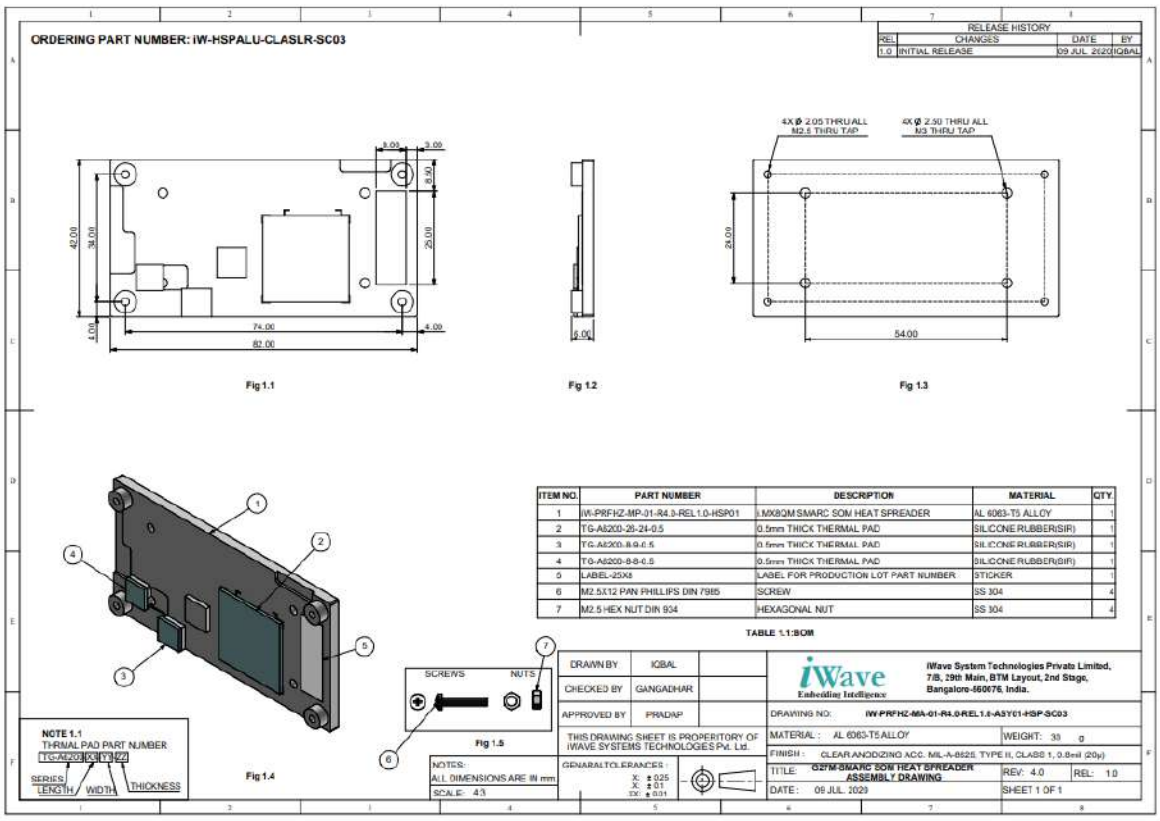

Figure 10: Mechanical dimension of Heat Spreader

3.2.3 RoHS Compliance

iWave's i.MX8 SMARC SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.4 Electrostatic Discharge

iWave's i.MX8 SMARC SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.3 Mechanical Characteristics

3.3.1 i.MX8 SMARC SOM Mechanical Dimensions

i.MX8 SMARC SOM PCB size is 50 mm x 82mm x 1.2mm. SMARC SOM mechanical dimension is shown below. (All dimensions are shown in mm)

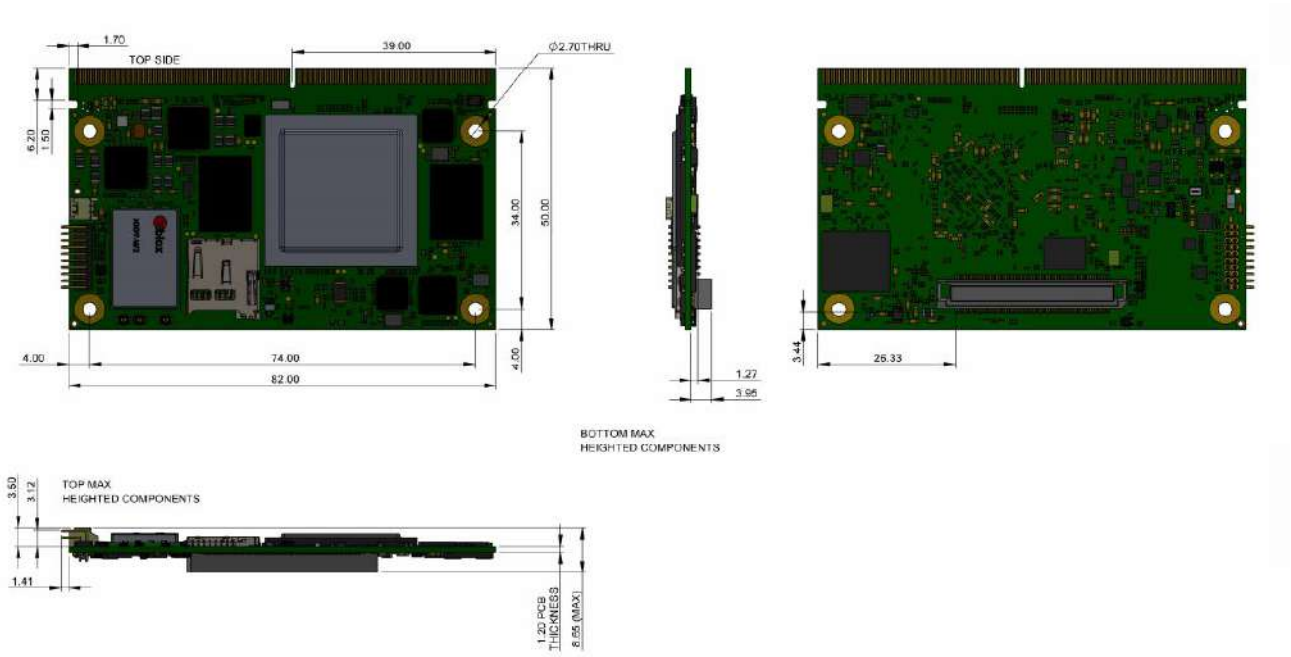

Figure 11: Mechanical dimensions of i.MX8 SMARC SOM

The i.MX8 SMARC SOM PCB thickness is 1.2mm±0.15mm, top side maximum height component is 3.5mm (debug Connector) which is optional in default configuration hence 3.4mm FAN header will be the maximum height on Top side in default configuration followed by Wi-Fi module (2.42mm) & Processor (2.17mm). In bottom side maximum height component is expansion connector (3.95mm) followed by Bulk Capacitors (1.35mm). Please refer the below figure which gives height details of the i.MX8 SMARC SOM.

Please refer the above figure for the details of the Expansion connector location on i.MX8 SMARC SOM.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX8 SMARC SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 13: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G27M - i.MX8 SMARC SOM (Industrial grade) without Expansion Connector		
iW-G27M-SCQM-4L004G-E016G-BIL	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L004G-E016G-BIM	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with boot code - Without Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L008G-E032G-BIL	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L008G-E032G-BIM	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with boot code - Without Wi-Fi, BT	-40°C to 85°C
iW-Rainbow G27M - i.MX8 SMARC SOM (Industrial grade) with Expansion Connector		
iW-G27M-SCQM-4L004G-E016G-LIG	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with Linux - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L004G-E016G-LIH	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with Linux - Without Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L004G-E016G-AIG	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with Android - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L004G-E016G-AIH	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with Android - Without Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L008G-E032G-LIG	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with Linux - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L008G-E032G-LIH	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with Linux - Without Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L008G-E032G-AIG	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with Android - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-SCQM-4L008G-E032G-AIH	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with Android - Without Wi-Fi, BT	-40°C to 85°C

Note: Some Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.

For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with QR Code on SOM.

5. APPENDIX

5.1 i.MX8 SMARC SOM Development Platform

iWave Systems supports iW-RainboW-G27D-i.MX8 SMARC SOM Development Platform which is targeted for quick validation of i.MX8 CPU based SMARC SOM and its features. Being a Nano-ITX form factor with 120mm x 120mm size, the carrier board is highly packed with all necessary interfaces & on-board connectors to validate complete SMARC supported features.

For more details on i.MX8 SMARC SOM Development Platform, visit the below web link.

https://www.iwavesystems.com/product/dev-kits/smarc/nxp-i-mx8-board/imx8-quadmax-smarc-development-kit.html

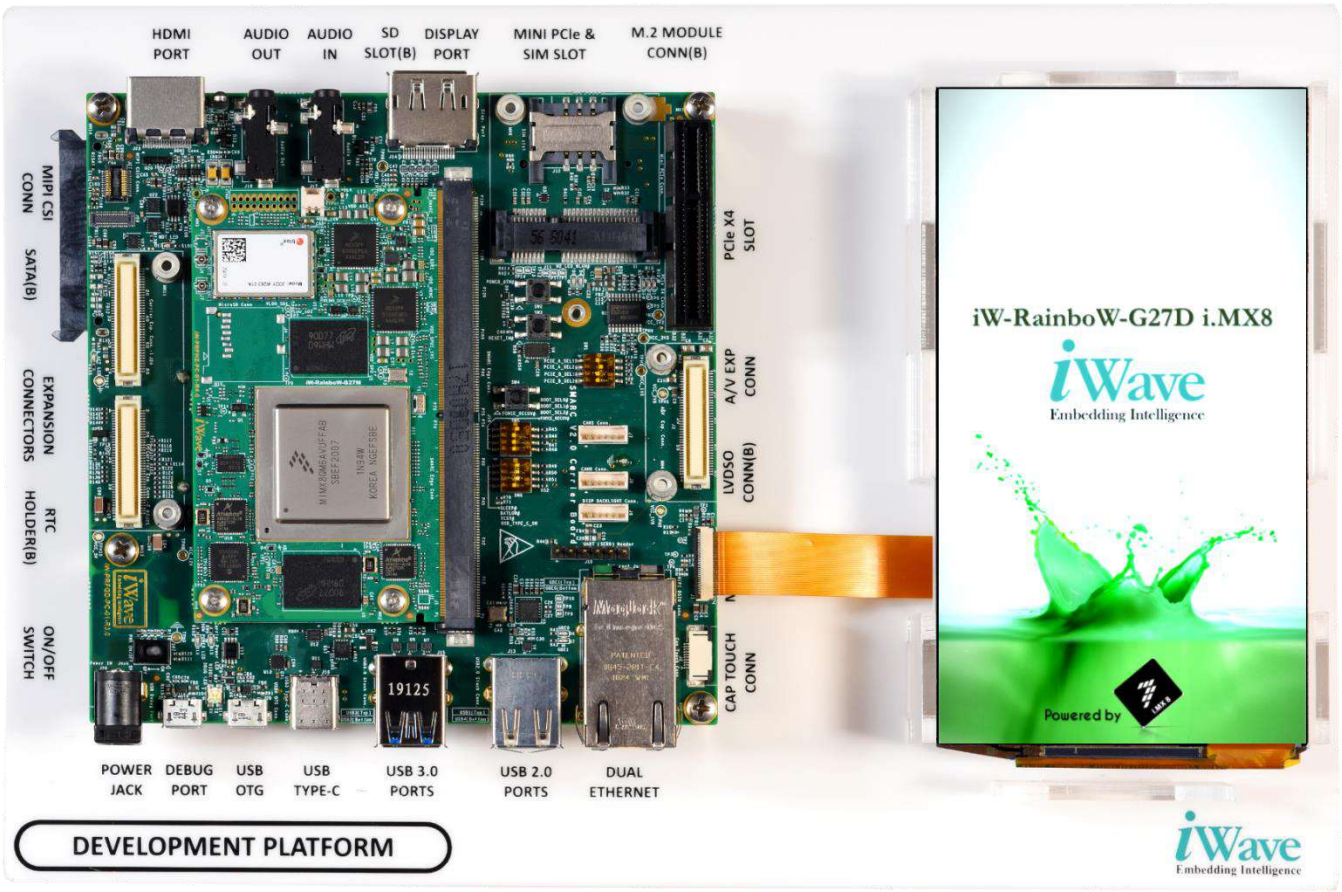

Figure 12: i.MX8 SMARC SOM Development Platform


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