8-bit Microcontroller

KM101EFG1 Series
Datasheet

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1 Overview

1.1 Overview

The KM101E series of 8-bit single-chip microcomputers incorporate multiple types of peripheral functions. This chip series is well suited for camera, TV, CD, printer, telephone, home automation, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. The KM101EFG1K has an internal 256 KB of ROM and 8 KB of RAM. The KM101EFG1H has an internal 164 KB of ROM and 8 KB of RAM. Peripheral functions include 6 external interrupts, 23 internal interrupts including NMI, 9 timer counters, 5 sets of serial inter-faces, A/D converter, watchdog timer, 1 set of automatic data transfer, synchronous output function and buzzer output. The configuration of this microcomputer is well suited for application as a system con-troller in camera, CD player, or minicomponent.

With three oscillation system (high frequency : max. 10 MHz / low frequency : 32.768 kHz and PLL : fre-quency multiplier of high frequency) contained on the chip, the system clock can be switched to high frequency input (high speed mode), PLL input (PLL mode), or to low frequency input (low speed mode). The system clock is generated by dividing the oscillation clock. The best operation clock for the system can be selected by switching its frequency by software. High speed mode has the normal mode which is based on 2-cycle clock (fpll/2) and the double speed mode which is based on the not-devided clock with fpll.

A machine cycle (min. instructions execution) in the normal mode is 200 ns when fosc is 10 MHz (at the time that PLL is not used). A machine cycle in the double speed mode is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).The package is 80-pin, LQFP.

1.2 Product Summary

This datasheet describes the following model. This product has identical functions.

Table: 1.1 Product Summary

Model	ROM Size	RAM Size	Classification	Package
KM101EFG1K	256 KB	8 KB	Flash EEPROM version	LQFP 80-pin
KM101EFG1H	164 KB	8 KB		

2. Hardware Functions

- Memory Capacity: ROM Capacity: 256 Kbyte / 164 Kbyte
  RAM Capacity: 8 Kbyte
- Package: LQFP 80-pin (14 mm square, 0.65 mm pitch)
- Machine Cycle: High-speed mode
  0.050 μs/20 MHz (2.7 V to 5.5 V)
  0.125 μs/ 8 MHz (1.8 V to 5.5 V)
  Low-speed mode
  62.5 μs/32 kHz (1.8 V to 5.5 V)
- Clock Gear: Operation speed of system clock is variable by changing the frequency.
- Multiplied Clock: High-speed frequency clock (fosc) can be multiplied by 2, 3, 4, 5, 6, 8 and 10.
- Memory Bank: Data memory space is expanded by the bank system.
  Bank for the source address/Bank for the destination address.
- ROM correction: Correcting address designation : up to 7 addresses possible
- Operation Mode: NORMAL mode (High speed mode)
  PLL mode
  SLOW mode (Low speed mode)
  HALT mode
  STOP mode
  (The operation clock can be switched in each mode.)
- Operating Voltage: 1.8 V to 5.5 V
- Operation ambient temperature
  -40°C to +85°C
- Interrupt: 29 levels
  <Watchdog timer>
  NMI-Watchdog timer overflow
  <Timer interrupts>
  TM0IRQ-Timer 0 interrupt (8-bit timer)
  TM1IRQ-Timer 1 interrupt (8-bit timer)
  TM2IRQ-Timer 2 interrupt (8-bit timer)
  TM3IRQ-Timer 3 interrupt (8-bit timer)
  TM4IRQ-Timer 4 interrupt (8-bit timer)
  TM6IRQ-Timer 6 interrupt (8-bit timer)
  TBIRQ-Clock timer interrupt
  TM7IRQ-Timer 7 interrupt (16-bit timer)
  T7OC2IRQ- Timer 7 interrupt (16-bit timer)
  TM8IRQ-Timer 8 interrupt (16-bit timer)
  T8OC2IRQ- Timer 8 interrupt (16-bit timer)

- Interrupt (continued)

<Serial interrupts>
SC0TIRQ-Serial interface 0 interrupt (UART transmission, synchronous)
SC0RIRQ-Serial interface 0 interrupt (UART reception)
(Peripheral function group interrupt)
SC1TIRQ-Serial interface 1 interrupt (UART transmission, synchronous)
SC1RIRQ-Serial interface 1 interrupt (UART reception)
(Peripheral function group interrupt)
SC2TIRQ-Serial interface 2 interrupt (UART transmission, synchronous)
SC2RIRQ-Serial interface 2 interrupt (UART reception)
SC4TIRQ- Serial interface 4 interrupt (synchronous)
SC4SIRQ- Serial interface 4 interrupt (Multi master I2C, Stop condition)
(Peripheral function group interrupt)
SC5TIRQ- Serial interface 5 interrupt (Slave I2C)
(Peripheral function group interrupt)

<A/D conversion end>
ADIRQ-AD conversion end

<Automatic Transfer Controller interrupts>
ATC1IRQ (Peripheral function group interrupt)

<External interrupts> Edge selectable
IRQ0:External interrupt
IRQ1:External interrupt
IRQ2:External interrupt (Both edges interrupt)
IRQ3:External interrupt (Both edges interrupt)
IRQ4:External interrupt (Both edges interrupt)
IRQ5:External interrupt (Key scan interrupt only)

- Timer Counter

10 timers All timer counters generate interrupt (9 can be operated independently)
8-bit timer for general use : 5 sets
8-bit free-running timer : 1 set
Time base timer : 1 set
16-bit timer for general use : 2 sets
Simple 8-bit timer : 1 set

Timer 0 (8-bit timer for general use)
- Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM0IOB), event count, remote control carrier output, simple pulse with measurement
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128,
  fs/2, fs/4, fs/8, fx, external clock, TimerA output
- Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0)

Timer 1 (8-bit timer for general use)
- Square wave output(timer pulse output), event count, 16-bit cascade connected with Timer 0 timer synchronous output event
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128,
  fs/2, fs/4, fs/8, fx, external clock, TimerA output

- Timer Counter (continued)

Timer 2 (8-bit timer for general use)
- Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM2IOB), event count, simple pulse with measurement, 24-bit cascade connected with Timer 0, 1 timer synchronous output event
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128,
  fs/2, fs/4, fs/8, fx, external clock, TimerA output
- Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

Timer 3 (8-bit timer for general use)
- Square wave output(timer pulse output), event count, remote control carrier output, 16bit cascade connected with Timer 2, 32-bit cascade connected with Timer 0, 1, 2
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128,
  fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 4 (8-bit timer for general use)
- Square wave output (timer pulse output), added pulse(2-bit) system PWM output, event count, serial transfer clock, simple pulse measurement
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128,
  fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 6 (8-bit free-running timer, Time base timer)

8-bit free-running timer
- Clock source
  fpll, fpll/2^{12}, fpll/2^{13}, fs, fx, fx/2^{12}, fx/2^{13}

Time base timer
- Interrupt generation cycle
  fpll/2^{7}, fpll/2^{8}, fpll/2^{9}, fpll/2^{10}, fpll/2^{13}, fpll/2^{15},
  fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}, fx/2^{15}

Timer 7 (16-bit timer for general use)
- Clock source
  fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16
  1/1, 1/2, 1/4, 1/16 of the external clock, TimerA output
- Hardware organization
  Compare register with double buffer : 2 sets
  Input capture register : 1 set
  Timer interrupt : 2 vectors
- Timer functions
  Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable), IGBT output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOB.
  Timer synchronous output, event count, Input capture function (Both edges can be operated).
- -Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

- Timer Counter (continued)

Timer 8 (16-bit timer for general use)
- Clock source
  fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16
  1/1, 1/2, 1/4, 1/16 of the external clock, TimerA output
- Hardware organization
  Compare register with double buffer : 2 sets
  Input capture register : 1 set
  Timer interrupt : 2 vectors
- Timer functions
  Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture (Both edge available), 32-bit cascade connected with Timer7, 32-bit PWM output, Input capture is available at 32-bit cascade.

TimerA output (Simple timer counter A)
Clock output for peripheral function

- Watchdog timer

Time-out cycle can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
On detection of errors, hard reset is done inside LSI.

- Synchronous output function

Timer synchronous output, interrupt synchronous output
Port 8 outputs the latched data, on the event timing of the synchronous output signal of timer
Timer1, Timer2, or Timer7, or of the external interrupt 2 (IRQ2).

- Buzzer Output/ Reverse Buzzer Output

Output frequency can be selected from $fpll/2^9$, $fpll/2^{10}$, $fpll/2^{11}$, $fpll/2^{12}$, $fpll/2^{13}$, $fpll/2^{14}$,$fx/2^3$,$fx/2^4$.

- Remote Control Carrier Output

A remote control carrier output with duty cycle of 1/2 or 1/3 of timer 0 or timer 3 output are available.

- A/D Converter

10-bit × 12 channels

- Data automatic transfer

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ATC1
Data is transferred automatically in all memory space
-External request/internal event request/software request
-Maximum transfer cycles are 255
-Support continuous serial transmission / reception.
-Burst transfer function (Urgent stop of interrupts is contained.)

- Serial Interface

5 channels

Serial 0 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
  fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4,
  Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 2 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

- Serial Interface (continued)

Serial 1 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
  fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4,
  Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 2 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 2 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
  fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4,
  Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 2 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 4 (multi master IIC / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
  fpll/2, fpll/4, fpll/8, fpll/32, fs/2, fs/4,
  Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 2 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Multi master IIC
- 7-bit of slave address can be set.
- General call communication mode handling

Serial5 (IIC slave interface)
- IIC high-speed transfer mode (communication speed: 400 kbps)
- 7-bit or 10-bit of slave address can be set.
- General call communication mode handling

- LED Driver — 7 pins (Push-pull structure)
- Automatic Reset
- Low voltage detection circuit

• Ports	I/O ports	70 pins
	LED (large current) driver pins	7 pins
	Serial interface pin	25 pins
	Timer I/O	15 pins
	Buzzer output	2 pins
	A/D input	12 pins
	External interrupt pin	5 pins
	XI/XO	2 pins
	Special pins	10 pins
	Operation mode input pins	3 pins
	Analog reference voltage input pin	1 pin
	Reset input pin	1 pin
	Oscillation pins	2 pins
	Power pins	3 pins

3 Pin Description

3.1 Pin configuration

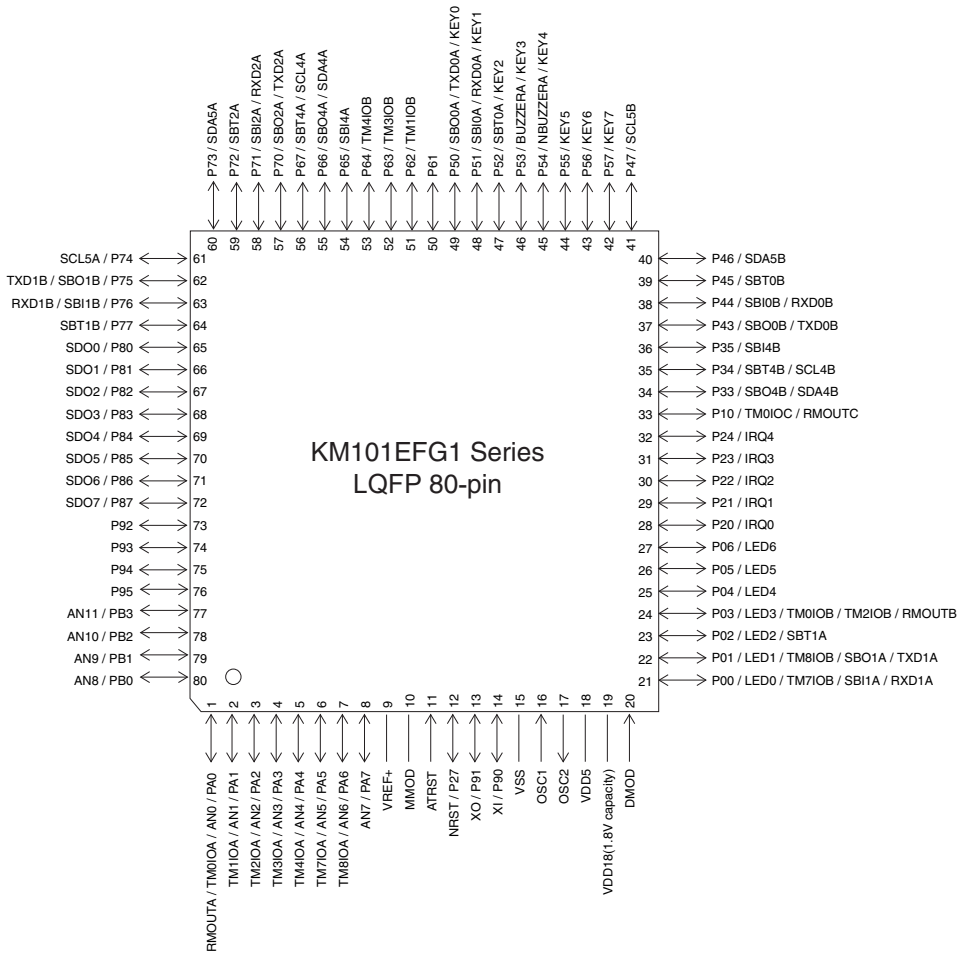

Figure: 3.1 Pin Configuration (LQFP 80-pin)

3.2. Pin Functions

Table: 3.1 Pin Functions

Pins	Pin No.	I/O	Function	Description
VSS VDD5	15 18	-	Power connect pins	Apply 1.8 V to 5.5 V to VDD5 and 0 V to VSS. Connect approximate 10-times capacity to connect to VDD18 pin for stabilization of internal power supply.
VDD18 (Capacity 1.8V)	19	-	Capacity connect pins	For internal power circuit output stability, connect at least one bypass capacitor of 1 uF or larger between VDD18 and VSS.
OSC1	16	Input	Clock input pins	Connect these oscillation pins to ceramic or crystal oscillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
OSC2	17	Output	Clock output pin	
XI	14	Input	Clock input pins	Connect these oscillation pins to crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. The chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to VSS and leave XO open.
XO	13	Output	Clock output pins	
NRST	12	Input	Reset pin [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Type. 50 kΩ). Setting this pin low initialize the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if “0” is written to P27 and the reset is initiated by soft-ware, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between NRST and VSS, it is recommended that a discharge diode be placed between NRST and VDD5.
ATRST	11	input	Auto reset setting pin	Input “H” to enable auto reset function and “L” to disable this function.
P00 P01 P02 P03 P04 P05 P06	21 22 23 24 25 26 27	I/O	I/O port0	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P0PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) Direct LED drive available at output. At reset, the input mode is selected and pull-up resistors are disabled (high impedance) .
P10	33	I/O	I/O port1	1-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P1PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance) .
P20 P21 P22 P23 P24	28 29 30 31 32	I/O	I/O port2	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P2PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P27	12	input	I/O port2	Port P27 has an N-channel open-drain configuration. When “0” is written and the reset is initiated by software, a low level will be output.

Pins	Pin No.	I/O	Function	Description
P33 P34 P35	34 35 36	I/O	I/O port3	3-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P3PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P43 P44 P45 P46 P47	37 38 39 40 41	I/O	I/O port4	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P4PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P50 P51 P52 P53 P54 P55 P56 P57	49 48 47 46 45 44 43 42	I/O	I/O port5	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P5PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P61 P62 P63 P64 P65 P66 P67	50 51 52 53 54 55 56	I/O	I/O port6	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P6PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P70 P71 P72 P73 P74 P75 P76 P77	57 58 59 60 61 62 63 64	I/O	I/O port7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P7PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P80 P81 P82 P83 P84 P85 P86 P87	65 66 67 68 69 70 71 72	I/O	I/O port8	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P90 P91 P92 P93 P94 P95	14 13 73 74 75 76	I/O	I/O port9	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).

Pins	Pin No.	I/O	Function	Description
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	1 2 3 4 5 6 7 8	I/O	I/O portA	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up resistor for each bit can be selected individually by the PAPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
PB0 PB1 PB2 PB3	80 79 78 77	I/O	I/O portB	4-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PBDIR register. A pull-up resistor for each bit can be selected individually by the PBPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
SBO0A SBO0B SBO1A SBO1B SBO2A SBO4A SBO4B	49 37 22 62 57 55 34	I/O	Serial interface transmission data output pins	Transmission data output pins for serial interface 0 to 4. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0A SBI0B SBI1A SBI1B SBI2A SBI4A SBI4B	48 38 21 63 58 54 36	input	Serial interface reception data input pins	Reception data output pins for serial interface 0 to 4. A pull-up resistor can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBT0A SBT0B SBT1A SBT1B SBT2A SBT4A SBT4B	47 39 23 64 59 56 35	I/O	Serial interface clock I/O pins	Clock I/O pins for serial interface 0 to 4. The output configuration, either CMOS push-pull or n- channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD, P6PLUD and P7PLUD registers. Select the clock I/O with the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1) according to the communication. These can be used as normal I/O pins when the serial interface is not used.
TXD0A TXD0B TXD1A TXD1B TXD2A	49 37 22 62 57	output	UART transmission data output pins	In the serial interface0 to 2 in UART mode, this pin is configured as the transmission data output pin. The output configuration, either CMOS push-pull or n- channel open-drain can be selected with the P0ODC, P4ODC, P5ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P4PLUD, P5PLUD and P7PLUD registers. Select the output mode at the P0DIR, P4DIR , P5DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC2MD1). These can be used as normal I/O pins when the serial interface is not used.

Pins	Pin No.	I/O	Function	Description
RXD0A RXD0B RXD1A RXD1B RXD2A	48 38 21 63 58	input	UART reception data input pins	In the serial interface0 to 2 in UART mode, this pin is configured as the reception data output pin. Pull-up resistor can be selected by the P0PLUD, P4PLUD, P5PLUD and P7PLUD registers. Select the output mode at the P0DIR, P4DIR, P5DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC2MD1). These can be used as normal I/O pins when the serial interface is not used.
SDA4A SDA4B SDA5A SDA5B	55 34 60 40	I/O	IIC data I/O pins	In the serial interface4, 5 in IIC mode, this pin is configured as the data input / output pin. For the output configuration, select n-channel open-drain with the P3ODC, P4ODC, P6ODC and P7ODC registers and pull-up resistors by the P3PLUD, P4PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P3DIR, P4DIR, P6DIR and P7DIR registers and serial data input / output mode by serial mode register 1 (SC4MD1, SC5MD1). These can be used as normal I/O pins when the serial interface is not used.
SCL4A SCL4B SCL5A SCL5B	56 35 61 41	I/O	IIC clock I/O pins	In the serial interface4, 5 in IIC mode, this pin is configured as the clock input / output pin. For the output configuration, select n-channel open-drain with the P3ODC, P4ODC, P6ODC and P7ODC registers and pull-up resistors by the P3PLUD, P4PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P3DIR, P4DIR, P6DIR and P7DIR registers and clock I/O mode by serial mode register 1 (SC4MD1, SC5MD1). These can be used as normal I/O pins when the serial interface is not used.
TM0IOA TM0IOB TM0IOC TM1IOA TM1IOB TM2IOA TM2IOB TM3IOA TM3IOB TM4IOA TM4IOB	1 24 33 2 51 3 24 4 52 5 53	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 4. To use this pin as event clock input, configure this as input by P0DIR register, P1DIR register, P6DIR register and PADIR register. In the input mode, pull-up resistors can be selected by the P0PLUD register, P1PLUD register, P6PLUD register and PAPLU register. For timer output, PWM signal output, select the special function pin by port 0 output mode register, port 1 output mode register, port 6 output mode register and port A out- put mode register ((P0OMD, P1OMD, P6OMD and PAOMD), and set to the output mode at P0DIR register, P1DIR register and PADIR register. These can be used as normal I/O pins when are not used as timer I/O pins.
RMOUTA RMOUTB RMOUTC	1 24 33	I/O	Remote control transmission signal output pins	Output pin for remote control transmission with a carrier signal. For remote control carrier output, select the special function pin by the port 0 output mode register, port 1 output mode register and port A output mode register (P0OMD, P1OMD and PAOMD), and set to the output mode by the P0DIR register, P1DIR register, P6DIR register and PADIR register. At the same time, select buzzer output at oscillation stabilization waiting control register. These can be used as normal I/O pins when the buzzer output is not used.
BUZZERA NBUZZERA	46 45	I/O	Buzzer output	Piezoelectric buzzer driving pin. Buzzer output is available to port5. The driving frequency can be selected with the DLYCTR register. To select buzzer output for port5, select the special function pin by the port 5 output mode register (P5OMD), and set to the output mode by the P5DIR register. At the same time, select buzzer output by the oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when the serial interface is not used.

Pins	Pin No.	I/O	Function	Description
TM7IOA TM7IOB TM8IOA TM8IOB	6 21 7 22	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer7 and 8. To use this pin as event clock input, configure this as input with the PADIR register. In the input mode, pull-up resistors can be selected by P0PLU register and PAPLU register. For timer output, PWM signal output, select the special function pin by the port 0 output mode register and port A output mode register (P0OMD and PAOMD), and set to the output mode at P0DIR register and PADIR register. These can be used as normal I/O pins when are not used as timer I/O pins.
SDO0 SDO1 SDO2 SDO3 SDO4 SDO5 SDO6 SDO7	65 66 67 68 69 70 71 72	output	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 8 synchronous output control register (P8SYO). Set to the output mode by the P8DIR register. These pins can be used as a normal I/O pins when not used for synchronous output.
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7 AN8 AN9 AN10 AN11	1 2 3 4 5 6 7 8 80 79 78 77	input	Analog input pins	Analog input pins for an 12-channel, 10-bit A/D converter. When not used for analog input, these pins can be used as normal input pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4	28 29 30 31 32	input	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to 4 can be selected with the IRQnICR register. IRQ1 can be set at both edges at pin voltage level. When not used for interrupts, these can be used as normal input pins.
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	49 48 47 46 45 44 43 42	input	Key interrupt input pins	Input pins for interrupt based on OR condition of pin inputs. These can be set to key input pins by 1-bit with the key interrupt control register (KEYT3_1IMD, KEYT3_2IMD) and by 2-bit with the key interrupt control register (KEYT3_1IMD). When not used for KEY input, these pins can be used as normal I/O pins.
LED0 LED1 LED2 LED3 LED4 LED5 LED6	21 22 23 24 25 26 27	I/O	LED drive pins	Large current output pins. When not used for LED output, these pins can be used as normal I/O pins.
MMOD	10	input	Memory mode switch input pins	Set always to VSS level.
DMOD	20	input	Mode switch input pins	Set always to VDD5 level.

4 Block Diagram

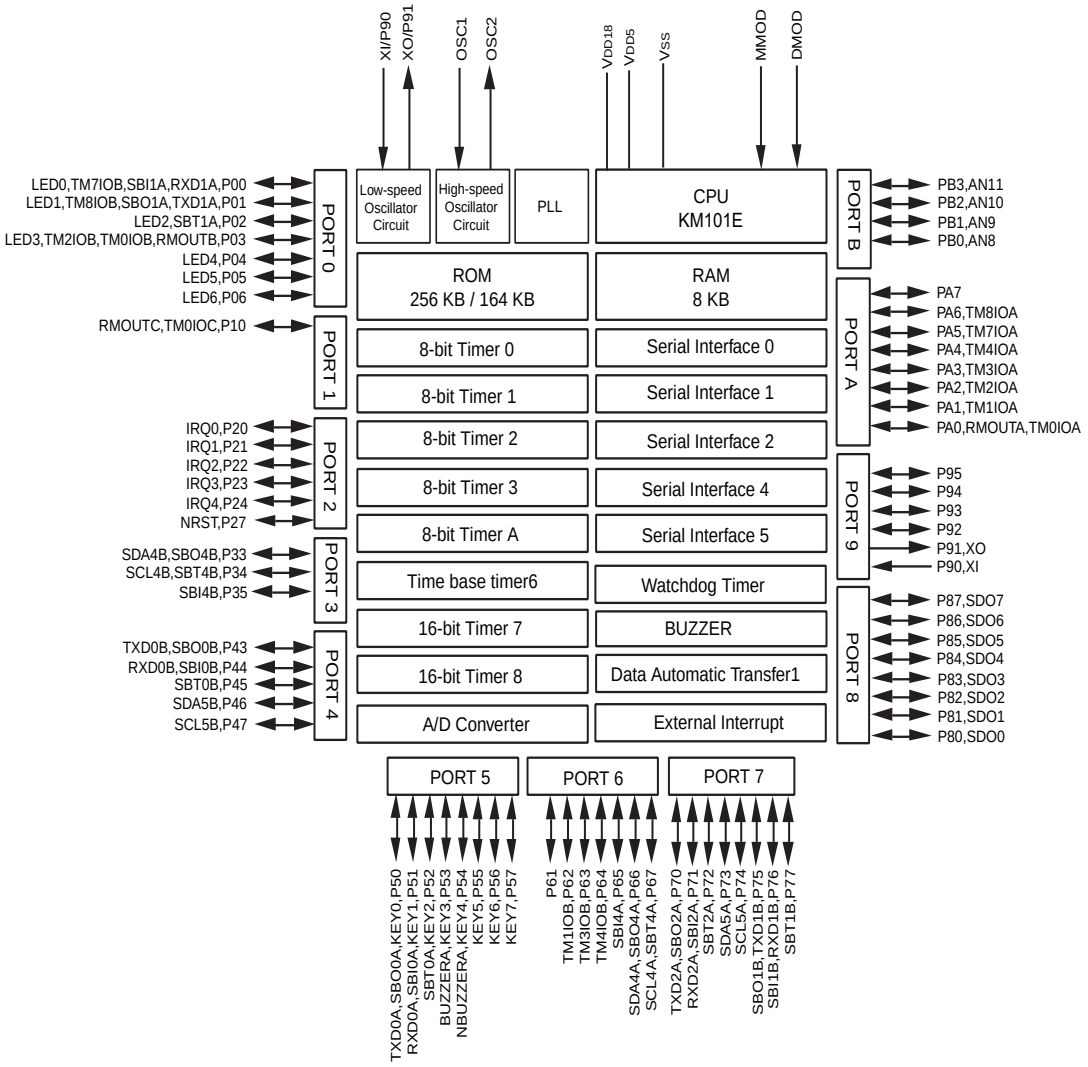

Figure: 4.1 Block Diagram

5 Electrical Characteristics

This datasheet describes the standard specification.

Machine cycle (system clock fs) is described based on the standard mode: double high oscillation fosc=fs (Normal mode), fosc=fs (Double speed mode), fs02≤ MHz (Multiplied by 2 to 10 mode) at NORMAL mode, or on the clock frequency:1/2 of low oscillation at SLOW mode. Please ask our sales offices for the product specifications.

Contents	Structure	CMOS integrated circuit
	Application	General purpose
	Function	CMOS, 8-bit, single chip micro controller

5.1 Absolute Maximum Ratings

Vss=0 V

	Parameter		Symbol	Rating	Unit
1	Power supply voltage		V_{DD5}	-0.3 to +7.0	V
2	Capacity connect pin voltage		V_{DD18}	-0.3 to +2.5	
3	Input pin voltage		V_I	-0.3 to V_{DD5} +0.3(up to 7.0 V)	V
4	output pin voltage		V_O	-0.3 to V_{DD5} +0.3(up to 7.0 V)	
5	I/O pin voltage		V_{IO1}	-0.3 to V_{DD5} +0.3(up to 7.0 V)	
6	Pointed output current	LED driving pins	I_{OL1} (peak)	30	mA
7		Any other than LED driving pins	I_{OL2} (peak)	20	
8		All pins	I_{OH} (peak)	-10	
9	Average output current *1	LED driving pins	I_{OL1} (avg)	20	
10		Any other than LED driving pins	I_{OL2} (avg)	15	
11		All pins	I_{OH} (avg)	-5	
12	Power dissipation		P_T	400	mW
13	Operating ambient temperature		T_{opr}	-40 to +85	°C
14	Storage temperature		T_{stg}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 0.1μF or larger between VDD5 power supply pin and the ground for latch-up prevention.

*3 Connect apprroximate 1μF capacitor between VDD18 power supply pin and the ground, and apprroximate 10-times capacitor connect to VDD18 between VDD5 power supply pin and the ground for the internal power supply stabilization.

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

5.2 Operating Conditions

V_{SS} =0 V
Ta=-40 °C to +85 °C

Paramete		Symbol	Concitions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage *5							
1	Power supply voltage	V_{DD1}	fs ≤ 8 MHz	1.8		5.5	V
2		V_{DD2}	fs ≤ 20 MHz	2.7		5.5	
3		V_{DD3}	fs = 16.384 kHz	1.8		5.5	
4	Voltage to maintain RAM data	V_{DD4}	During STOP mode	1.8		5.5	
Operating speed *6							
5	Minimum instruction execution time	tc1	V_{DD5} = 1.8 V to 5.5 V	0.125			µs
6		tc2	V_{DD5} = 2.7 V to 5.5 V	0.05			
7		tc3	V_{DD5} = 1.8 V to 5.5 V	61			

*5 fs : Machine clock frequency.

*6 t_{c1} to t_{c2} : In the case of multiplied clock by PLL or external high-speed clock as Machine clock.
t_{c3} : In the case of external high-speed clock as Machine clock.

V_{SS} = 0 V
Ta =- 40 °C + 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Crystal oscillator 1 Figure: 5.1 [NORMAL mode]							
8	Crystal frequency	f_{sosc-1}	V_{DD5}=within the range of operation (Refer to specified value of power supply1 to 3)	2.0		10	MHz
9	Internal feedback resistor	R_{f10}	V_{DD5}=5.0 V		980		kΩ
Crystal oscillator 1 Figure: 5.2 [SLOW mode]							
10	Crystal frequency	f_{sosc-1}	V_{DD5}=1.8 V to 5.5 V		32.768		kHz
11	Internal feedback resistor	R_{f20}	V_{DD5}=5.0 V		6.2		MΩ

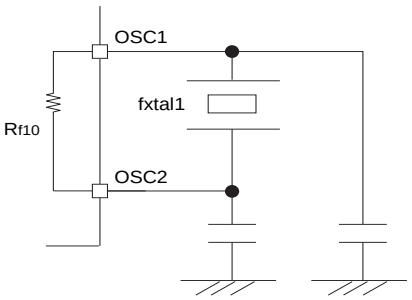

Figure: 5.1 Crystal oscillator 1

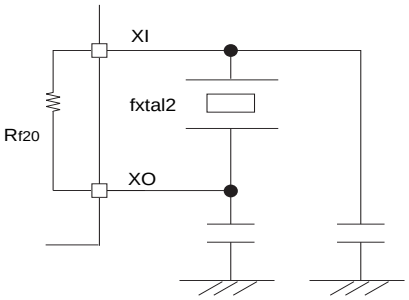

Figure: 5.2 Crystal oscillator 2

Note	Connect external capacitors suited for the used oscillator. The reference value denotes external capacity value based on our matching result. When crystal oscillator or ceramic oscillator is used, the oscillation frequency is changed depending on the value of capacitor. For external capacity value, please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

V_{DD5}=1.8 V to 5.5 V V_{SS}=0 V
Ta=-40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1(OSC2 is unconnected)							
12	Clock frequency	f_{hosc-2}		1.0		10.0	MHz
13	High level pulse width *7	t_{wh1}	Figure: 5.3	45.0			ns
14	Low level pulse width *7	t_{wl1}		45.0			
15	Rising time *8	t_{wr1}	Figure: 5.3	0		5.0	
16	Falling time *8	t_{wf1}		0		5.0	
External clock input 2 XI(XO is unconnected)							
17	Clock frequency	f_{sosc-2}			32.768		kHz
18	High level pulse width *7	t_{wh2}	Figure: 5.4		4.5		µs
19	Low level pulse width *7	t_{wl2}			4.5		
20	Rising time *8	t_{wr2}	Figure: 5.4	0		20	ns
21	Falling time *8	t_{wf2}		0		20	

*7 The clock duty rate in the standard mode should be 45% to 55%.

*8 Rising time and falling time are different by oscillation frequency.
The max value is not a specified value but a rough value.
Consult the manufacturer of the pin for the appropriate after full matching evaluation.

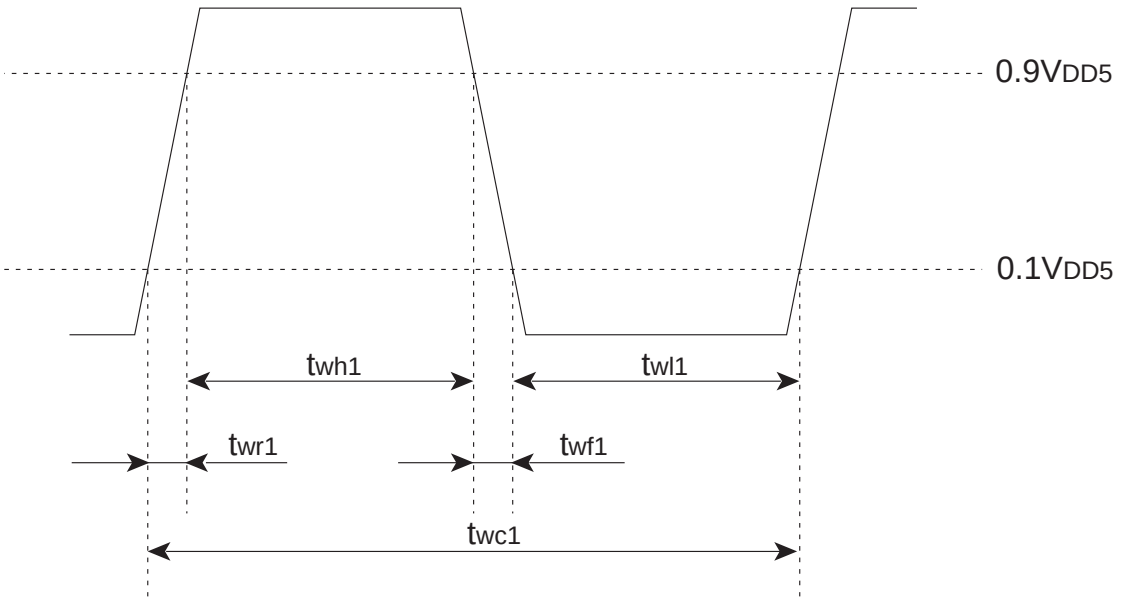

Figure: 5.3 f_{hosc-2} Timing Chart

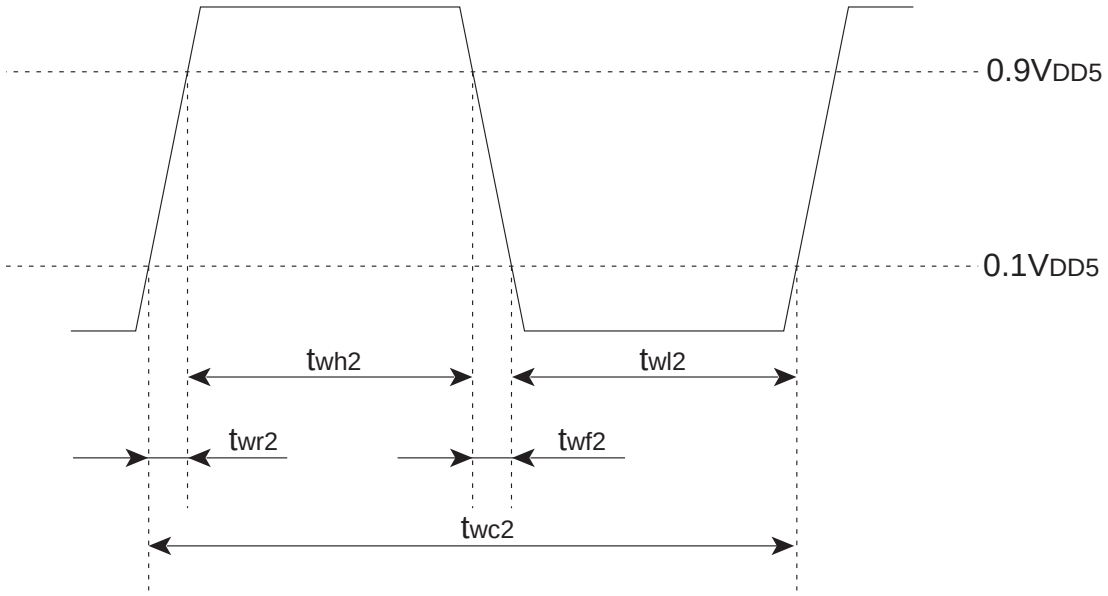

Figure: 5.4 f_{sosc-2} Timing Chart

5.3 DC Characteristics

V_{SS}=0 V
Ta=-40 °C to + 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current *9		(NORMAL mode : fs=fosc/2 SLOW mode : fs=fx/2)					
1	Power supply current	I_{DD1}	fosc=10 MHz [Double-speed mode:fs=fosc] V_{DD5}=5 V (In not using PLL) *10		5.2	11	mA
2		I_{DD2}	fosc=8 MHz [Double-speed mode:fs=fosc] V_{DD5}=5 V (In not using PLL) *11		4.7	9.4	
3		I_{DD3}	fosc=4 MHz [Double-speed mode:fs=fosc] V_{DD5}=5 V (In not using PLL) *11		3.4	6	
4		I_{DD4}	fosc=4 MHz [multiplied by 10:fs=20 MHz] V_{DD5}=5 V (In using PLL) *10		8.2	20	
5		I_{DD5}	fx=32.768 MHz [Normal mode:fs=fx/2] V_{DD5}=3 V Ta=25 °C		200	330	µA
6			fx=32.768 MHz [Normal mode:fs=fx/2] V_{DD5}=3 V Ta=85 °C			470	
7	Supply current during HALT1 mode	I_{DD6}	fx=32.768 MHz V_{DD5}=3 V Ta=25 °C		130	255	
8			fx=32.768 kHz V_{DD5}=3 V Ta=85 °C			300	
9	Supply current during STOP mode	I_{DD7}	V_{DD5}=5 V Ta=25 °C		125	240	
10			V_{DD5}=5 V Ta=85 °C			280	

*9 Measured under conditions at Ta=-40 °C without load. (pull-up / pull-down resistors are unconnected.)

- The supply current during operation, I_{DD1} to I_{DD5} are measured under the following conditions:
  After all I/O pins are set to input mode and the cpu mode is set to <NORMAL mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and a 10 MHz square wave of V_{DD5} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during operation, I_{DD5} is measured under the following conditions:
  After all I/O pins are set to input mode and the cpu mode is set to <SLOW mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and clock is supplied from internal low-speed oscillation circuit.
- The supply current during HALT1 mode, I_{DD6} is measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <HALT1 mode>, the input pins are at V_{DD5} level, and MMOD pin is at V_{SS} level.
- The supply current during STOP mode, I_{DD7} is measured under the following conditions:
  After the oscillation is set to <STOP mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and the OSC1 is unconnected.

*10 In case of setting “1” to bp2 of XSEL register (0x03F2F).

*11 In case of setting “0” to bp2 of XSEL register (0x03F2F).

V_{DD5}=1.8 V to 5.5 V V_{SS}=0 V
Ta=-40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 MMOD, DMOD, ATRST							
11	Input high voltage	V_{IH1}		0.8V_{DD5}		V_{DD5}	V
12	Input low voltage	V_{IL1}		0		0.2V_{DD5}	
13	Input leakage current	I_{LK1}	V_{IN}=0 V to V_{DD5}			± 2	µA
I/O pin 2 P27 (NRST)							
14	Input high voltage	V_{IH2}		0.8V_{DD5}		V_{DD5}	V
15	Input low voltage	V_{IL2}		0		0.15V_{DD5}	
16	Pull-up resistor	R_{RH2}	V_{DD5}=5.0V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
I/O pin 3 P10, P20 to P24, P33 to P35, P43 to P47, P50 to P57, P61 to P67, P70 to P77							
17	Input high voltage	V_{IH3}		0.8V_{DD5}		V_{DD5}	V
18	Input low voltage	V_{IL3}		0		0.2V_{DD5}	
19	Input leak current	I_{LK3}	V_{IN}=0 V to V_{DD5}			± 2	µA
20	Pull-up resistor	R_{RH3}	V_{DD5}=5.0V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
21	Pull-down resistor	R_{RL3}	V_{DD5}=5.0V V_{IN}=V_{DD5} Pull-down resistor ON	10	50	100	
22	Output high voltage	V_{OH3}	V_{DD5}=5.0V I_{OH}= -0.5 mA	4.5			V
23	Output low voltage	V_{OL3}	V_{DD5}=5.0V I_{OL}=1.0 mA			0.5	
I/O pin 4 P80 to P87, P90 to P95, PA0 to PA7, PB0 to PB3							
24	Input high voltage	V_{IH4}		0.8V_{DD5}		V_{DD5}	V
25	Input low voltage	V_{IL4}		0		0.2V_{DD5}	
26	Input leak current	I_{LK4}	V_{IN}=0 V to V_{DD5}			± 2	µA
27	Pull-up resistor	R_{RH4}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
28	Output high voltage	V_{OH4}	V_{DD5}=5.0 V I_{OH}=0.5 mA	4.5			V
29	Output low voltage	V_{OL4}	V_{DD5}=5.0 V I_{OL}=1.0 mA			0.5	
I/O pin 5 P00 to P06							
30	Input high voltage1	V_{IH5}		0.8V_{DD5}		V_{DD5}	V
31	Input low voltage1	V_{IL5}		0		0.2V_{DD5}	
32	Input leak current	I_{LK5}	V_{IN}=0 V to V_{DD5}			± 2	µA
33	Pull-up resistor	R_{RH5}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
34	Pull-down resistor	R_{RL5}	V_{DD5}=5.0 V V_{IN}=V_{DD5} Pull-down resistor ON	10	50	100	
35	Output high voltage	V_{OH5}	V_{DD5}=5.0V I_{OH}= -0.5 mA	4.5			V
36	Output low voltage1	V_{OL15}	V_{DD5}=5.0V I_{OL}=1.0 mA LED output OFF			0.5	
37	Output low voltage2	V_{OL25}	V_{DD5}=5.0V I_{OL}=15 mA LED output ON			1.0	

5.4 A/D Converter Characteristics

V_{DD5}=5.0 V V_{SS}=0 V
Ta=-40 °C to + 85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution					10	Bits
2	None-linearity error 1		V_{DD5} = 5.0 V, V_{SS} = 0 V, V_{REF+} = 5.0 V T_{AD} = 800 ns *12			±3	LSB
3	Differential non-linearity error 1					±3	
4	Zero transition voltage		V_{DD5} = 5.0 V, V_{SS} = 0 V, V_{REF+} = 5.0 V T_{AD} = 800 ns *12	-30	10	30	mV
5	Full-scale transition voltage			4970	4990	5030	
6	A/D conversion time		T_{AD} = 800 ns *12	12.93			µs
7			fx=32.768 kHz, T_{AD} = 15.26 µs *12	427.25			
8	Sampling time		T_{AD} = 800 ns *12	1.6			
9			fx=32.768 kHz T_{AD} = 15.26 µs *12	30.52			
10	Reference Voltage	V_{REF+}		1.8		V_{DD5}	V
11	Analog input voltage			V_{SS}		V_{REF+}	
12	Analog input leakage current		When channel is OFF V_{ADIN} = 0 V to 5.0 V			±2	µA
13	Reference voltage pin Leakage current		In Ladder resistance OFF $V_{ss} \leq V_{REF+} \leq V_{DD5}$			±5	
14	Ladder resistance	R_{LADD}	V_{DD5}= 5.0 V	15	40	80	kΩ

*12 T_{AD} is A/D conversion clock cycle.
The values of 2 to 5 are guaranteed on the condition that V_{DD5}=V_{REF+}=5 V, V_{SS}=0 V.

The reference voltage input VREF+ pin uses value of 2.0 V ≤ V_{REF+} ≤ V_{DD5}. When input voltage is V_{REF+} < 2.0 V, there is a possibility that the microcontroller malfunctions.

5.5 Auto Reset Characteristics

V_{DD5}= V_{RST} to 5.5 V V_{SS}=0 V
Ta=-40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
1	Operation voltage	V_{DD7}	When using auto reset	V_{RST}		5.5	V
Auto reset circuit							
2	Reset detection voltage	V_{RST1}	At rising	2.00	2.10	2.20	V
3	Reset detection voltage	V_{RST2}	At falling	1.90	2.00	2.10	
4	Rate of change power supply voltage	$\Delta t / \Delta V$		2			ms/V
Power supply current							
5	Auto reset circuit consumption	I_{DD8}	V_{DD5} = 5 V		1.5	3	μA

5.6 Flash EEPROM Programming Condition

V_{DD5} = 2.7 V to 5.5 V V_{SS} = 0 V
Ta=-40°C to +85°C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Voltage for rewriting	V_{DDEW}		2.7		5.5	V
2	Data retention period	E_{MAX}	Guaranteed number of rewritable times			1000	Time
3	Data retention period *1	T_{HOLD8}	Ta = 85 °C, P/E times ≤ 1000	10			Year

*1 Including time when power is turned off

5.7 Power Supply Voltage Detection Circuit

V_{DD5} = 1.8 V to 5.5 V V_{SS} = 0 V
Ta=-40°C to +85°C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
1	Power supply voltage detection level 1-1	V_{LVI11}	At rising	3.8	4.0	4.2	V
2	Power supply voltage detection level 1-2	V_{LVI12}	At falling	3.7	3.9	4.1	
3	Power supply voltage detection level 2-1	V_{LVI21}	At rising	3.6	3.8	4.0	
4	Power supply voltage detection level 2-2	V_{LVI22}	At falling	3.5	3.7	3.9	
5	Power supply voltage detection level 3-1	V_{LVI31}	At rising	3.4	3.6	3.8	
6	Power supply voltage detection level 3-2	V_{LVI32}	At falling	3.3	3.5	3.7	
7	Power supply voltage detection level 4-1	V_{LVI41}	At rising	3.2	3.4	3.6	
8	Power supply voltage detection level 4-2	V_{LVI42}	At falling	3.1	3.3	3.5	
9	Power supply voltage detection level 5-1	V_{LVI51}	At rising	3.0	3.2	3.4	
10	Power supply voltage detection level 5-2	V_{LVI52}	At falling	2.9	3.1	3.3	
11	Power supply voltage detection level 6-1	V_{LVI61}	At rising	2.8	3.0	3.2	
12	Power supply voltage detection level 6-2	V_{LVI62}	At falling	2.7	2.9	3.1	
13	Power supply voltage detection level 7-1	V_{LVI71}	At rising	2.7	2.8	2.9	
14	Power supply voltage detection level 7-2	V_{LVI72}	At falling	2.6	2.7	2.8	
15	Power supply voltage detection level 8-1	V_{LVI81}	At rising	2.5	2.6	2.7	
16	Power supply voltage detection level 8-2	V_{LVI82}	At falling	2.4	2.5	2.6	
17	Power supply voltage detection level 9-1	V_{LVI91}	At rising	2.3	2.4	2.5	
18	Power supply voltage detection level 9-2	V_{LVI92}	At falling	2.2	2.3	2.4	
19	Power supply voltage detection level 10-1	V_{LVI101}	At rising	2.1	2.2	2.3	
20	Power supply voltage detection level 10-2	V_{LVI102}	At falling	2.0	2.1	2.2	
21	Minimum pulse width	T_W		20	60		ms
22	Supply voltage change rate	$\Delta t / \Delta V$		2			ms/V
Consumption current							
23	Consumption current in power supply voltage detection circuit	I_{DD16}	V_{DD5} = 5.0 V		2	4	μA

6 Package Dimension

■ LQFP 80-pin (14 mm square, 0.65 mm pitch)

Units: mm

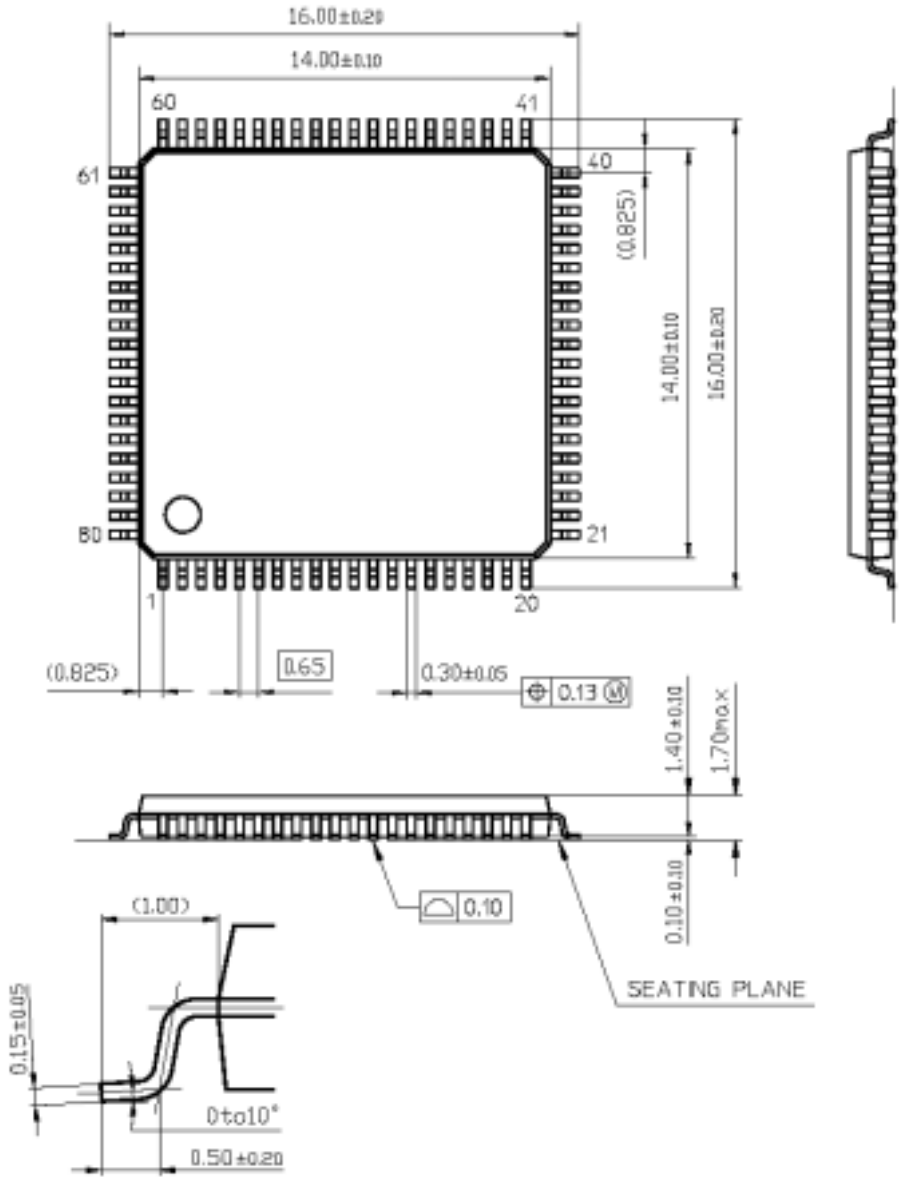

Figure: 6.1 Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

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