

# Digital Temperature Sensor and Thermal Watchdog with 2-Wire Interface

# LM75

## General Description

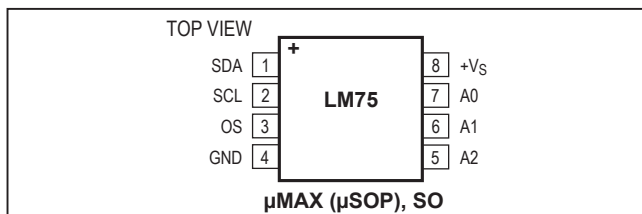
The LM75 temperature sensor includes a delta-sigma analog-to-digital converter, and a digital overtemperature detector. The host can query the LM75 through its I<sup>2</sup>C interface to read temperature at any time. The open-drain overtemperature output (OS) sinks current when the programmable temperature limit is exceeded. The OS output operates in either of two modes, comparator or interrupt. The host controls the temperature at which the alarm is asserted (T<sub>OS</sub>) and the hysteresis temperature below which the alarm condition is not valid (T<sub>HYST</sub>). Also, the LM75's T<sub>OS</sub> and T<sub>HYST</sub> registers can be read by the host. The address of the LM75 is set with three pins to allow multiple devices to work on the same bus. Power-up is in comparator mode, with defaults of T<sub>OS</sub> = +80°C and T<sub>HYST</sub> = +75°C. The 3.0V to 5.5V supply voltage range, low supply current, and I<sup>2</sup>C interface make the LM75 ideal for many applications in thermal management and protection.

## Applications

- Thermal System Management
- Thermal Protection
- Test Equipment
- Computers and Office Electronics

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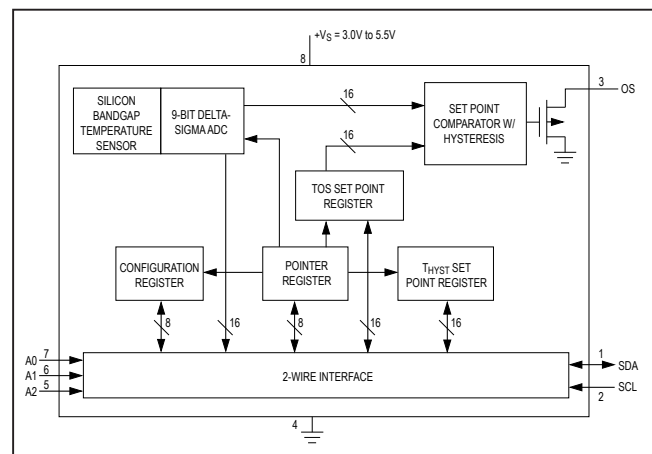
## Pin Configuration



## Features

- ISO (SOP) and µMAX® (µSOP) Packages
- I<sup>2</sup>C Bus Interface
- Separate Open-Drain OS Output Operates as Interrupt or Comparator/Thermostat Input
- Register Readback Capability
- Power-Up Defaults Permit Stand-Alone Operation as a Thermostat
- 3.0V to 5.5V Supply Voltage
- Low Operating Supply Current 250µA (typ), 1mA (max)
- 4µA (typ) Shutdown Mode Minimizes Power Consumption
- Up to Eight LM75s Can Be Connected to a Single Bus
- Pin- and/or Register-Compatible with Improved-Performance Maxim Sensors Including MAX7500, MAX6625, MAX6626, DS75LV, and DS7505

## Functional Diagram



## Ordering Information/Selector Guide

PART	PIN-PACKAGE	PKG	SUPPLY VOLTAGE (V)	TOP MARK
LM75BIM-3+	8 SO (SOP)	Bulk	3.3	LM75BMIM-3
LM75BIMX-3+	8 SO (SOP)	T&R	3.3	LM75BMIM-3
LM75BIMM-3+	8 µMAX (µSOP)	Bulk	3.3	T01B
LM75BIMMX-3+	8 µMAX (µSOP)	T&R	3.3	T01B
LM75BIM-5+	8 SO (SOP)	Bulk	5.0	LM75BIM-5
LM75BIMX-5+	8 SO (SOP)	T&R	5.0	LM75BIM-5
LM75BIMM-5+	8 µMAX (µSOP)	Bulk	5.0	T00B
LM75BIMMX-5+	8 µMAX (FSOP)	T&R	5.0	T00B

**Note:** Devices are specified over the -55°C to +125°C temperature range and include I<sup>2</sup>C noise filter.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T&R = Tape and reel.

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### Absolute Maximum Ratings (Note 1)

+V <sub>S</sub> to GND.....	-0.3V to +6.0V
OS, SDA, SCL to GND.....	-0.3V to +6.0V
All Other Pins to GND.....	-0.3V to (+V <sub>S</sub> + 0.3V)
Input Current at Any Pin (Note 2).....	5mA
Package Input Current (Note 2).....	20mA
OS Output Sink Current.....	10mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C) (Note 3)	
8-Pin μMAX (μSOP)	
(derate 4.5mW/°C above +70°C).....	362mW
8-Pin SO (SOP) (derate 5.9mW/°C above +70°C).....	471mW
Junction-to-Case Thermal Resistance (θ <sub>JC</sub> ) (Note 3)	
8-Pin μMAX (μSOP).....	42°C/W
8-Pin SO (SOP).....	40°C/W

Junction-to-Ambient Thermal Resistance (θ <sub>JA</sub> ) (Note 3)	
8-Pin μMAX (μSOP).....	221°C/W
8-Pin SO (SOP).....	170°C/W
ESD Protection	
Human Body Model (R <sub>D</sub> = 1.5kΩ, C <sub>S</sub> = 100pF)	
All Pins to GND.....	±2kV
Operating Temperature Range.....	-55°C to +125°C
Junction Temperature.....	+150°C
Storage Temperature Range.....	-65°C to +150°C
Lead Temperature (soldering, 10s).....	+300°C

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions.

**Note 2:** When the input voltage (V<sub>I</sub>) at any pin exceeds the Absolute Maximum Ratings limits (V<sub>I</sub> < GND, V<sub>I</sub> > 6V or V<sub>I</sub> > +V<sub>S</sub>), the current at that pin should be limited to 5mA. The 20mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 5mA to four.

**Note 3:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a single-layer board. For detailed information on package thermal considerations, refer to [www.maximintegrated.com/thermal-tutorial](http://www.maximintegrated.com/thermal-tutorial).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

### Electrical Characteristics

(+V<sub>S</sub> = +3.0V to +5.5V, unless otherwise noted. Temperature accuracy specifications apply for +V<sub>S</sub> = 3.3V for versions with "-3" in the suffix and for +V<sub>S</sub> = 5V for versions with "-5" in the suffix. T<sub>A</sub> = -55°C to +125°C, unless otherwise noted. Typical values are at +V<sub>S</sub> = +5V, T<sub>A</sub> = +25°C.) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Accuracy (Six-Sigma)		-25°C ≤ T <sub>A</sub> ≤ +100°C	-2.0		+2.0	°C
		-55°C ≤ T <sub>A</sub> ≤ +125°C	-3.0		+3.0	
Accuracy (Three-Sigma) (Note 6)		-25°C ≤ T <sub>A</sub> ≤ +100°C	-1.5		+1.5	°C
		-55°C ≤ T <sub>A</sub> ≤ +125°C	-2.0		+2.0	
Resolution				9		Bits
Temperature Conversion Time		(Note 7)		100	300	ms
Quiescent Supply Current		I <sup>2</sup> C inactive		0.25	0.5	mA
		Shutdown mode, +V <sub>S</sub> = 3V		4	μA	
		Shutdown mode, +V <sub>S</sub> = 5V		6		
+V <sub>S</sub> Supply Voltage Range			3.0		5.5	V
OS Output Saturation Voltage		I <sub>OUT</sub> = 4.0mA (Note 8)			0.8	V
OS Delay		(Note 9)	1		6	Conversions
OS Output Fall Time	t <sub>OF</sub>	C <sub>L</sub> = 400pF, I <sub>O</sub> = 3mA (Note 10)			250	ns
T <sub>OS</sub> Default Temperature		(Note 11)		80		°C
T <sub>HYST</sub> Default Temperature		(Note 11)		75		°C

## Electrical Characteristics (continued)

( $+V_S = +3.0V$  to  $+5.5V$ , unless otherwise noted. Temperature accuracy specifications apply for  $+V_S = 3.3V$  for versions with “-3” in the suffix and for  $+V_S = 5V$  for versions with “-5” in the suffix.  $T_A = -55^\circ C$  to  $+125^\circ C$ , unless otherwise noted. Typical values are at  $+V_S = +5V$ ,  $T_A = +25^\circ C$ .) (Notes 4, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>LOGIC (SDA, SCL, A0, A1, A2)</b>						
Input High Voltage	$V_{IH}$		$+V_S \times 0.7$		$+V_S + 0.5$	V
Input Low Voltage	$V_{IL}$		-0.3		$+V_S \times 0.3$	V
Input High Current	$I_{IH}$	$V_{IN} = 5V$		0.005	1.0	$\mu A$
Input Low Current	$I_{IL}$	$V_{IN} = 0V$	-1.0	-0.005		$\mu A$
Input Capacitance	$C_{IN}$	All digital inputs		20		pF
Output High Current		$V_{OH} = 5V$			10	$\mu A$
Output Low Voltage		$I_{OL} = 3mA$			0.4	V
<b>I<sup>2</sup>C-COMPATIBLE TIMING (Notes 12, 13)</b>						
(Clock) SCL Period	$t_{SCL}$	Bus timeout inactive	2.5			$\mu s$
Data In Setup Time to SCL High	$t_{SU:DAT}$	10% of SDA to 10% of SCL	100			ns
Data Out Stable After SCL Low	$t_{HD:DAT}$	10% of SCL to 10% of SDA	0			$\mu s$
Start Condition Setup Time (SDA Low to SCL Low)	$t_{SU:STA}$	90% of SCL to 90% of SDA	100			ns
STOP Condition Hold Time	$t_{HD:STO}$		100			ns
SDA Time Low for Reset of Serial Interface	$t_{TIMEOUT}$	(Note 14)	75		325	ms

**Note 4:** All parts operate properly over the 3V to 5.5V supply voltage range. The devices are tested and specified for rated accuracy at their nominal supply voltage.

**Note 5:** All parameters are measured at  $T_A = +25^\circ C$ . Values over the temperature range are guaranteed by design.

**Note 6:** There is no industry-wide standard for temperature accuracy specifications. Maxim's standard is six-sigma. The three-sigma specification is included to allow easier comparison to products built by manufacturers who use different standards.

**Note 7:** This specification indicates how often temperature data is updated. The devices can be read at any time without regard to conversion state, while yielding the last conversion result.

**Note 8:** For best accuracy, minimize output loading. Higher sink currents can affect sensor accuracy due to internal heating.

**Note 9:** OS delay is user programmable up to 6 over-limit conversions before OS is set to minimize false tripping in noisy environments.

**Note 10:** Guaranteed by design.

**Note 11:** Default values set at power-up.

**Note 12:** All timing specifications are guaranteed by design.

**Note 13:** Unless otherwise noted, these specifications apply for  $+V_S = +5VDC$  for LM75BIM-5 and LM75BIMM-5 and  $+V_S = +3.3VDC$  for LM75BIM-3 and LM75BIMM-3.  $C_L$  (load capacitance) on output lines = 80pF, unless otherwise specified.

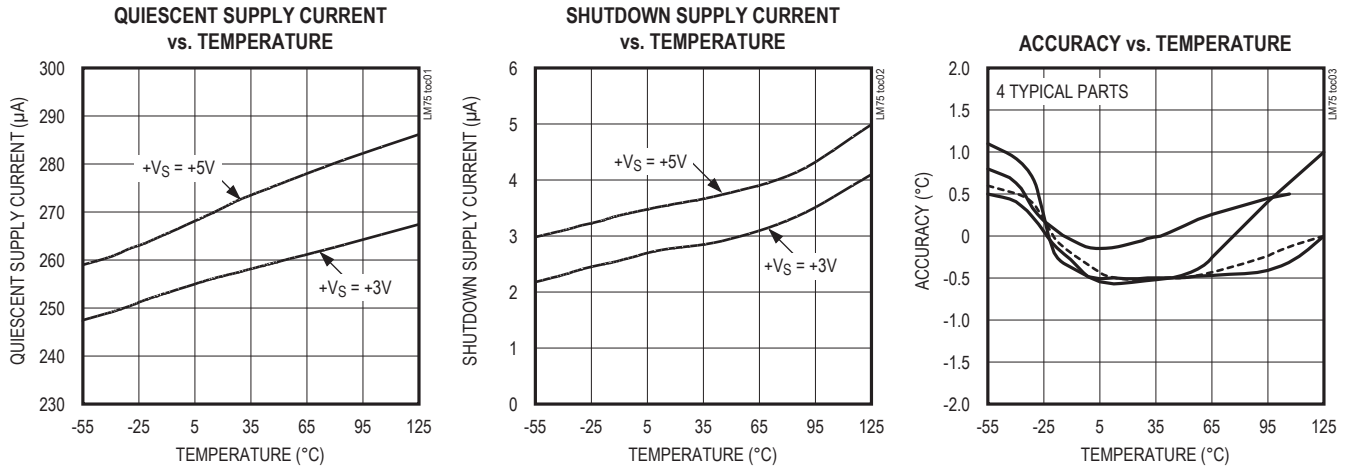
The switching characteristics of the LM75 fully meet or exceed the published specifications of the I<sup>2</sup>C bus.

These parameters are the timing relationships between SCL and SDA signals related to the LM75. They are not I<sup>2</sup>C bus specifications.

**Note 14:** Holding the SDA line low for a time greater than  $t_{TIMEOUT}$  causes the device to reset SDA to the IDLE state of the serial bus communication (SDA set high).

Typical Operating Characteristics

(T<sub>A</sub> = +25°C, unless otherwise noted.)



Pin Description

PIN	NAME	FUNCTION
1	SDA	Serial-Data Input/Output Line. Open drain. Connect SDA to a pullup resistor.
2	SCL	Serial Clock Input. Open drain. Connect SCL to a pullup resistor.
3	OS	Overtemperature Shutdown Output. Open drain. Connect OS to a pullup resistor.
4	GND	Ground
5	A2	2-Wire Interface Address Input. Connect A2 to GND or +V <sub>S</sub> to set the desired I <sup>2</sup> C bus address. Do not leave unconnected (see Table 1).
6	A1	2-Wire Interface Address Input. Connect A1 to GND or +V <sub>S</sub> to set the desired I <sup>2</sup> C bus address. Do not leave unconnected (see Table 1).
7	A0	2-Wire Interface Address Input. Connect A0 to GND or +V <sub>S</sub> to set the desired I <sup>2</sup> C bus address. Do not leave unconnected (see Table 1).
8	+V <sub>S</sub>	Positive Supply Voltage Input. Bypass to GND with a 0.1µF bypass capacitor.

Detailed Description

The LM75 temperature sensor measures temperature and converts the data into digital form using a bandgap type temperature sensor and a 9-bit delta-sigma ADC. An I<sup>2</sup>C-compatible 2-wire serial interface allows access to conversion results. The LM75 accepts standard I<sup>2</sup>C commands to read the data, set the overtemperature alarm (OS) trip thresholds, and configure other characteristics. While reading the Temperature register, any changes in temperature are ignored until the read is completed. The Temperature register is updated for the new temperature measurement upon completion of the read operation.

OS Output, T<sub>OS</sub>, and T<sub>HYST</sub> Limits

In comparator mode (see Figure 1), the open-drain OS output asserts when the temperature rises above the limit programmed into the T<sub>OS</sub> register, and becomes high impedance when the temperature falls below the limit set in the T<sub>HYST</sub> register. In this mode the LM75 operates as a thermostat, and the OS output can be used to take action to reduce the temperature (e.g., turn on a cooling fan, reduce clock speed, or shut down the system).

In interrupt mode, exceeding T<sub>OS</sub> also asserts OS. OS remains asserted until a read operation is performed on any of the registers. Once OS has asserted due to crossing above T<sub>OS</sub> and is then reset, it is asserted again only when the temperature drops below T<sub>HYST</sub>. The output then remains asserted until it is reset by a read. It is then asserted again if the temperature rises above T<sub>OS</sub>, and so on. Putting the LM75 into shutdown mode also resets OS.

Power-Up and Power-Down

The LM75 powers up to a known state, as indicated in Table 2. Some of these settings are summarized as following:

- Comparator mode
- T<sub>OS</sub> = +80°C
- T<sub>HYST</sub> = +75°C
- OS active low
- Command byte pointer = 0x00

I<sup>2</sup>C-Compatible Bus Interface

From a software perspective, the LM75 appears as a set of byte-wide registers that contain temperature data, alarm threshold values, and control bits. A standard I<sup>2</sup>C-compatible, 2-wire serial interface reads temperature data and writes control bits and alarm threshold data. Each device responds to its own I<sup>2</sup>C slave address, which is selected using A0, A1, and A2. See Table 1.

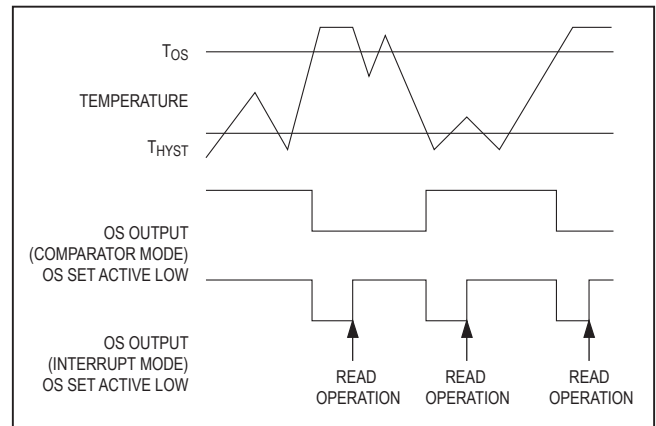


Figure 1. OS Output Temperature Response Diagram

Table 1. Slave Address

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	0	0	1	A2	A1	A0	R/W

Table 2. Register Functions

REGISTER NAME	ADDRESS (hex)	POR STATE (hex)	POR STATE (binary)	POR STATE (°C)	READ/ WRITE
Temperature	00	000X	0000 0000 0XXX XXXX	—	Read only
Configuration	01	00	0000 0000	—	R/W
T <sub>HYST</sub>	02	4B0X	0100 1011 0XXX XXXX	75	R/W
T <sub>OS</sub>	03	500X	0101 0000 0XXX XXXX	80	R/W

X = Don't care.

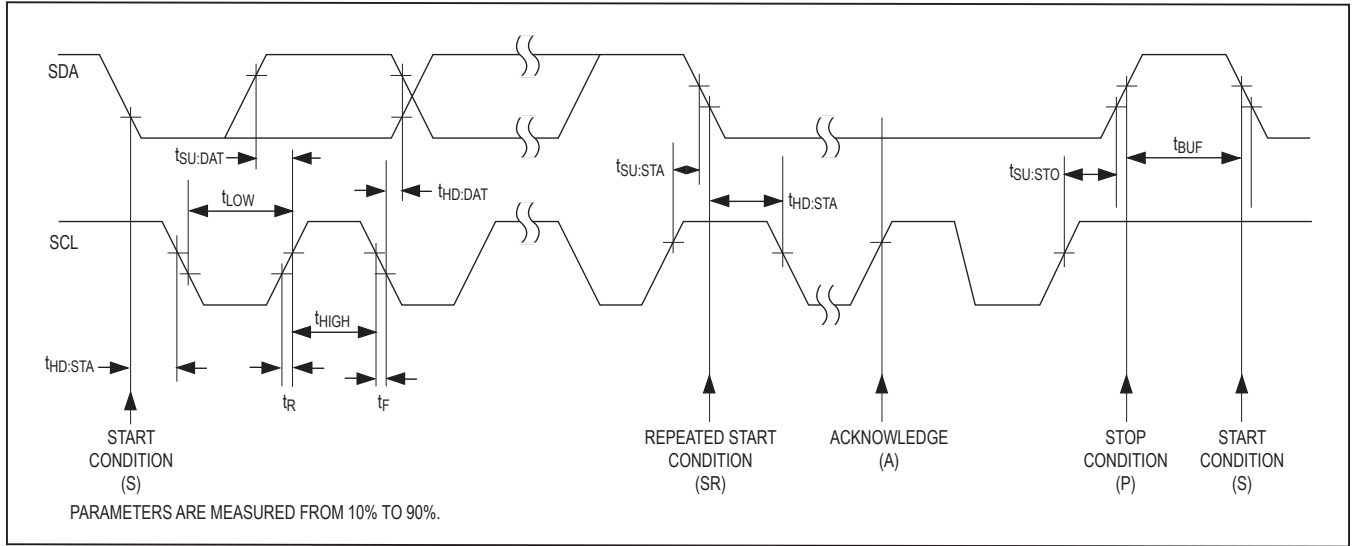


Figure 2. Serial Bus Timing

Table 3. Temperature, THYST, and TOS Register Definition

UPPER BYTE								LOWER BYTE							
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Sign bit 1 = Negative 0 = Positive	MSB 64°C	32°C	16°C	8°C	4°C	2°C	1°C	LSB 0.5°C	X	X	X	X	X	X	X

X = Don't care.

Table 4. Temperature Data Output Format

TEMPERATURE (°C)	DIGITAL OUTPUT	
	BINARY	HEX
+125	0111 1101 0XXX XXXX	7D0X
+25	0001 1001 0XXX XXXX	190X
+0.5	0000 0000 1XXX XXXX	008X
0	0000 0000 0XXX XXXX	000X
-0.5	1111 1111 1XXX XXXX	FF8X
-25	1110 0111 0XXX XXXX	E70X
-55	1100 1001 0XXX XXXX	C90X

X = Don't care.

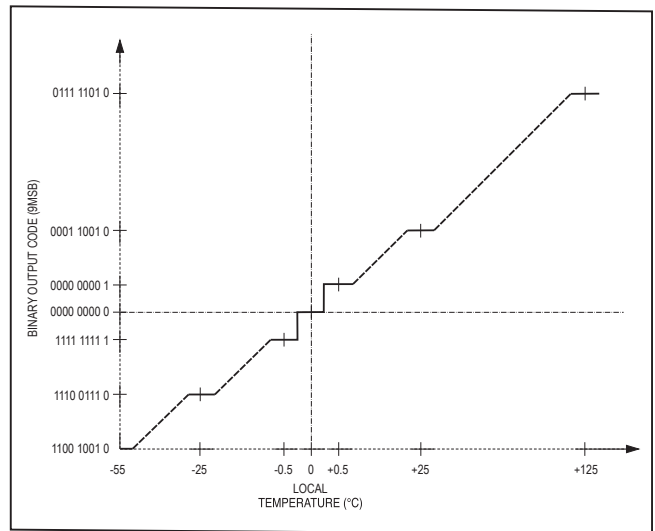


Figure 3. Temperature-to-Digital Transfer Function

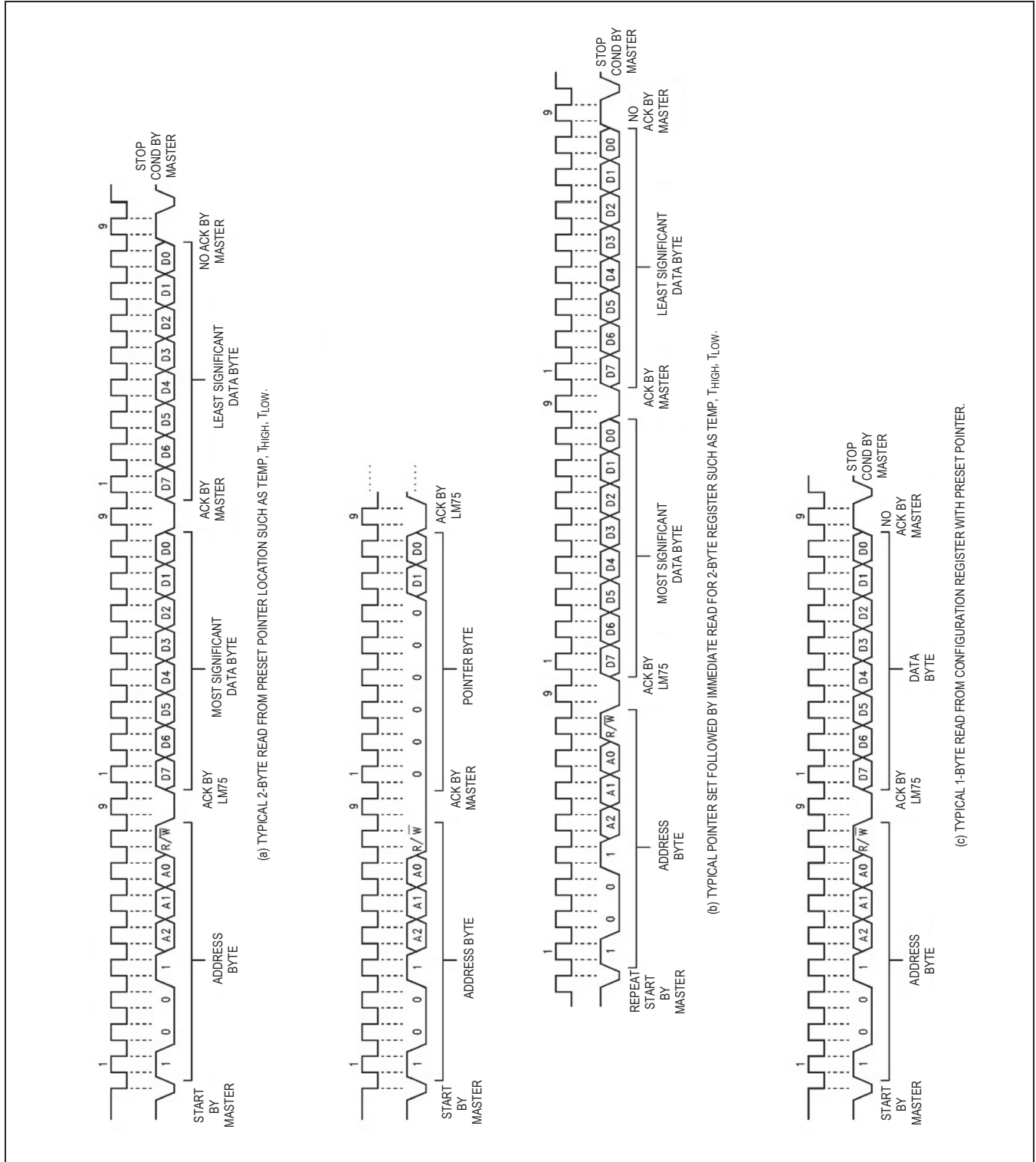


Figure 4. I<sup>2</sup>C-Compatible Timing Diagram (Read)

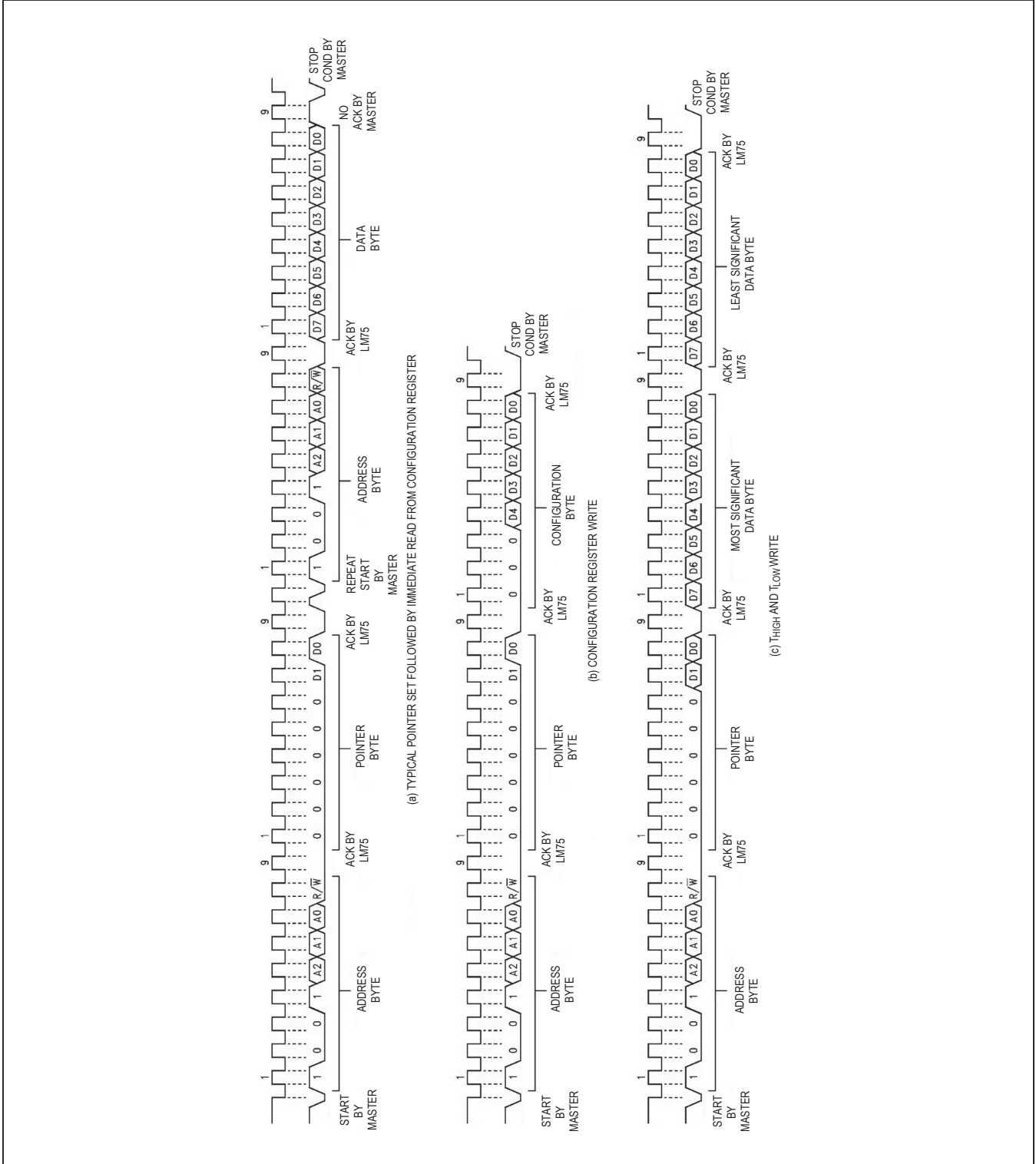


Figure 5. I<sup>2</sup>C-Compatible Timing Diagram (Write)



### Temperature Data Format

Temperature data is stored in the Temperature,  $T_{OS}$  Set Point, and  $T_{HYST}$  Set Point registers. The temperature data format is 9 bits, two's complement, and the register is read out in 2 bytes: an upper byte and a lower byte. Bits D15–D7 contain the temperature data, with the LSB representing  $0.5^{\circ}\text{C}$  and the MSB representing the sign bit (see Table 3). The MSB is transmitted first. The last 7 bits of the lower byte, bits D6–D0, are don't cares.

### Shutdown

Set bit D0 in the Configuration register to 1 to place the LM75 in shutdown mode and reduce supply current to  $4\mu\text{A}$ . In interrupt mode, entering shutdown resets the OS output. While in shutdown, the I<sup>2</sup>C remains active and  $T_{OS}$  and  $T_{HYST}$  limit registers along with the Configuration register remain accessible to the master.

### Fault Queue

The fault queue prevents OS false tripping in noisy environments. The number of faults set in the queue (up to 6) must occur to trip the OS output.

### Comparator/Interrupt Mode

The events that trigger OS are identical between comparator and interrupt modes. In comparator mode, OS is asserted when the temperature rises above the  $T_{OS}$  value. OS is deasserted when the temperature drops below the  $T_{HYST}$  value. In interrupt mode, OS is asserted when the temperature rises above the  $T_{OS}$  value or falls below the  $T_{HYST}$  value. OS is deasserted only after performing a read operation.

### OS Output

The OS output is an open-drain output without an internal pullup. Connect a pullup resistor from OS to  $+V_S$ . Using larger resistance values reduces any temperature errors due to self heating from current entering OS.

### OS Polarity

The OS polarity can be programmed for active-low or active-high operation. In active-low operation, OS goes low when triggered by a temperature event.

### Internal Registers

The LM75's Pointer register selects between four data registers (see Figure 6). At power-up, the pointer is set to read the Temperature register at address 0x00. The Pointer register latches the last location to which it was set. All registers are read and write, except the Temperature register, which is read only.

Write to the Configuration register by writing an address byte, a data pointer byte, and a data byte. If 2 data bytes are written, the second data byte overrides the first. The  $T_{OS}$  and  $T_{HYST}$  registers require 1 address byte, 1 pointer byte, and 2 data bytes. If only 1 data byte is written, it is saved in bits D15–D8 of the respective register. If more than 2 data bytes are written, only the first 2 bytes are recognized while the remaining bytes are ignored.

Read from the LM75 in one of two ways. If the location latched in the Pointer register is set from the previous read, the new read consists of an address byte, followed by retrieving the corresponding number of data bytes. If the Pointer register needs to be set to a new address, perform a read operation by writing an address byte, pointer byte, repeat start, and another address byte.

An inadvertent 8-bit read from a 16-bit register, with the D7 bit low, can cause the device to stop in a state where the SDA line is held low. Ordinarily, this would prevent any further bus communication until the master sends nine additional clock cycles or SDA goes high. At that time, a stop condition resets the device. If the additional clock cycles are not generated by the master, the LM75 bus resets and unlocks after the bus timeout period has elapsed.

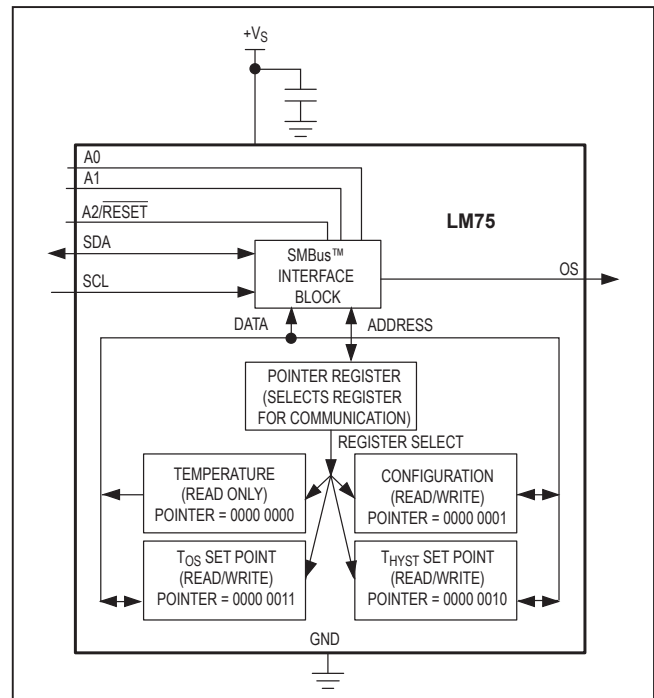


Figure 6. Block Diagram

SMBus is a trademark of Intel Corp.

**Table 5. Configuration Register Definition**

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	Fault Queue	Fault Queue	OS Polarity	Comparator/ Interrupt	Shutdown

### Configuration Register

The 8-bit Configuration register sets the fault queue, OS polarity, shutdown control, and whether the OS output functions in comparator or interrupt mode. When writing to the Configuration register, set bits D7, D6, and D5 to zero (see Table 5).

Bits D4 and D3, the fault queue bits, determine the number of faults necessary to trigger an OS condition (see Table 6). The number of faults set in the queue must occur consecutively to trip the OS output. The fault queue prevents OS false tripping in noisy environments.

Set bit D2, the OS polarity bit, to zero to force the OS output polarity to active low. Set bit D2 to 1 to set the OS output polarity to active high. OS is an open-drain output under all conditions and requires a pullup resistor to output a high voltage (see Figure 1).

Set bit D1, the comparator/interrupt bit to zero to operate OS in comparator mode. In comparator mode, OS is asserted when the temperature rises above the  $T_{OS}$  value. OS is deasserted when the temperature drops below the  $T_{HYST}$  value (see Figure 1). Set bit D1 to 1 to operate OS in interrupt mode. OS is asserted in interrupt mode when the temperature rises above the  $T_{OS}$  value or falls below the  $T_{HYST}$  value. OS is deasserted only after performing a read operation.

Set bit D0, the shutdown bit, to zero for normal operation. Set bit D0 to 1 to shutdown the LM75's internal blocks. The I<sup>2</sup>C interface remains active as long as the shutdown bit is set. The  $T_{OS}$ ,  $T_{HYST}$ , and Configuration registers can still be written to and read from while in shutdown.

### Applications Information

LM75 measures the temperature of its own die. The thermal path between the die and the outside world determines the accuracy of temperature measurements. Most of the heat flows in to or out of the die through the leads.

**Table 6. Configuration Register Fault Queue Bits**

D4	D3	NUMBER OF FAULTS
0	0	1 (POR state)
0	1	2
1	0	4
1	1	6

Because of this, the LM75 most easily measures the PCB temperature. For ambient temperature measurements, mount the LM75 on a separate PCB away from high power sources. Temperature errors due to self heating of the LM75 die is minimal due to the low supply current.

### Digital Noise Issues

The lowpass filters in the SCL and SDA digital lines mitigate the effects of bus noise, and make communications in noisy environments more robust. Good layout practices also help. Keep switching power supplies away from digital lines, and arrange for high-speed digital traces to cross SCL and SDA at right angles. Properly terminate long PCB traces and bus traces connected to multiple slaves.

Serial bus no-acknowledge (which causes unnecessary bus traffic) is the most common symptom of excessive noise coupling into the SDA and SCL lines. Noise with amplitude greater than the LM75's hysteresis (400mV<sub>P-P</sub>, typ), overshoot greater than 300mV above +V<sub>S</sub>, and undershoot more than 300mV below GND may prevent successful serial communication.

Resistance can be added in series with the SDA and SCL lines to help filter noise and ringing. A 5kΩ resistor placed in series with the SCL line and as close as possible to the SCL pin, with the 5pF to 10pF stray capacitance of the device, provides a 6MHz to 12MHz lowpass filter, which is sufficient filtering in many cases.

# LM75

## Digital Temperature Sensor and Thermal Watchdog with 2-Wire Interface

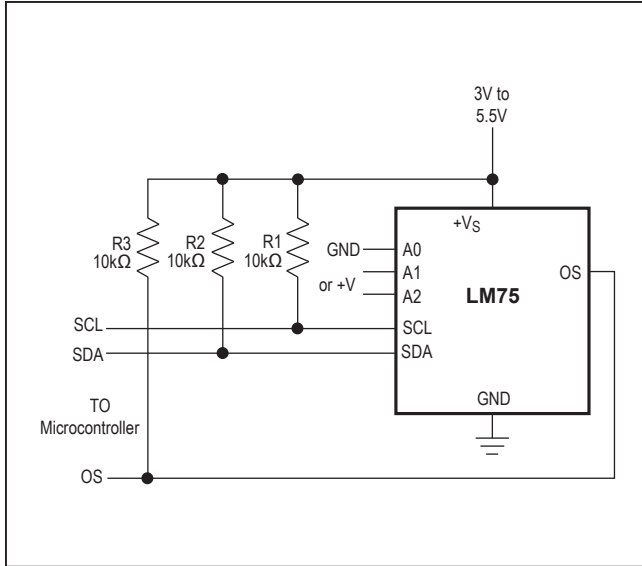


Figure 7. I<sup>2</sup>C Controlled Temperature Sensor

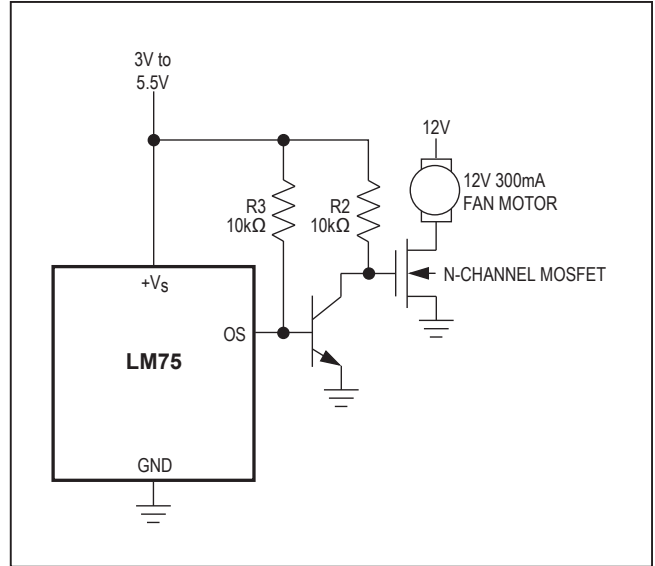


Figure 8. Fan Control

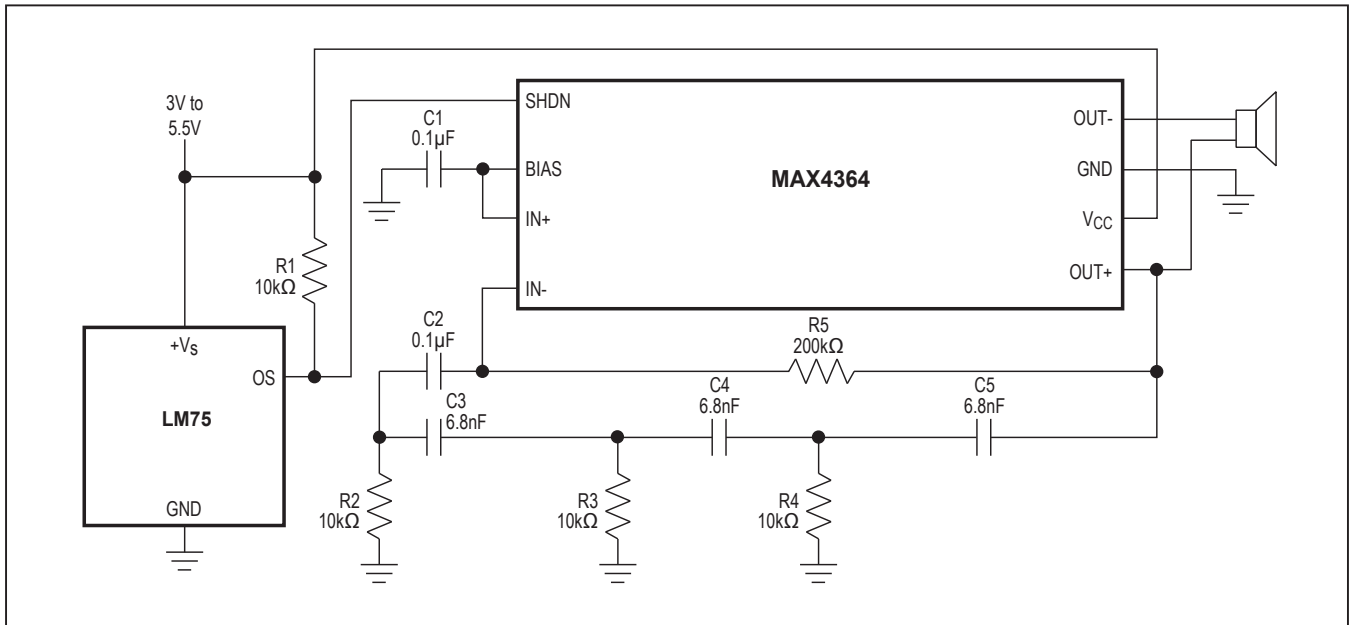


Figure 9. Temperature Sensor with Audible Alarm

**Chip Information**

PROCESS: CMOS

**Package Information**

For the latest package outline information and land patterns (footprints), go to [www.maximintegrated.com/packages](http://www.maximintegrated.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 SO (SOP)	S8-2	<a href="#">21-0041</a>
8 $\mu$ MAX ( $\mu$ SOP)	U8-1	<a href="#">21-0036</a>

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/09	Initial release	—
1	11/21	Updated <i>Ordering Information</i> table	1
2	11/21	Updated <i>Ordering Information</i> table	1
3	02/24	Updated <i>Ordering Information</i> table	1

