MC34025, MC33025

High Speed Double-Ended PWM Controller

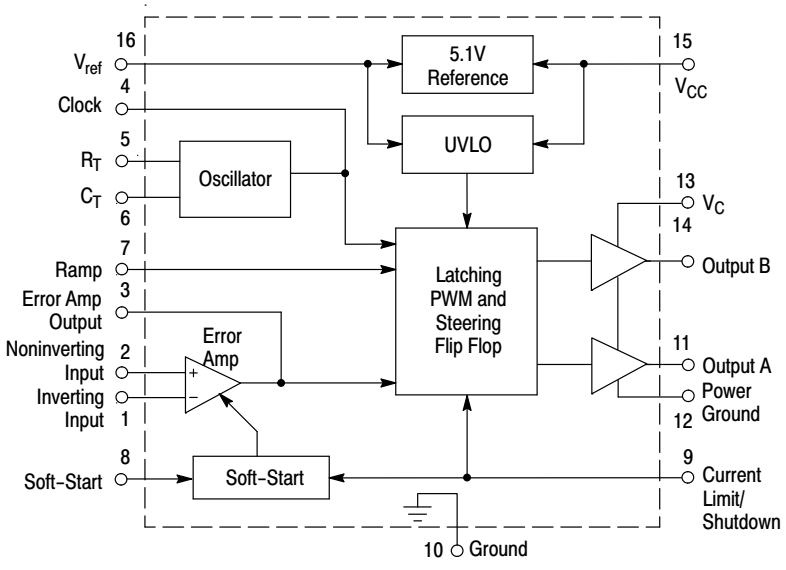
The MC34025 series are high speed, fixed frequency, double−ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off−Line and DC−to−DC converter applications offering the designer a cost effective solution with minimal external components. These integrated circuits feature an oscillator, a temperature compensated reference, a wide bandwidth error amplifier, a high speed current sensing comparator, steering flip−flop, and dual high current totem pole outputs ideally suited for driving power MOSFETs.

Also included are protective features consisting of input and reference undervoltage lockouts each with hysteresis, cycle−by−cycle current limiting, and a latch for single pulse metering.

The flexibility of this series allows it to be easily configured for either current mode or voltage mode control.

Features

- 50 ns Propagation Delay to Outputs
- Dual High Current Totem Pole Outputs
- Wide Bandwidth Error Amplifier
- Fully−Latched Logic with Double Pulse Suppression
- Latching PWM for Cycle−By−Cycle Current Limiting
- Soft−Start Control with Latched Overcurrent Reset
- Input Undervoltage Lockout with Hysteresis
- Low Startup Current (500 μA Typ)
- Internally Trimmed Reference with Undervoltage Lockout
- 45% Maximum Duty Cycle (Externally Adjustable)
- Precision Trimmed Oscillator
- Voltage or Current Mode Operation to 1.0 MHz
- Functionally Similar to the UC3825
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant



This device contains 227 active transistors.

Figure 1. Simplified Application

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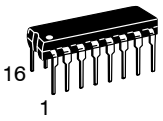
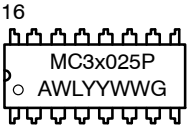
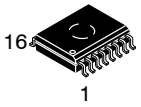
MARKING DIAGRAMS

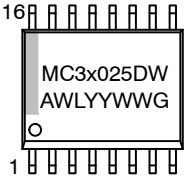


PDIP−16
P SUFFIX
CASE 648



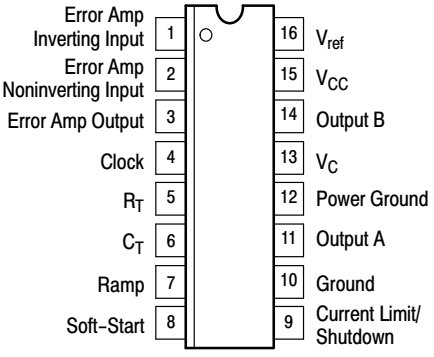


SO−16WB
DW SUFFIX
CASE 751G



x	= 3 or 4
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 18 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	30	V
Output Driver Supply Voltage	V_C	25	V
Output Current, Source or Sink (Note 1) DC Pulsed (0.5 μs)	I_O	 0.5 2.0	A
Current Sense, Soft−Start, Ramp, and Error Amp Inputs	V_{in}	−0.3 to +7.0	V
Error Amp Output and Soft−Start Sink Current	I_O	10	mA
Clock and R_T Output Current	I_{CO}	5.0	mA
Power Dissipation and Thermal Characteristics SO−16 Package (Case 751G) Maximum Power Dissipation @ T_A = +25°C Thermal Resistance, Junction−to−Air DIP Package (Case 648) Maximum Power Dissipation @ T_A = +25°C Thermal Resistance, Junction−to−Air	 P_D $R_{\theta JA}$ P_D $R_{\theta JA}$	 862 145 1.25 100	 mW °C/W W °C/W
Operating Junction Temperature	T_J	+150	°C
Operating Ambient Temperature (Note 2) MC34025 MC33025	T_A	 0 to +70 −40 to +105	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Human Body Model ESD Capability per JEDEC − JESD22−A114F	HBM	2000	V
Machine Model ESD Capability per JEDEC − JESD22−A115C	MM	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 2], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
REFERENCE SECTION					
Reference Output Voltage (I_O = 1.0 mA, T_J = +25°C)	V_{ref}	5.05	5.1	5.15	V
Line Regulation (V_{CC} = 10 V to 30 V)	Reg_{line}	−	2.0	15	mV
Load Regulation (I_O = 1.0 mA to 10 mA)	Reg_{load}	−	2.0	15	mV
Temperature Stability	T_S	−	0.2	−	mV/°C
Total Output Variation over Line, Load, and Temperature	V_{ref}	4.95	−	5.25	V
Output Noise Voltage (f = 10 Hz to 10 kHz, T_J = +25°C)	V_n	−	50	−	μV
Long Term Stability (T_A = +125°C for 1000 Hours)	S	−	5.0	−	mV
Output Short Circuit Current	I_{SC}	−30	−65	−100	mA
OSCILLATOR SECTION					
Frequency T_J = +25°C Line (V_{CC} = 10 V to 30 V) and Temperature (T_A = T_{low} to T_{high})	f_{osc}	380 370	400 400	420 430	kHz
Frequency Change with Voltage (V_{CC} = 10 V to 30 V)	$\Delta f_{osc}/\Delta V$	−	0.2	1.0	%
Frequency Change with Temperature (T_A = T_{low} to T_{high})	$\Delta f_{osc}/\Delta T$	−	2.0	−	%
Sawtooth Peak Voltage	V_P	2.6	2.8	3.0	V
Sawtooth Valley Voltage	V_V	0.7	1.0	1.25	V
Clock Output Voltage High State Low State	V_{OH} V_{OL}	3.9 −	4.5 2.3	− 2.9	V

1. Maximum package power dissipation limits must be observed.
2. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for MC34025 T_{high} = +70°C for MC34025
   = − 40°C for MC33025 = +105°C for MC33025

ELECTRICAL CHARACTERISTICS (V_{CC} = 15 V, R_T = 3.65 kΩ, C_T = 1.0 nF, for typical values T_A = +25°C, for min/max values T_A is the operating ambient temperature range that applies [Note 4], unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER SECTION					
Input Offset Voltage	V_{IO}	–	–	15	mV
Input Bias Current	I_{IB}	–	0.6	3.0	μA
Input Offset Current	I_{IO}	–	0.1	1.0	μA
Open−Loop Voltage Gain (V_O = 1.0 V to 4.0 V)	A_{VOL}	60	95	–	dB
Gain Bandwidth Product (T_J = +25°C)	GBW	4.0	8.3	–	MHz
Common Mode Rejection Ratio (V_{CM} = 1.5 V to 5.5 V)	CMRR	75	95	–	dB
Power Supply Rejection Ratio (V_{CC} = 10 V to 30 V)	PSRR	85	110	–	dB
Output Current, Source (V_O = 4.0 V) Sink (V_O = 1.0 V)	I_{Source} I_{Sink}	0.5 1.0	3.0 3.6	– –	mA
Output Voltage Swing, High State (I_O = – 0.5 mA) Low State (I_O = 1.0 mA)	V_{OH} V_{OL}	4.5 0	4.75 0.4	5.0 1.0	V
Slew Rate	SR	6.0	12	–	V/μs
PWM COMPARATOR SECTION					
Ramp Input Bias Current	I_{IB}	–	−0.5	−5.0	μA
Duty Cycle of Each Output, Maximum Minimum	$DC_{(max)}$ $DC_{(min)}$	40 –	45 –	– 0	%
Zero Duty Cycle Threshold Voltage Pin 3(4) (Pin 7(9) = 0 V)	V_{th}	1.1	1.25	1.4	V
Propagation Delay (Ramp Input to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	60	100	ns
SOFT−START SECTION					
Charge Current ($V_{Soft-Start}$ = 0.5 V)	I_{chg}	3.0	9.0	20	μA
Discharge Current ($V_{Soft-Start}$ = 1.5 V)	I_{dischg}	1.0	4.0	–	mA
CURRENT SENSE SECTION					
Input Bias Current (Pin 9(12) = 0 V to 4.0 V)	I_{IB}	–	–	15	μA
Current Limit Comparator Threshold Shutdown Comparator Threshold	V_{th} V_{th}	0.9 1.25	1.0 1.40	1.10 1.55	V
Propagation Delay (Current Limit/Shutdown to Output, T_J = +25°C)	$t_{PLH(in/out)}$	–	50	80	ns
OUTPUT SECTION					
Output Voltage Low State (I_{Sink} = 20 mA) (I_{Sink} = 200 mA) High State (I_{Source} = 20 mA) (I_{Source} = 200 mA)	 V_{OL} V_{OH} 	 – – 13 12	 0.25 1.2 13.5 13	 0.4 2.2 – –	V
Output Voltage with UVLO Activated (V_{CC} = 6.0 V, I_{Sink} = 0.5 mA)	$V_{OL(UVLO)}$	–	0.25	1.0	V
Output Leakage Current (V_C = 20 V)	I_L	–	100	500	μA
Output Voltage Rise Time (C_L = 1.0 nF, T_J = +25°C)	t_r	–	30	60	ns
Output Voltage Fall Time (C_L = 1.0 nF, T_J = +25°C)	t_f	–	30	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Startup Threshold (V_{CC} Increasing)	$V_{th(on)}$	8.8	9.2	9.6	V
UVLO Hysteresis Voltage (V_{CC} Decreasing After Turn−On)	V_H	0.4	0.8	1.2	V
TOTAL DEVICE					
Power Supply Current Startup (V_{CC} = 8.0 V) Operating	I_{CC}	 – –	 0.5 25	 1.2 35	mA

3. Maximum package power dissipation limits must be observed.
4. Low duty cycle pulse techniques are used during test to maintain junction temperature as close to ambient as possible.
   T_{low} = 0°C for MC34025 T_{high} = +70°C for MC34025
   = – 40°C for MC33025 = +105°C for MC33025

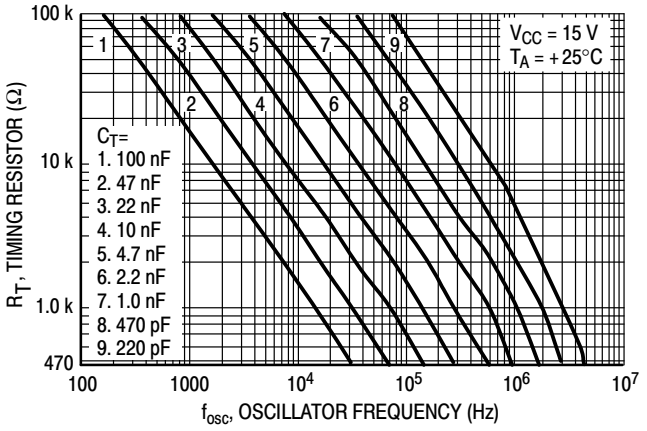


Figure 2. Timing Resistor versus Oscillator Frequency

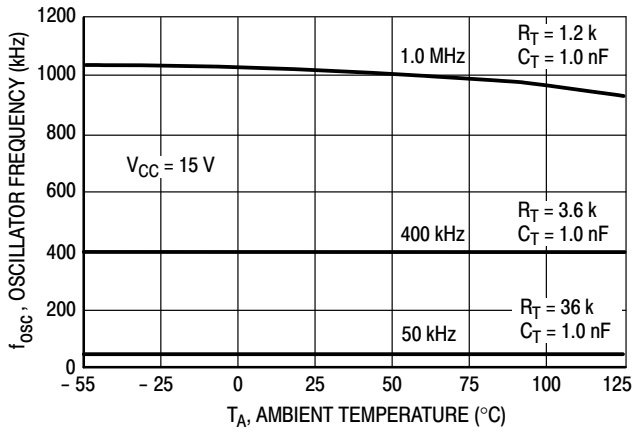


Figure 3. Oscillator Frequency versus Temperature

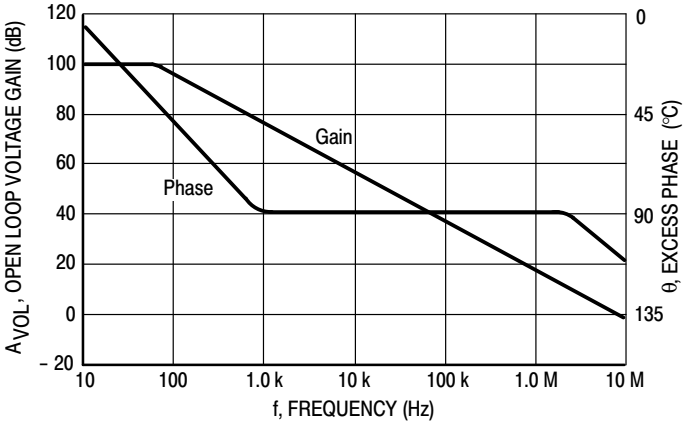


Figure 4. Error Amp Open Loop Gain and Phase versus Frequency

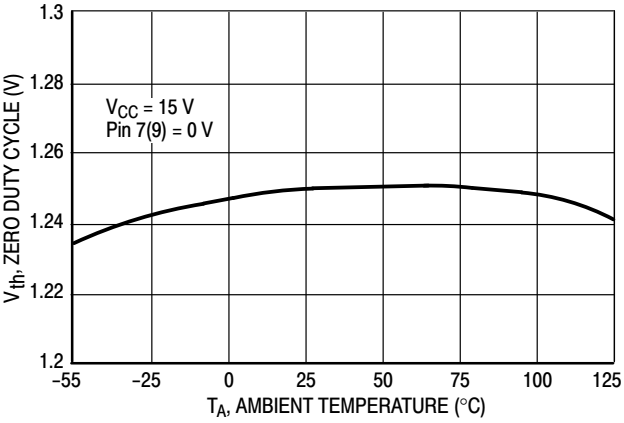


Figure 5. PWM Comparator Zero Duty Cycle Threshold Voltage versus Temperature

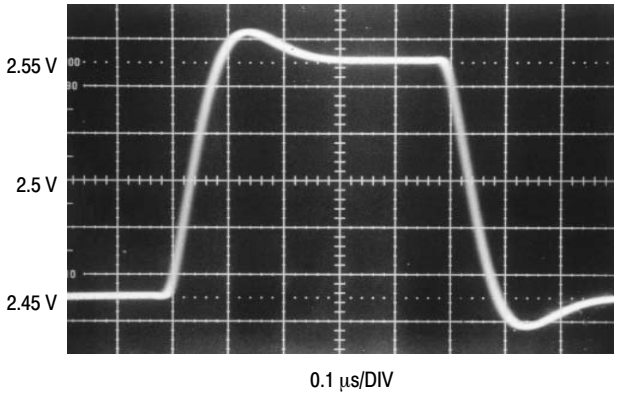


Figure 6. Error Amp Small Signal Transient Response

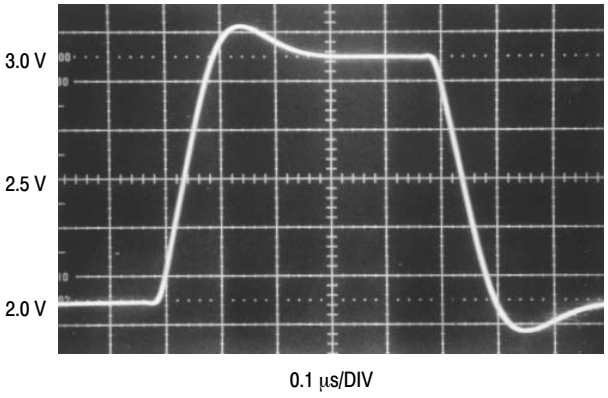


Figure 7. Error Amp Large Signal Transient Response

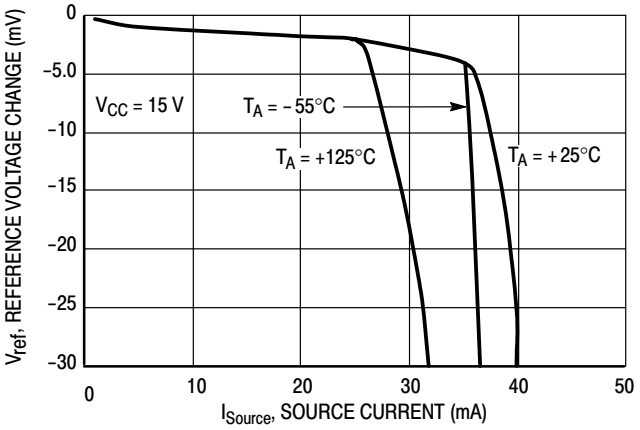


Figure 8. Reference Voltage Change versus Source Current

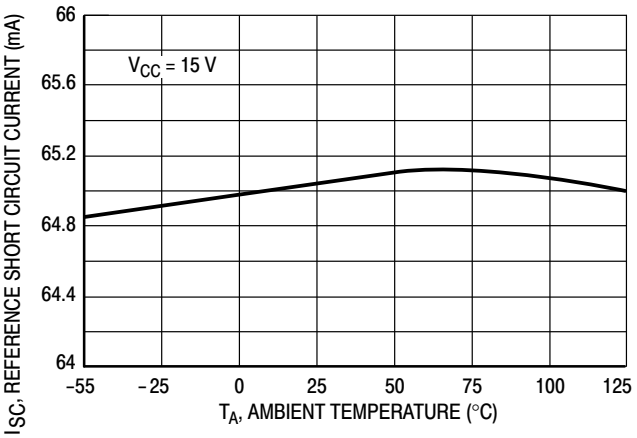


Figure 9. Reference Short Circuit Current versus Temperature

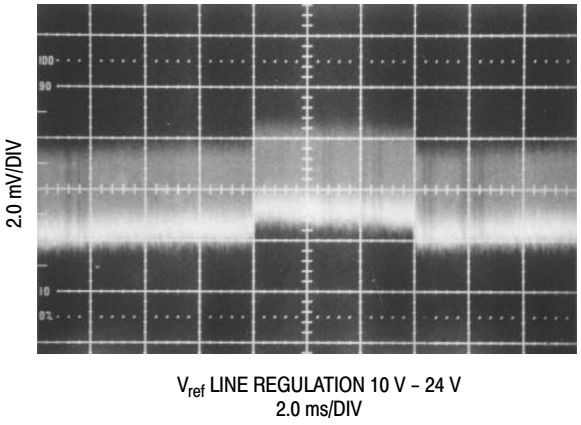


Figure 10. Reference Line Regulation

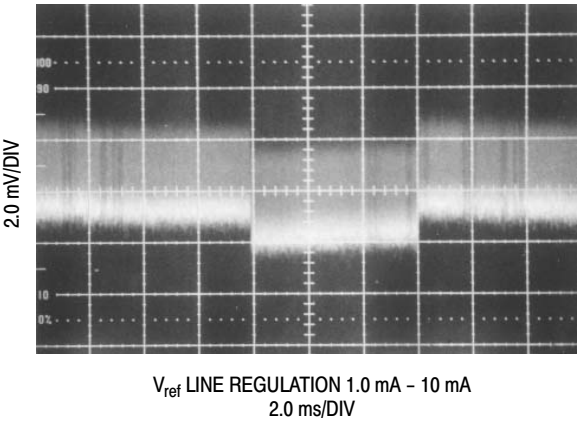


Figure 11. Reference Load Regulation

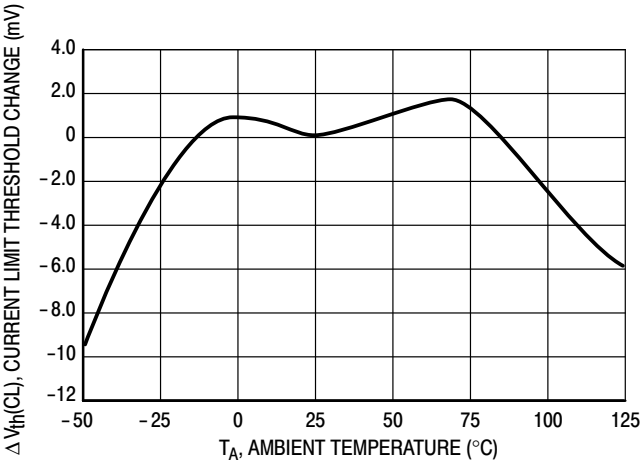


Figure 12. Current Limit Comparator Threshold Change versus Temperature

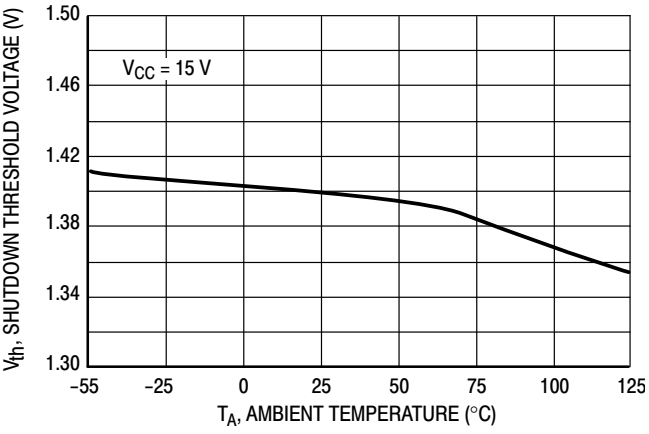


Figure 13. Shutdown Comparator Threshold Voltage versus Temperature

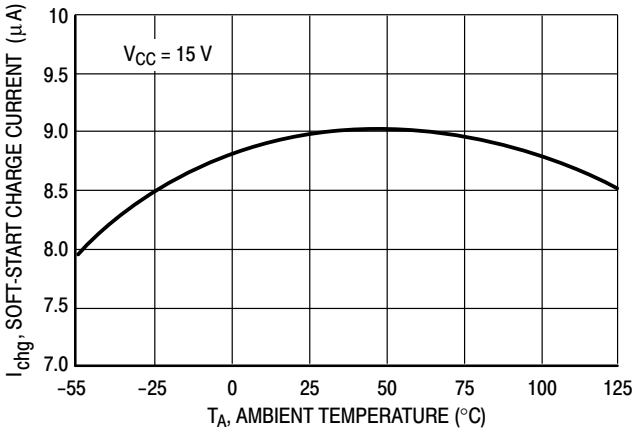


Figure 14. Soft−Start Charge Current versus Temperature

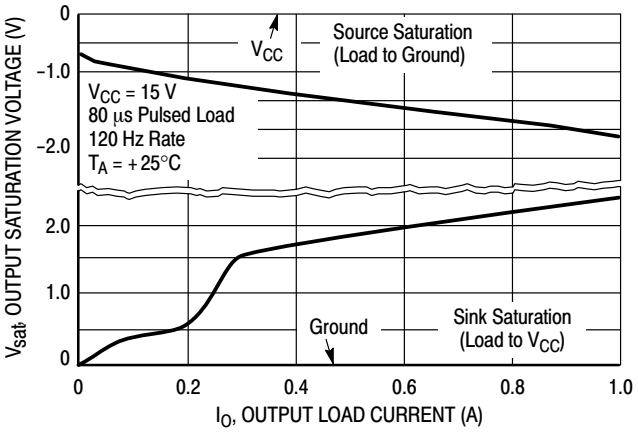
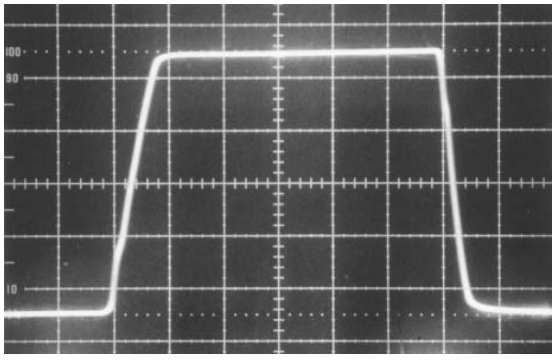
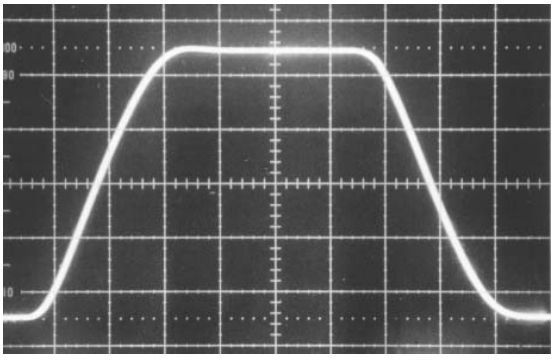


Figure 15. Output Saturation Voltage versus Load Current



OUTPUT RISE & FALL TIME 1.0 nF LOAD
50 ns/DIV

Figure 16. Drive Output Rise and Fall Time



OUTPUT RISE & FALL TIME 10.0 nF LOAD
50 ns/DIV

Figure 17. Drive Output Rise and Fall Time

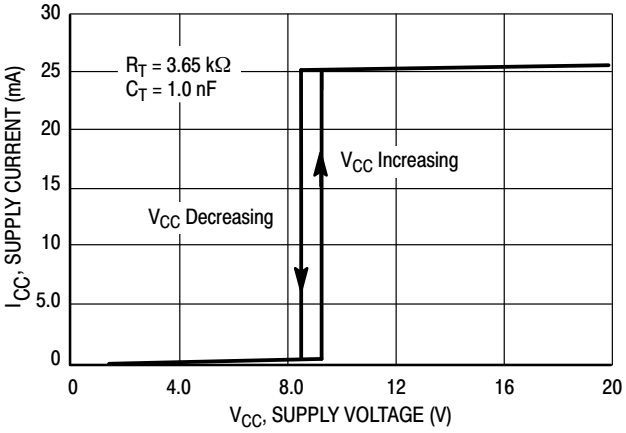


Figure 18. Supply Voltage versus Supply Current

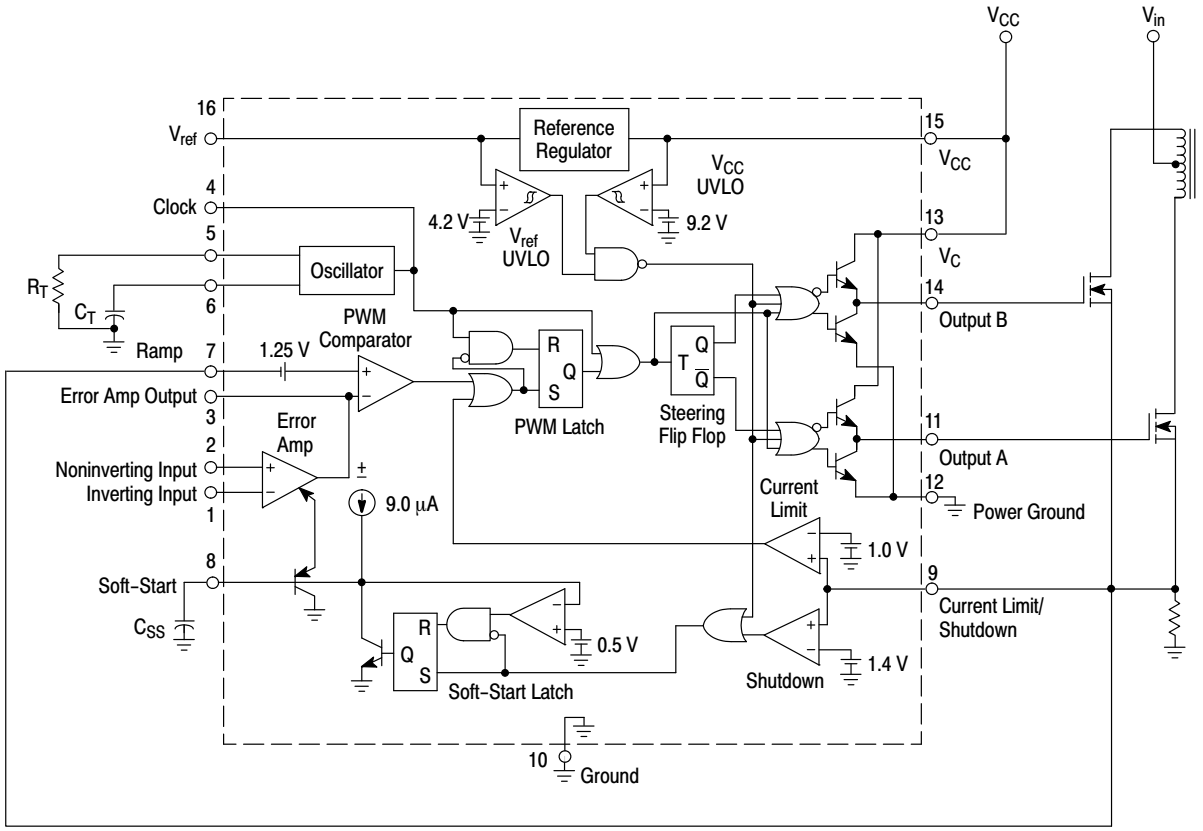


Figure 19. Representative Block Diagram

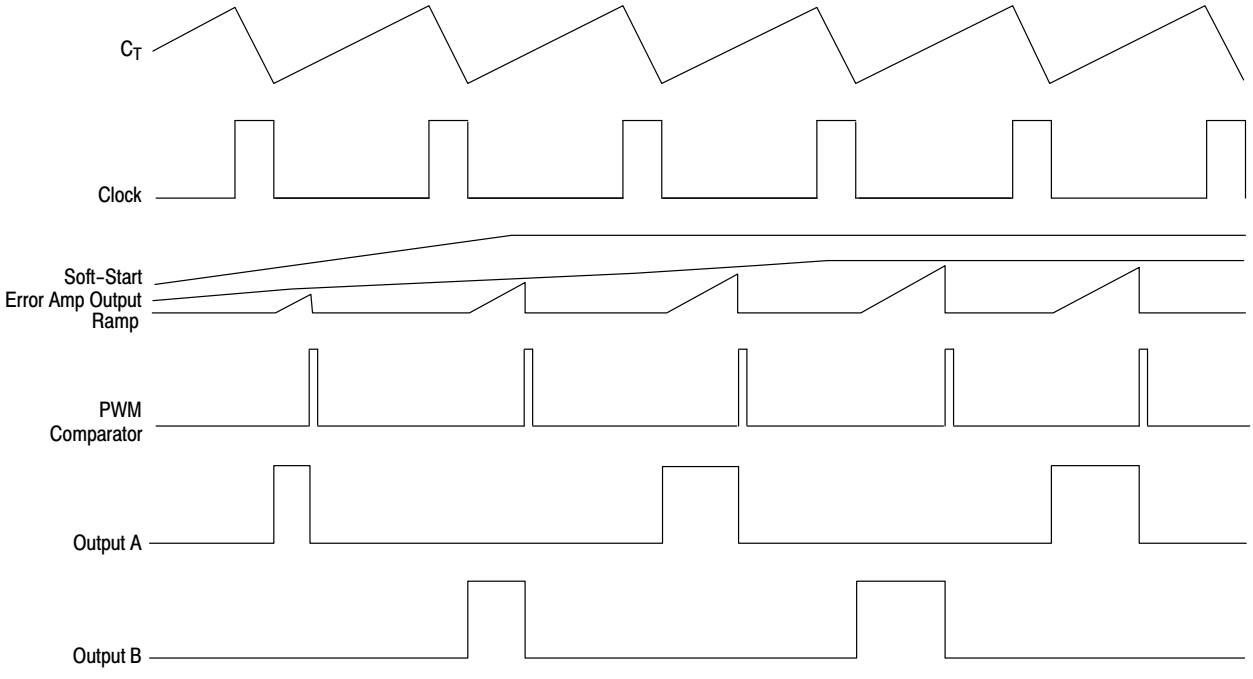


Figure 20. Current Limit Operating Waveforms

OPERATING DESCRIPTION

The MC33025 and MC34025 series are high speed, fixed frequency, double−ended pulse width modulator controllers optimized for high frequency operation. They are specifically designed for Off−Line and DC−to−DC converter applications offering the designer a cost effective solution with minimal external components. A representative block diagram is shown in Figure 19.

Oscillator

The oscillator frequency is programmed by the values selected for the timing components R_T and C_T. The R_T pin is set to a temperature compensated 3.0 V. By selecting the value of R_T, the charge current is set through a current mirror for the timing capacitor C_T. This charge current runs continuously through C_T. The discharge current ratio is to be 10 times the charge current, which yields the maximum duty cycle of 90%. C_T is charged to 2.8 V and discharged to 1.0 V. During the discharge of C_T, the oscillator generates an internal blanking pulse that resets the PWM Latch, inhibits the outputs, and toggles the steering flip−flop. The threshold voltages on the oscillator comparator is trimmed to guarantee an oscillator accuracy of 5.0% at 25°C.

Additional dead time can be added by externally increasing the charge current to C_T as shown in Figure 24. This changes the charge to discharge ratio of C_T which is set internally to $I_{charge}/10$ I_{charge}. The new charge to discharge ratio will be:

$$\% \text{ Deadtime} = \frac{I_{additional} + I_{charge}}{10\ (I_{charge})}$$

A bidirectional clock pin is provided for synchronization or for master/slave operation. As a master, the clock pin provides a positive output pulse during the discharge of C_T. As a slave, the clock pin is an input that resets the PWM latch and blanks the drive output, but does not discharge C_T. Therefore, the oscillator is not synchronized by driving the clock pin alone. Figures 30 and 31 provide suggested synchronization.

Error Amplifier

A fully compensated Error Amplifier is provided. It features a typical DC voltage gain of 95 dB and a gain bandwidth product of 8.3 MHz with 75 degrees of phase margin (Figure 4). Typical application circuits will have the noninverting input tied to the reference. The inverting input will typically be connected to a feedback voltage generated from the output of the switching power supply. Both inputs have a Common Mode Voltage (V_{CM}) input range of 1.5 V to 5.5 V. The Error Amplifier Output is provided for external loop compensation.

Soft−Start Latch

Soft−Start is accomplished in conjunction with an external capacitor. The soft start capacitor is charged by an internal 9.0 μA current source. This capacitor clamps the output of the error amplifier to less than its normal output voltage, thus limiting the duty cycle.

The time it takes for a capacitor to reach full charge is given by:

$$t \approx (4.5 \bullet 10^5)\ C_{Soft\text{-}Start}$$

A Soft−Start latch is incorporated to prevent erratic operation of this circuitry. Two conditions can cause the Soft−Start circuit to latch so that the Soft−Start capacitor stays discharged. The first condition is activation of an undervoltage lockout of either V_{CC} or V_{ref}. The second condition is when current sense input exceeds 1.4 V. Since this latch is “set dominant”, it cannot be reset until either of these signals is removed, and the voltage at $C_{Soft−Start}$ is less than 0.5 V.

PWM Comparator and Latch

A PWM circuit typically compares an error voltage with a ramp signal. The outcome of this comparison determines the state of the output. In voltage mode operation the ramp signal is the voltage ramp of the timing capacitor. In current mode operation the ramp signal is the voltage ramp induced in a current sensing element. The ramp input of the PWM comparator is pinned out so that the user can decide which mode of operation best suits the application requirements. The ramp input has a 1.25 V offset such that whenever the voltage at this pin exceeds the Error Amplifier Output voltage minus 1.25 V, the PWM comparator will cause the PWM latch to set, disabling the outputs. Once the PWM latch is set, only a blanking pulse by the oscillator can reset it, thus initiating the next cycle.

A toggle flip flop connected to the output of the PWM latch controls which output is active. The flip flop is pulsed by an OR gate that gets its inputs from the oscillator clock and the output of the PWM latch. A pulse from either one will cause the flip flop to enable the other output.

Current Limiting and Shutdown

A pin is provided to perform current limiting and shutdown operations. Two comparators are connected to the input of this pin. When the voltage at this pin exceeds 1.0 V, one of the comparators is activated. The output of this comparator sets the PWM latch, which disables the output. In this way cycle−by−cycle current limiting is accomplished. If a current limit resistor is used in series with the power devices, the value of the resistor is found by:

$$R_{Sense} = \frac{1.0\ V}{I_{pk\ (switch)}}$$

If the voltage at this pin exceeds 1.4 V, the second comparator is activated. This comparator sets a latch which, in turn, causes the Soft−Start capacitor to be discharged. In this way a “hiccup” mode of recovery is possible in the case of output short circuits. If a current limit resistor is used in series with the output devices, the peak current at which the controller will enter a “hiccup” mode is given by:

$$I_{shutdown} = \frac{1.4\ V}{R_{Sense}}$$

Undervoltage Lockout

There are two undervoltage lockout circuits within the IC. The first senses V_{CC} and the second V_{ref}. During power−up, V_{CC} must exceed 9.2 V and V_{ref} must exceed 4.2 V before the outputs can be enabled and the Soft−Start latch released. If V_{CC} falls below 8.4 V or V_{ref} falls below 3.6 V, the outputs are disabled and the Soft−Start latch is activated. When the UVLO is active, the part is in a low current standby mode allowing the IC to have an off−line bootstrap startup circuit. Typical startup current is 500 μA.

Output

The MC34025 has two high current totem pole outputs specifically designed for direct drive of power MOSFETs. They are capable of up to ±2.0 A peak drive current with a typical rise and fall time of 30 ns driving a 1.0 nF load.

Separate pins for V_C and Power Ground are provided. With proper implementation, a significant reduction of switching transient noise imposed on the control circuitry is possible. The separate V_C supply input also allows the designer added flexibility in tailoring the drive voltage independent of V_{CC}.

Reference

A 5.1 V bandgap reference is pinned out and is trimmed to an initial accuracy of ±1.0% at 25°C. This reference has short circuit protection and can source in excess of 10 mA for powering additional control system circuitry.

Design Considerations

Do not attempt to construct the converter on wire−wrap or plug−in prototype boards. With high frequency, high power, switching power supplies it is imperative to have separate current loops for the signal paths and for the power paths. The printed circuit layout should contain a ground plane with low current signal and high current switch and output grounds returning on separate paths back to the input filter capacitor. All bypass capacitors and snubbers should be connected as close as possible to the specific part in question. The PC board lead lengths must be less than 0.5 inches for effective bypassing or snubbing.

Instabilities

In current mode control, an instability can be encountered at any given duty cycle. The instability is caused by the current feedback loop. It has been shown that the instability is caused by a double pole at half the switching frequency. If an external ramp (S_e) is added to the on−time ramp (S_n) of the current−sense waveform, stability can be achieved (see Figure 21).

One must be careful not to add too much ramp compensation. If too much is added, the system will start to perform like a voltage mode regulator. All benefits of current mode control will be lost. Figures 29A and 29B show examples of two different ways in which external ramp compensation can be implemented.

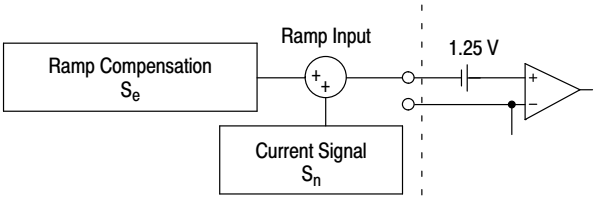


Figure 21. Ramp Compensation

A simple equation can be used to calculate the amount of external ramp necessary to add that will achieve stability in the current loop. For the following equations, the calculated values for the application circuit in Figure 37 are also shown.

$$S_e = \frac{V_O}{L}\left(\frac{N_S}{N_P}\right)(R_S)A_i$$

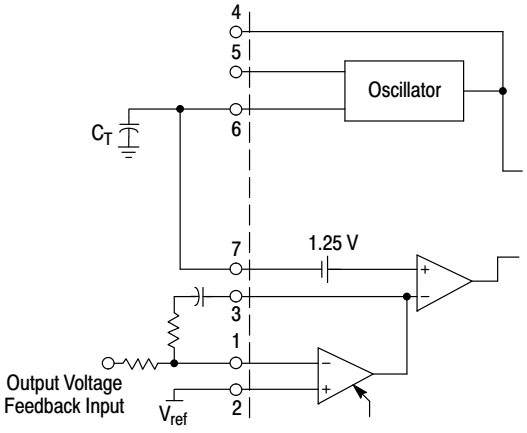
where:
- V_O = DC output voltage
- N_P, N_S = number of power transformer primary or secondary turns
- A_i = gain of the current sense network (see Figures 26, 27 and 28)
- L = output inductor
- R_S = current sense resistance

For the application circuit: $S_e = \frac{5}{1.8\ \mu}\left(\frac{4}{16}\right)(0.3)(0.55)$

$= 0.115\ V/\mu s$

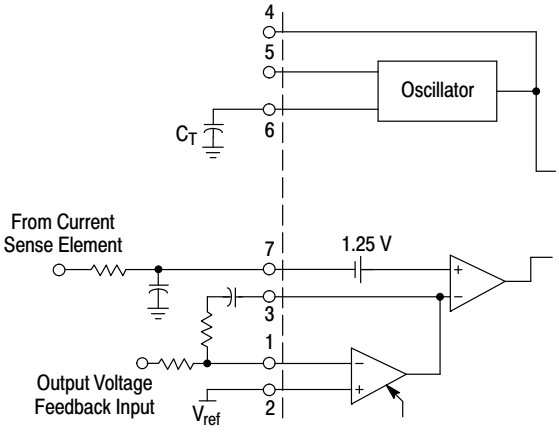
PIN FUNCTION DESCRIPTION

Pin No. DIP/SOIC	Function	Description
1	Error Amp Inverting Input	This pin is usually used for feedback from the output of the power supply.
2	Error Amp Noninverting Input	This pin is used to provide a reference in which an error signal can be produced on the output of the error amp. Usually this is connected to V_{ref}, however an external reference can also be used.
3	Error Amp Output	This pin is provided for compensating the error amp for poles and zeros encountered in the power supply system, mostly the output LC filter.
4	Clock	This is a bidirectional pin used for synchronization.
5	R_T	The value of R_T sets the charge current through timing Capacitor, C_T.
6	C_T	In conjunction with R_T, the timing Capacitor sets the switching frequency. Because this part is a push−pull output, each output runs at one−half the frequency set at this pin.
7	Ramp Input	For voltage mode operation this pin is connected to C_T. For current mode operation this pin is connected through a filter to the current sensing element.
8	Soft−Start	A capacitor at this pin sets the Soft−Start time.
9	Current Limit/Shutdown	This pin has two functions. First, it provides cycle−by−cycle current limiting. Second, if the current is excessive, this pin will reinitiate a Soft−Start cycle.
10	Ground	This pin is the ground for the control circuitry.
11	Output A	This is a high current totem pole output.
12	Power Ground	This is a separate power ground return that is connected back to the power source. It is used to reduce the effects of switching transient noise on the control circuitry.
13	V_C	This is a separate power source connection for the outputs that is connected back to the power source input. With a separate power source connection, it can reduce the effects of switching transient noise on the control circuitry.
14	Output B	This is a high current totem pole output.
15	V_{CC}	This pin is the positive supply of the control IC.
16	V_{ref}	This is a 5.1 V reference. It is usually connected to the noninverting input of the error amplifier.



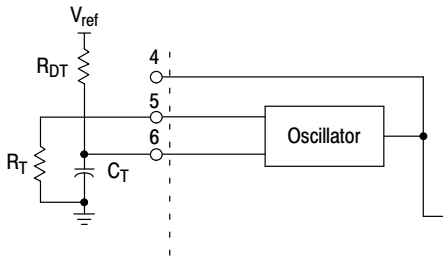
In voltage mode operation, the control range on the output of the Error Amplifier from 0% to 90% duty cycle is from 2.25 V to 4.05 V.

Figure 22. Voltage Mode Operation



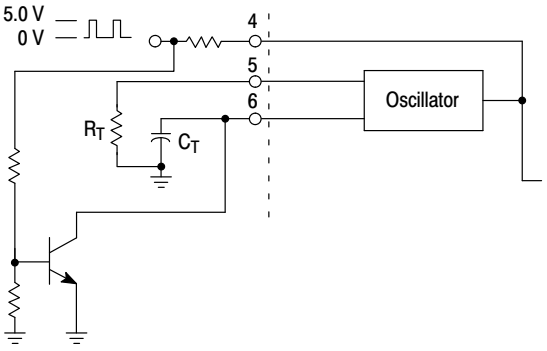
In current mode control, an RC filter should be placed at the ramp input to filter the leading edge spike caused by turn−on of a power MOSFET.

Figure 23. Current Mode Operation



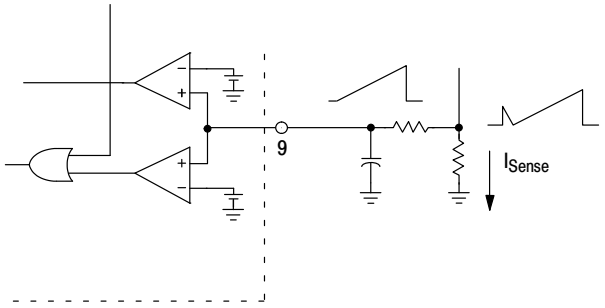
Additional dead time can be added by the addition of a dead time resistor from V_{ref} to C_T. See text on oscillator section for more information.

Figure 24. Dead Time Addition



The sync pulse fed into the clock pin must be at least 3.9 V. R_T and C_T need to be set 10% slower than the sync frequency. This circuit is also used in voltage mode operation for master/slave operation. The clock signal would be coming from the master which is set at the desired operating frequency, while the slave is set 10% slower.

Figure 25. External Clock Synchronization



The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. If a transformer is used, the gain can be calculated by:

$$A_i = \frac{R_{Sense}}{\text{turns ratio}}$$

Figure 26. Resistive Current Sensing

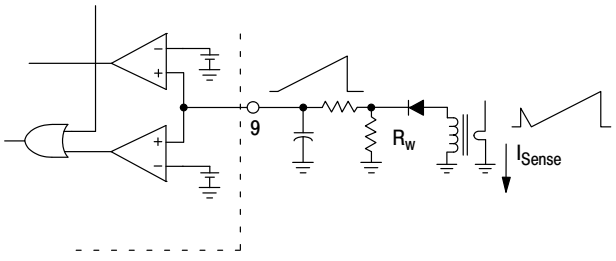


Figure 27. Primary Side Current Sensing

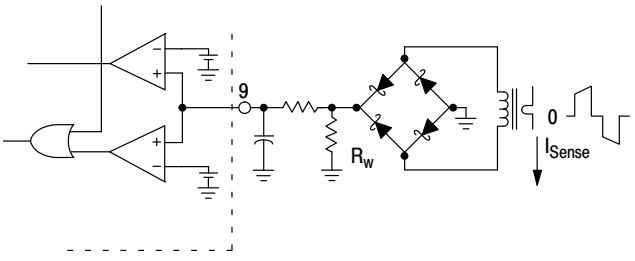
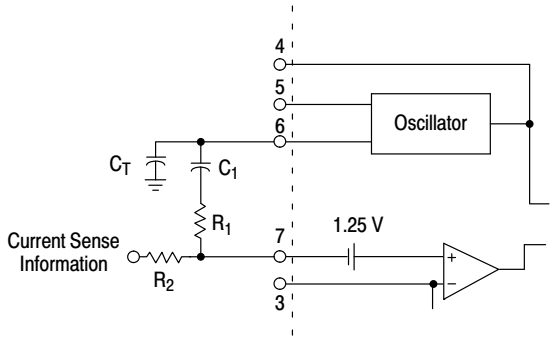


Figure 28. Primary or Secondary Side Current Sensing

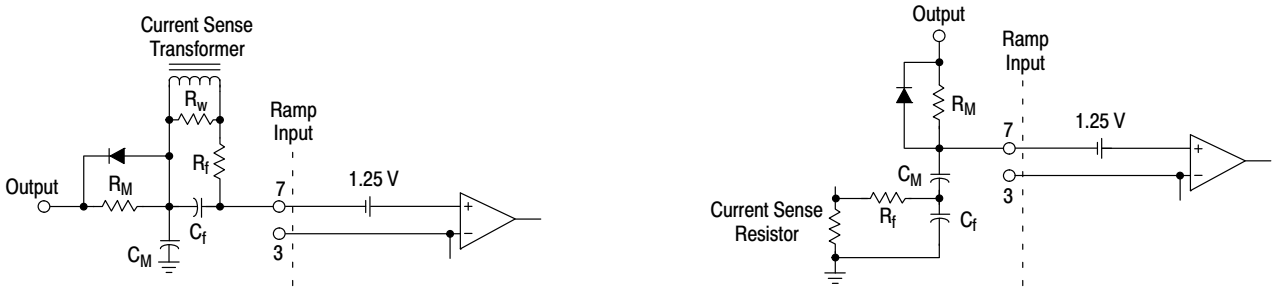
The addition of an RC filter will eliminate instability caused by the leading edge spike on the current waveform. This sense signal can also be used at the ramp input pin for current mode control. For ramp compensation it is necessary to know the gain of the current feedback loop. The gain can be calculated by:

$$A_i = \frac{R_w}{\text{turns ratio}}$$



This method of slope compensation is easy to implement, however, it is noise sensitive. Capacitor C_1 provides AC coupling. The oscillator signal is added to the current signal by a voltage divider consisting of resistors R_1 and R_2.

Figure 29A. Slope Compensation (Noise Sensitive)



When only one output is used, this method of slope compensation can be used and it is relatively noise immune. Resistor R_M and capacitor C_M provide the added slope necessary. By choosing R_M and C_M with a larger time constant than the switching frequency, you can assume that its charge is linear. First choose C_M, then R_M can be adjusted to achieve the required slope. The diode provides a reset pulse at the ramp input at the end of every cycle. The charge current I_M can be calculated by $I_M = C_M S_e$. Then R_M can be calculated by $R_M = V_{CC}/I_M$.

Figure 29B. Slope Compensation (Noise Immune)

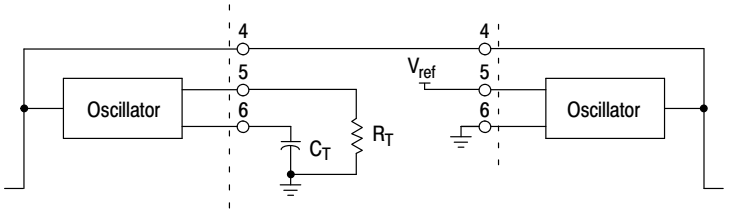


Figure 30. Current Mode Master/Slave Operation Over Short Distances

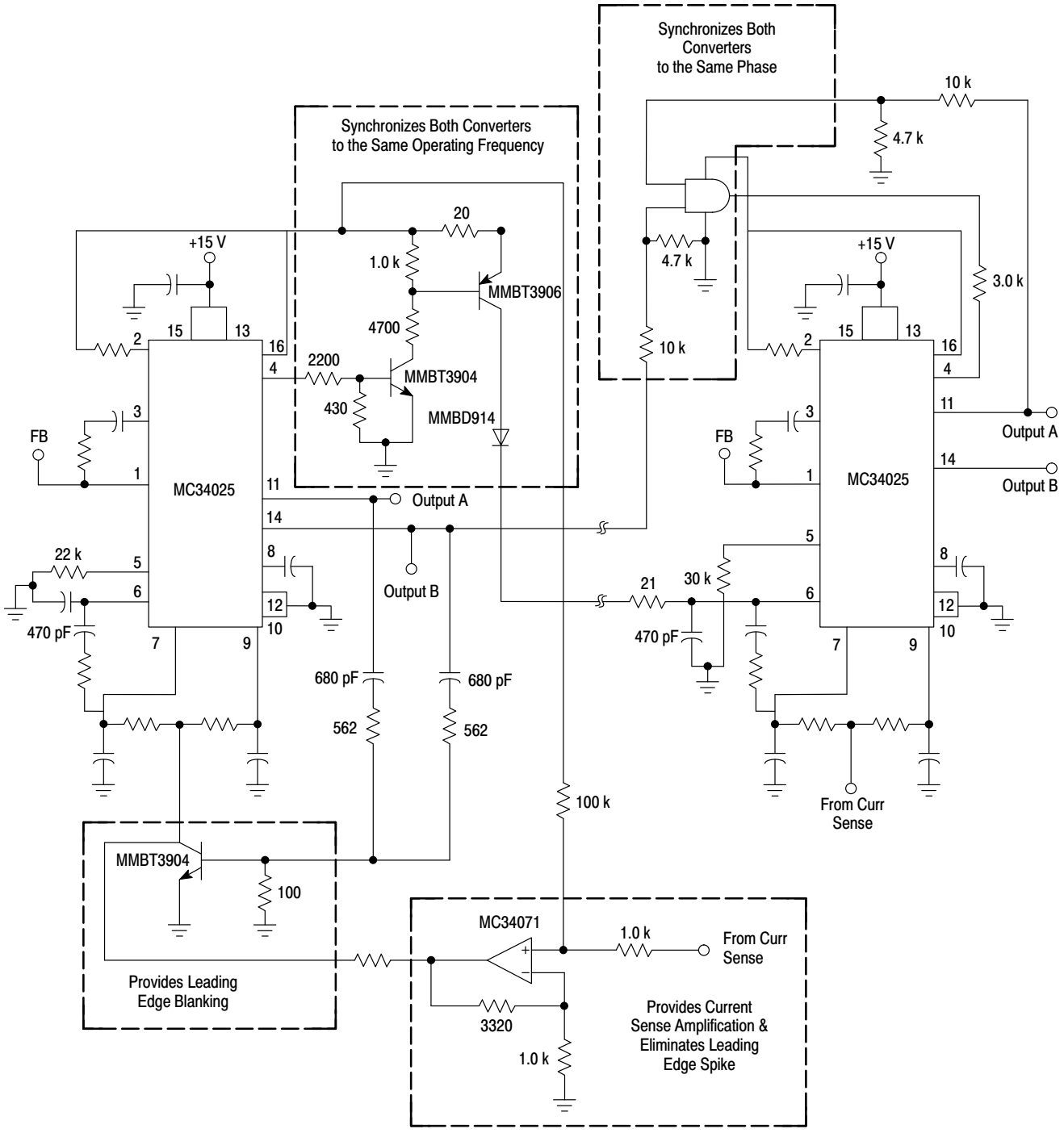
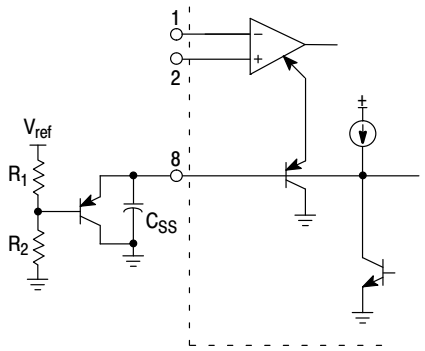


Figure 31. Synchronization Over Long Distances

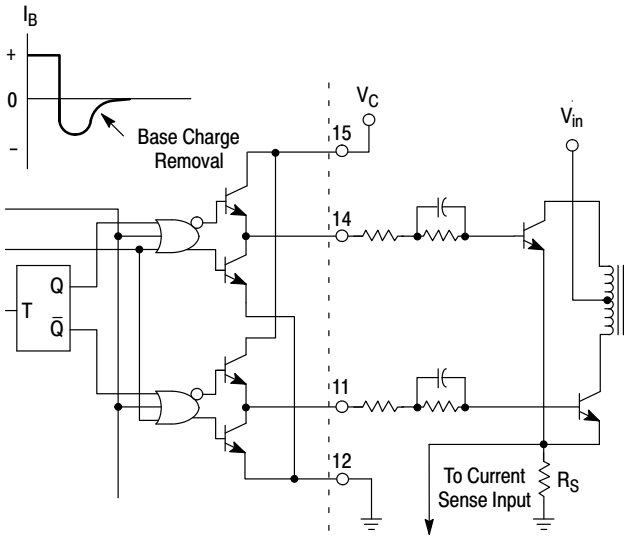


In voltage mode operation, the maximum duty cycle can be clamped. By the addition of a PNP transistor to buffer the clamp voltage, the Soft−Start current is not affected by R_1.

The new equation for Soft−Start is $t \approx \frac{V_{clamp} + 0.6}{9.0\ \mu A} (C_{SS})$

In current mode operation, this circuit will limit the maximum voltage allowed at the ramp input to end a cycle.

Figure 32. Buffered Maximum Clamp Level



The totem pole output can furnish negative base current for enhanced transistor turn−off, with the addition of the capacitor in series with the base.

Figure 33. Bipolar Transistor Drive

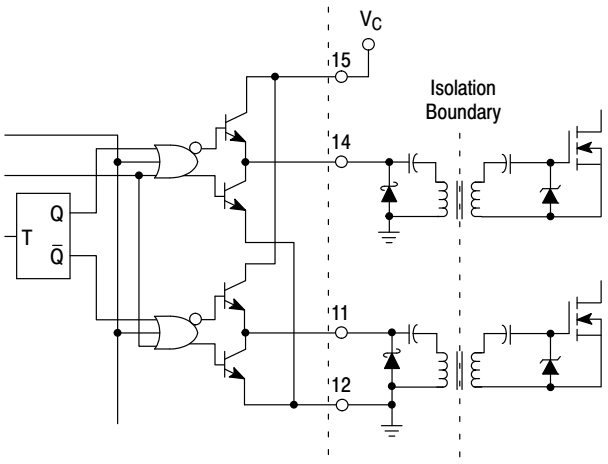


Figure 34. Isolated MOSFET Drive

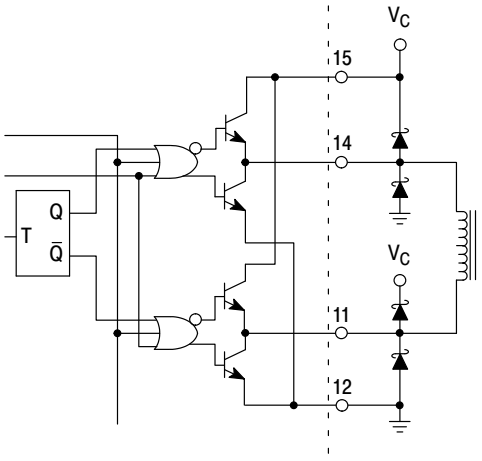
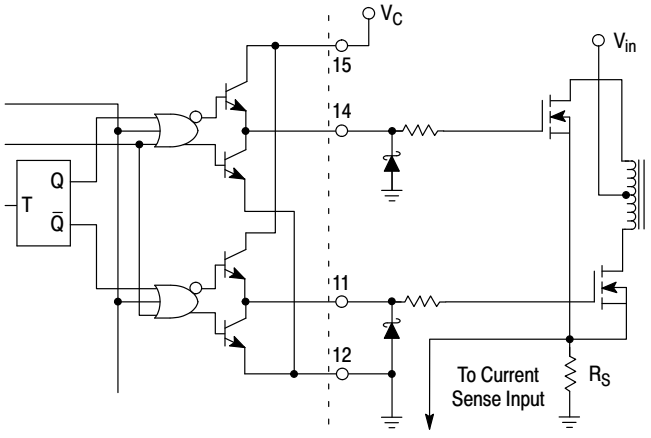


Figure 35. Direct Transformer Drive

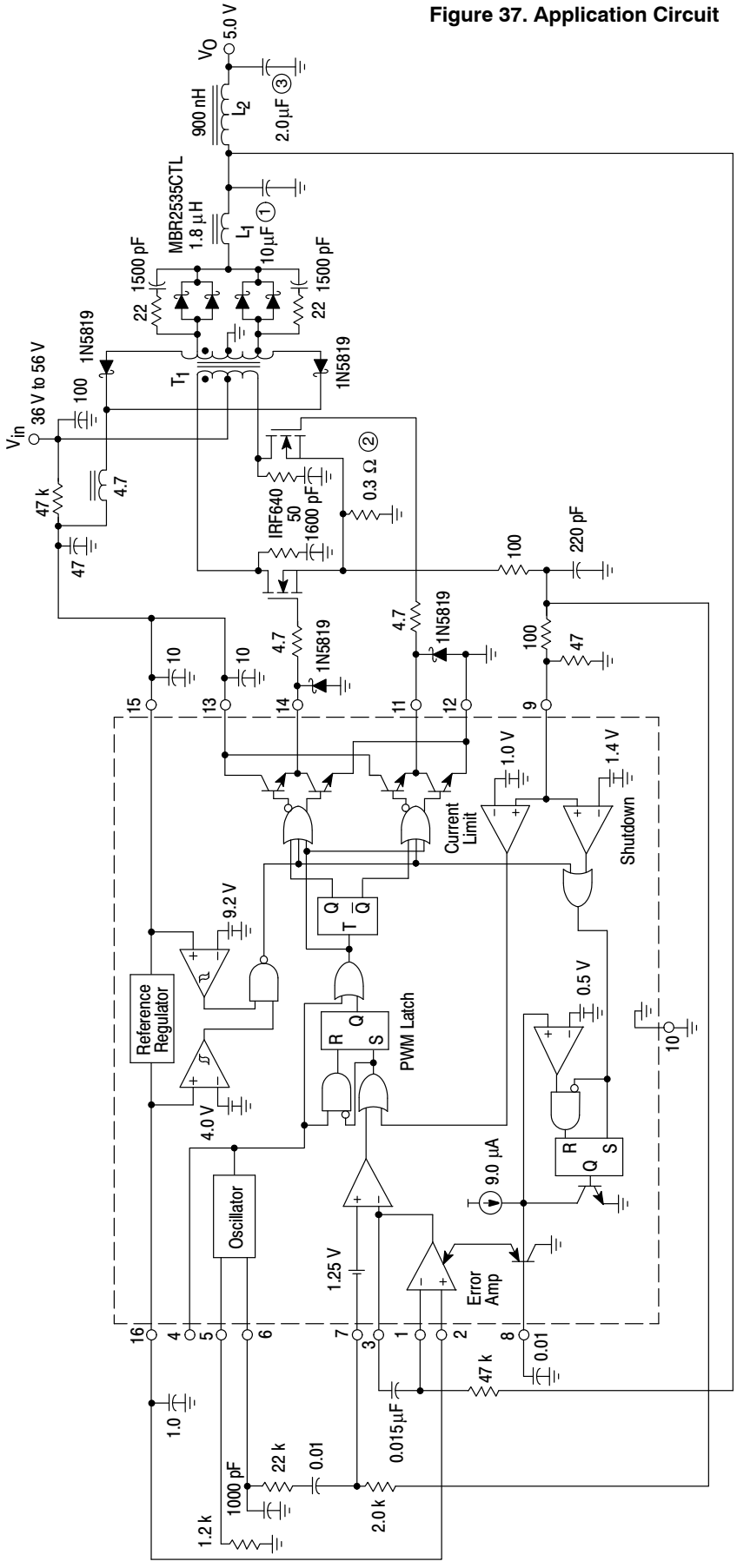
The totem pole output can easily drive pulse transformers. A Schottky diode is recommended when driving inductive loads at high frequencies. The diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground.



A series gate resistor may be needed to damp high frequency parasitic oscillation caused by a MOSFET's input capacitance and any series wiring inductance in the gate−source circuit. The series resistor will also decrease the MOSFET's switching speed. A Schottky diode can reduce the driver's power dissipation due to excessive ringing, by preventing the output pin from being driven below ground. The Schottky diode also prevents substrate injection when the output pin is driven below ground.

Figure 36. MOSFET Parasitic Oscillations

Figure 37. Application Circuit



Test	Condition	Result
Line Regulation	V_{in} = 40 V to 56 V, I_O = 15 A	14 mV = ±0.275%
Load Regulation	V_{in} = 48 V, I_O = 8.0 V to 15 A	54 mV = ±1.0%
Output Ripple	V_{in} = 48 V, I_O = 15 A	50 mVp−p
Efficiency	V_{in} = 48 V, I_O = 15 A	71.2%

T_1 – Primary: 16 turns center tapped #48 AWG (1300 strands litz wire)
Secondary: 4 turns center tapped 0.003″ (2 layers) copper foil
Bootstrap: 1 turn added to each secondary output #36 AWG
Core: Philips 3F3, part #4312 020 4124
Bobbin: Philips part #4322 021 3525
Coilcraft P3269−A

L_1 – 2 turns #48 AWG (1300 strands litz wire)
Core: Philips 3F3, part #EP10−3F3
Bobbin: Philips part #EP10PCB1−8
L = 1.8 µH
Coilcraft P3270−A

L_2 – 7 turns #18 AWG, 1/2″ diameter air core
Coilcraft P3271−A

Heatsinks – Power FET: AAVID Heatsink #533902B02554 with clip
Output Rectifiers: AAVID Heatsink #533402B02552 with clip

Insulators – All power devices are insulated with Berquist Sil−Pad 1500
① – 10 (1.0 µF) ceramic capacitors in parallel
② – 5 (1.5 Ω) resistors in parallel
③ – 2 (1.0 µF) cearmic capacitors in parallel

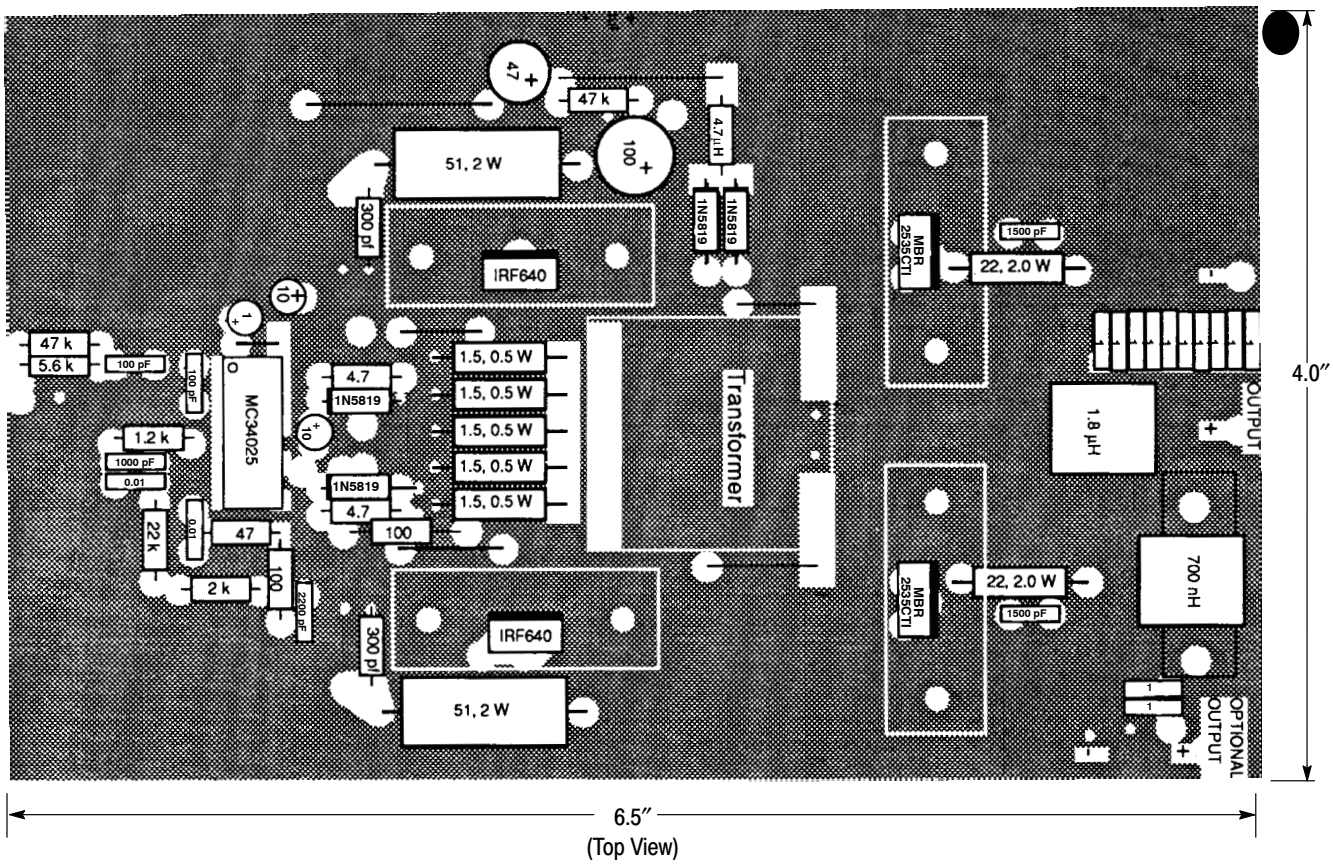
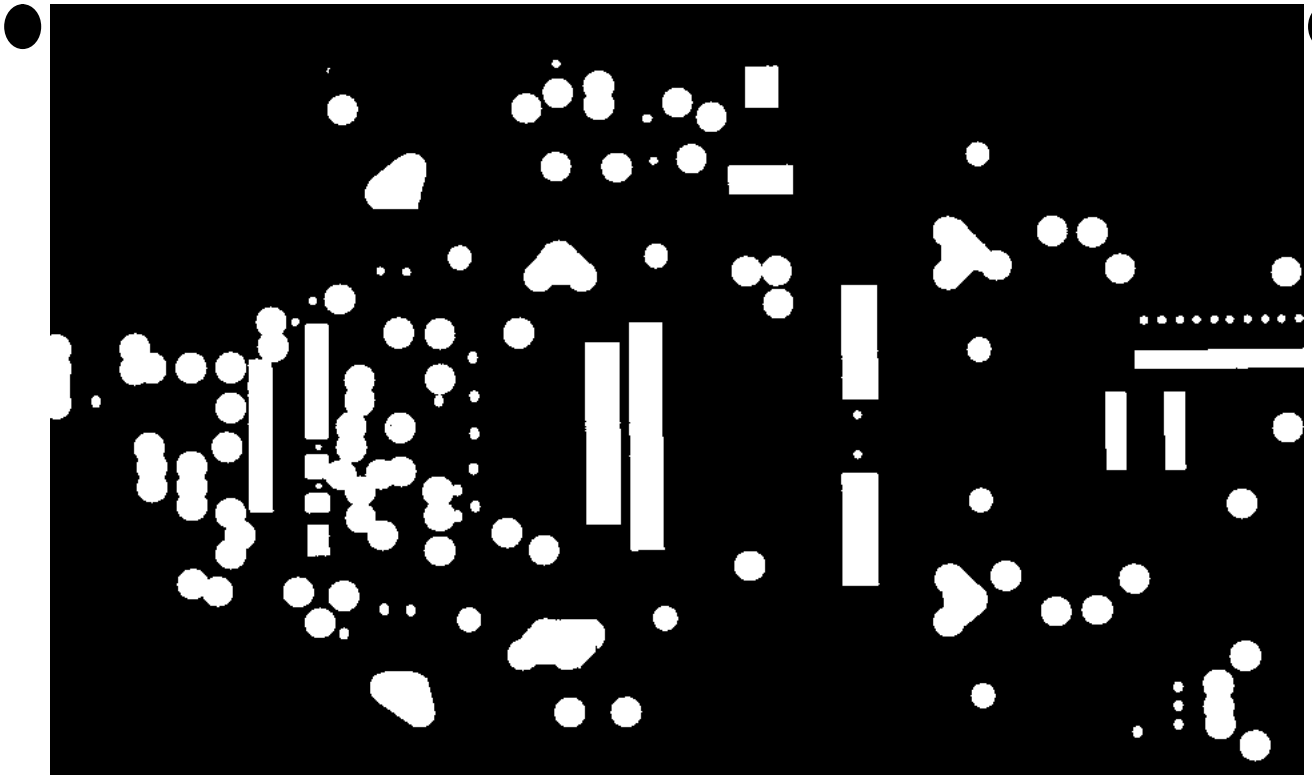
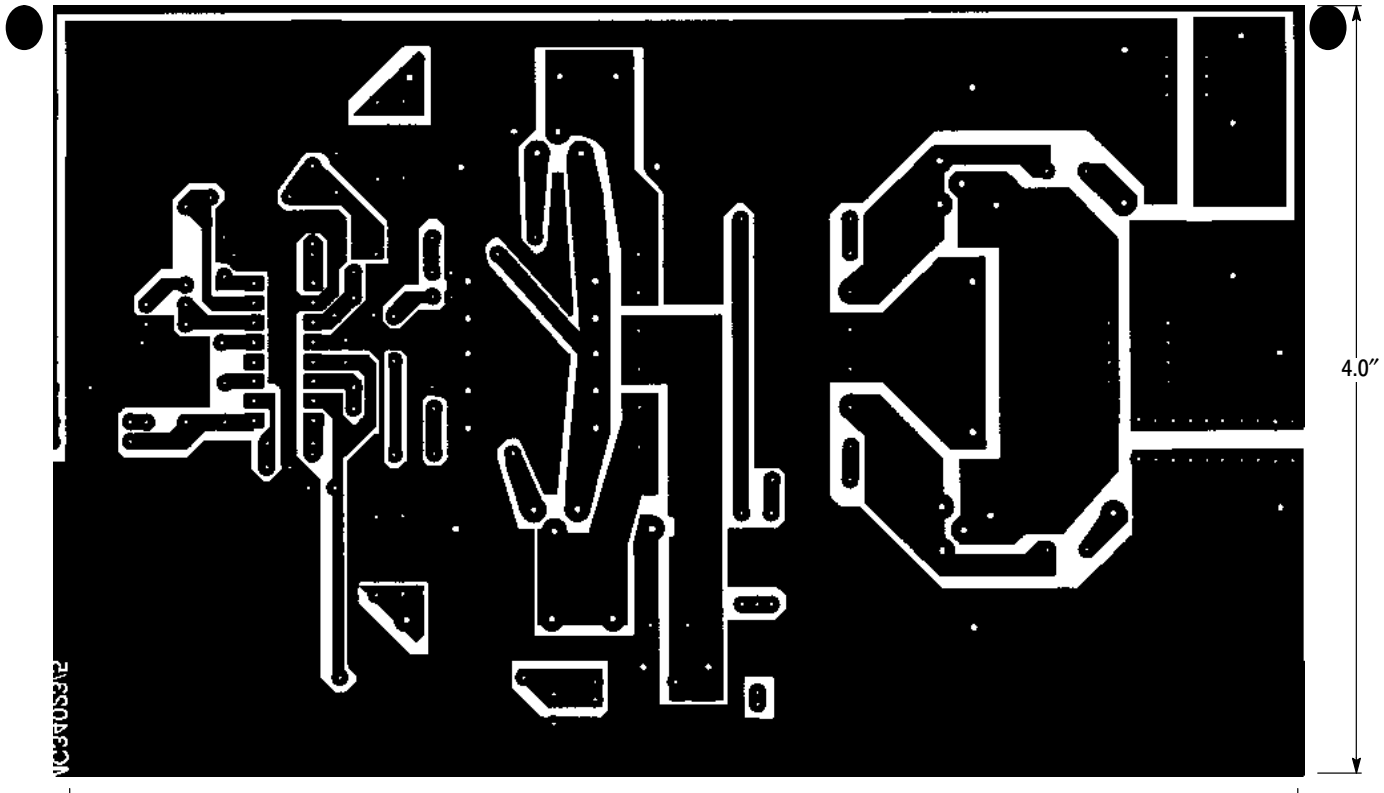


Figure 38. PC Board With Components



(Top View)



(Bottom View)

Figure 39. PC Board Without Components

ORDERING INFORMATION

Device	Package	Shipping†
MC33025DWG	SOIC−16WB (Pb−Free)	47 Units / Rail
MC33025DWR2G	SOIC−16WB (Pb−Free)	1000 Units / Tape & Reel
MC33025PG	PDIP−16 (Pb−Free)	25 Units / Rail
MC34025DWG	SOIC−16WB (Pb−Free)	47 Units / Rail
MC34025DWR2G	SOIC−16WB (Pb−Free)	1000 Units / Tape & Reel
MC34025PG	PDIP−16 (Pb−Free)	25 Units / Rail

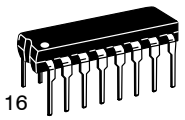
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

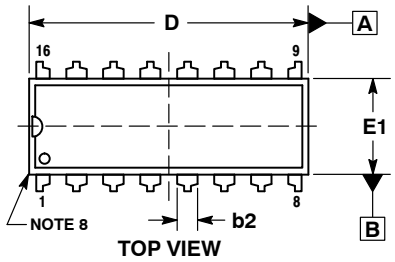
ON Semiconductor®

PDIP−16
CASE 648−08
ISSUE V

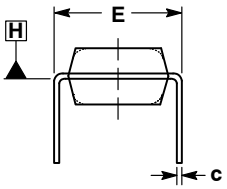
DATE 22 APR 2015



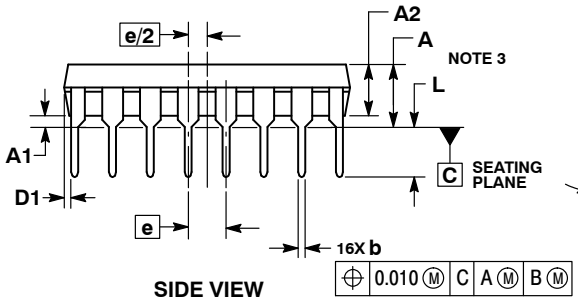
SCALE 1:1



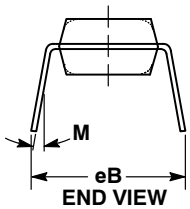
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



END VIEW
NOTE 6

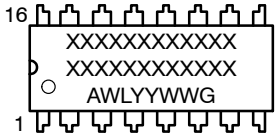
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.735	0.775	18.67	19.69
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

STYLE 2:
PIN 1. COMMON DRAIN
2. COMMON DRAIN
3. COMMON DRAIN
4. COMMON DRAIN
5. COMMON DRAIN
6. COMMON DRAIN
7. COMMON DRAIN
8. COMMON DRAIN
9. GATE
10. SOURCE
11. GATE
12. SOURCE
13. GATE
14. SOURCE
15. GATE
16. SOURCE

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

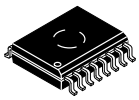
*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

DOCUMENT NUMBER:	98ASB42431B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	PDIP−16	PAGE 1 OF 1

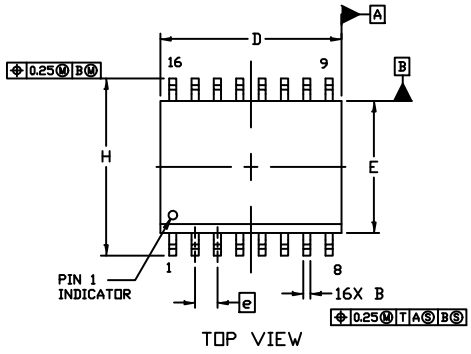
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−16 WB
CASE 751G
ISSUE E

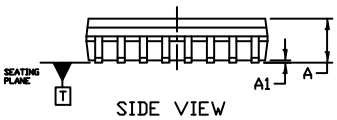
DATE 08 OCT 2021



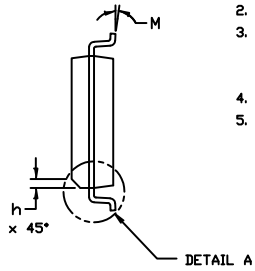
1
SCALE 1:1



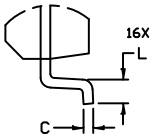
TOP VIEW



SIDE VIEW



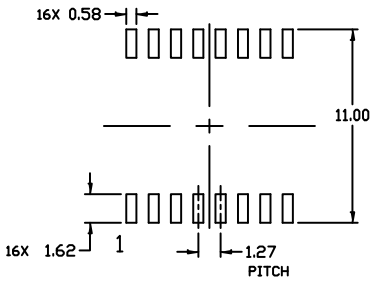
END VIEW



DETAIL A
2X SCALE

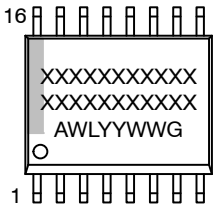
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOIC−16 WB**	**PAGE 1 OF 1**

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