

Low-Voltage CMOS 3-to-8 Decoder/Demultiplexer

With 5 V-Tolerant Inputs

MC74LCX138

The MC74LCX138 is a high performance, 3-to-8 decoder/demultiplexer operating from a 2.3 to 3.6 V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance. A V_I specification of 5.5 V allows MC74LCX138 inputs to be safely driven from 5 V devices. The MC74LCX138 is suitable for memory address decoding and other TTL level bus-oriented applications.

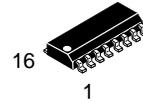
The MC74LCX138 high-speed 3-to-8 decoder/demultiplexer accepts three binary weighted inputs (A0, A1, A2) and, when enabled, provides eight mutually exclusive active-LOW outputs ($\overline{O0}$ – $\overline{O7}$). The LCX138 features three Enable inputs, two active-LOW ($\overline{E1}$, $\overline{E2}$) and one active-HIGH (E3). All outputs will be HIGH unless $\overline{E1}$ and $\overline{E2}$ are LOW, and E3 is HIGH. This multiple enabled function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four LCX138 devices and one inverter (see Figure 1). The LCX138 can be used as an 8-output demultiplexer by using one of the active-LOW Enable inputs as the data input and the other Enable inputs as strobes. The Enable inputs which are not used must be permanently tied to their appropriate active-HIGH or active-LOW state.

Current drive capability is 24 mA at the outputs.

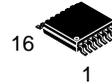
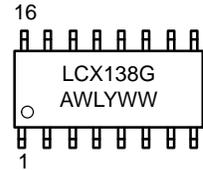
Features

- Designed for 2.3 V to 3.6 V V_{CC} Operation
- 5 V Tolerant Inputs – Interface Capability With 5 V TTL Logic
- LVTTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10 μ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500 mA
- ESD Performance: Human Body Model >2000 V
Machine Model >200 V
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

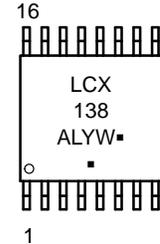
MARKING DIAGRAMS



SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F



A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 3.

MC74LCX138

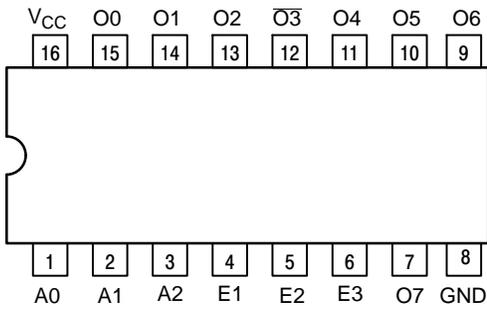


Figure 1. Pinout: 16-Lead (Top View)

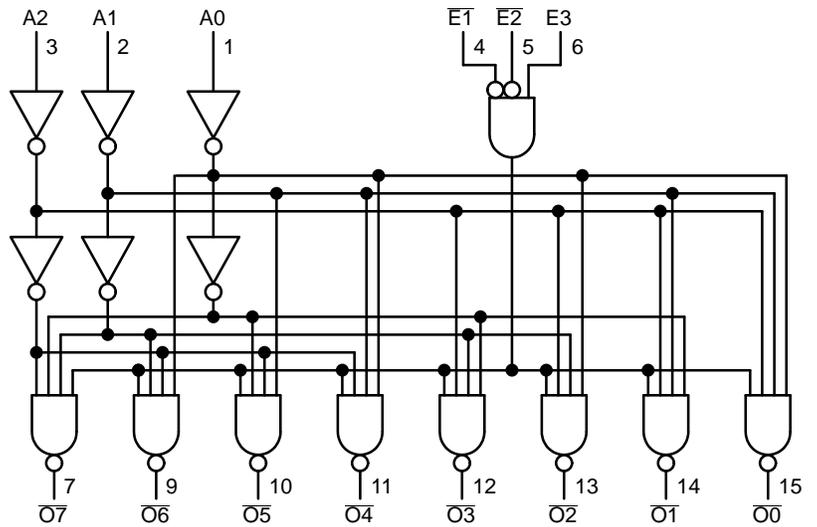


Figure 2. Logic Diagram

PIN NAMES

Pins	Function
A0-A2	Address Inputs
E1-E2	Enable Inputs
E3	Enable Input
O0-O7	Outputs

TRUTH TABLE

Inputs						Outputs							
E1	E2	E3	A0	A1	A2	O0	O1	O2	O3	O4	O5	O6	O7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = High Voltage Level

L = Low Voltage Level

X = High or Low Voltage Level and Transitions are Acceptable

For I_{CC} reasons, DO NOT FLOAT Inputs

MC74LCX138

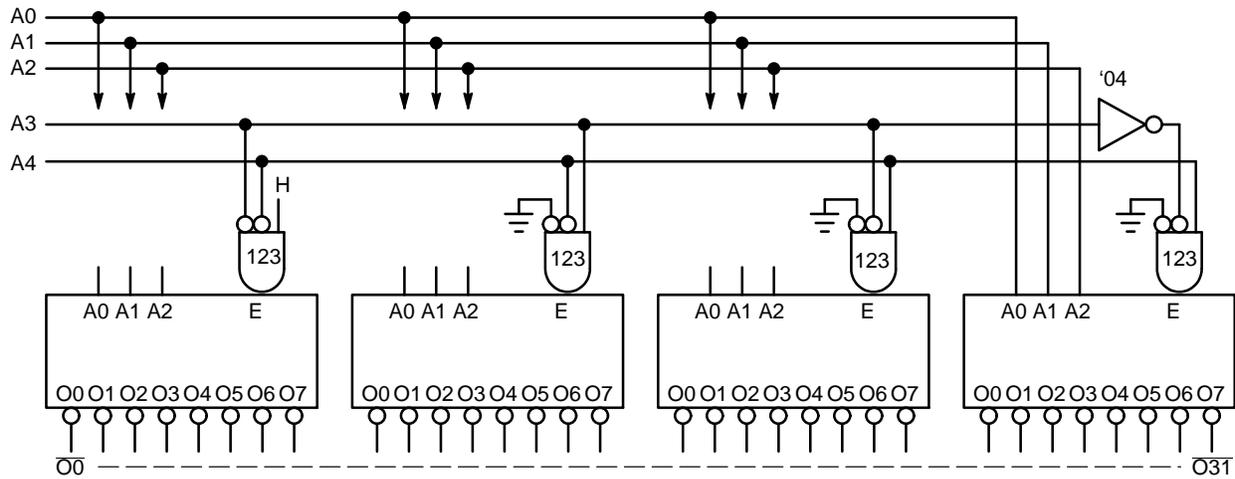


Figure 3. Expansion to 1-of-32 Decoding

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74LCX138DR2G	SOIC-16 (Pb-Free)	2500 Tape & Reel
MC74LCX138DTG	TSSOP-16 (Pb-Free)	96 Units / Rail
MC74LCX138DTR2G	TSSOP-16 (Pb-Free)	2500 Tape & Reel

DISCONTINUED (Note 1)

NLV74LCX138DR2G*	SOIC-16 (Pb-Free)	2500 Tape & Reel
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[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

1. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

MAXIMUM RATINGS

Symbol	Parameter	Value	Condition	Units
V _{CC}	DC Supply Voltage	-0.5 to +7.0		V
V _I	DC Input Voltage	-0.5 ≤ V _I ≤ +7.0		V
V _O	DC Output Voltage	-0.5 ≤ V _O ≤ V _{CC} + 0.5	Output in HIGH or LOW State (Note 1)	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50	V _O < GND	mA
		+50	V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current Per Supply Pin	±100		mA
I _{GND}	DC Ground Current Per Ground Pin	±100		mA
T _{STG}	Storage Temperature Range	-65 to +150		°C
MSL	Moisture Sensitivity		Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. I_O absolute maximum rating must be observed.

MC74LCX138

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
V _{CC}	Supply Voltage	2.0 1.5	2.5, 3.3 2.5, 3.3	3.6 3.6	V
V _I	Input Voltage	0		5.5	V
V _O	Output Voltage	0		V _{CC}	V
I _{OH}	HIGH Level Output Current			-24 -12 -8	mA
I _{OL}	LOW Level Output Voltage			+24 +12 +8	mA
T _A	Operating Free-Air Temperature	-40		+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate, V _{IN} from 0.8 V to 2.0 V, V _{CC} = 3.0 V	0		10	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic	Condition	T _A = -40°C to +85°C		Units
			Min	Max	
V _{IH}	HIGH Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V	1.7		V
		2.7 V ≤ V _{CC} ≤ 3.6 V	2.0		
V _{IL}	LOW Level Input Voltage (Note 2)	2.3 V ≤ V _{CC} ≤ 2.7 V		0.7	V
		2.7 V ≤ V _{CC} ≤ 3.6 V		0.8	
V _{OH}	HIGH Level Output Voltage	2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OH} = -100 μA	V _{CC} - 0.2		V
		V _{CC} = 2.3 V; I _{OH} = -8 mA	1.8		
		V _{CC} = 2.7 V; I _{OH} = -12 mA	2.2		
		V _{CC} = 3.0 V; I _{OH} = -18 mA	2.4		
V _{OL}	LOW Level Output Voltage	2.3 V ≤ V _{CC} ≤ 3.6 V; I _{OL} = 100 μA		0.2	V
		V _{CC} = 2.3 V; I _{OL} = 8 mA		0.6	
		V _{CC} = 2.7 V; I _{OL} = 12 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 16 mA		0.4	
		V _{CC} = 3.0 V; I _{OL} = 24 mA		0.55	
I _{OFF}	Power Off Leakage Current	V _{CC} = 0, V _{IN} = 5.5 V or V _{OUT} = 5.5 V		10	μA
I _{IN}	Input Leakage Current	V _{CC} = 3.6 V, V _{IN} = 5.5 V or GND		±5	μA
I _{CC}	Quiescent Supply Current	V _{CC} = 3.6 V, V _{IN} = 5.5 V or GND		10	μA
ΔI _{CC}	Increase in I _{CC} per Input	2.3 ≤ V _{CC} ≤ 3.6 V; V _{IH} = V _{CC} - 0.6 V		500	μA

2. These values of V_I are used to test DC electrical characteristics only.

AC CHARACTERISTICS (t_R = t_F = 2.5 ns; R_L = 500 Ω)

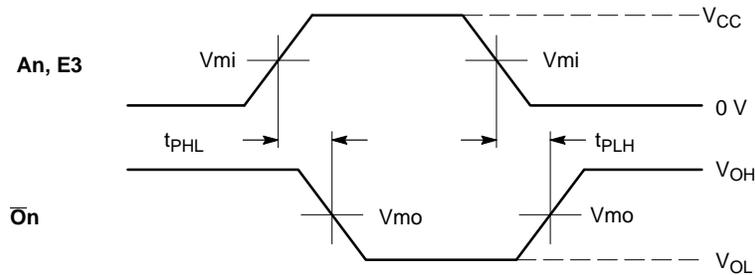
Symbol	Parameter	Waveform	Limits						Units
			T _A = -40°C to +85°C						
			V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 2.7 V		V _{CC} = 2.5 V ± 0.2 V		
			C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max		
t _{PLH} t _{PHL}	Propagation Delay An to $\bar{O}n$	1, 2	1.5	6.0	1.5	7.0	1.5	7.2	ns
			1.5	6.0	1.5	7.0	1.5	7.2	
t _{PLH} t _{PHL}	Propagation Delay E1, E2 to $\bar{O}n$	2	1.5	6.5	1.5	7.5	1.5	8.4	ns
			1.5	6.5	1.5	7.5	1.5	8.4	
t _{PLH} t _{PHL}	Propagation Delay E3 to $\bar{O}n$	1	1.5	6.0	1.5	7.0	1.5	7.2	ns
			1.5	6.0	1.5	7.0	1.5	7.2	
t _{OSSL} t _{OSLH}	Output-to-Output Skew (Note 3)			1.0 1.0					ns

3. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSSL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

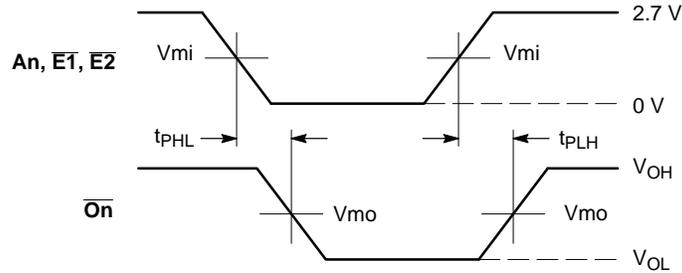
MC74LCX138

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Condition	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = 3.3 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	10 MHz, $V_{CC} = 3.3 \text{ V}$, $V_I = 0 \text{ V}$ or V_{CC}	25	pF



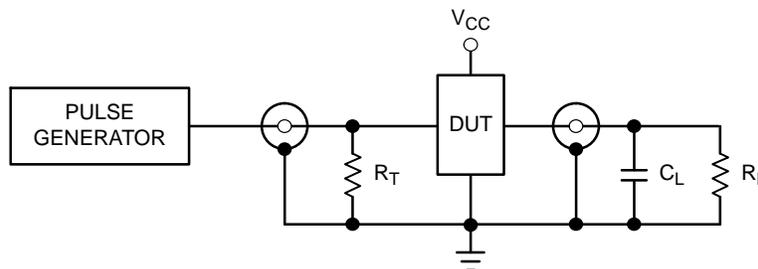
WAVEFORM 1: PROPAGATION DELAYS FOR INVERTING OUTPUTS



WAVEFORM 2: PROPAGATION DELAYS FOR NON-INVERTING OUTPUTS

Symbol	V_{CC}		
	$3.3 \text{ V} \pm 0.3 \text{ V}$	2.7 V	$2.5 \text{ V} \pm 0.2 \text{ V}$
V_{mi}	1.5 V	1.5 V	$V_{CC}/2$
V_{mo}	1.5 V	1.5 V	$V_{CC}/2$

Figure 4. AC Waveforms



$C_L = 50 \text{ pF}$ at $V_{CC} = 3.3 \pm 0.3 \text{ V}$ or equivalent (includes jig and probe capacitance)
 $C_L = 30 \text{ pF}$ at $V_{CC} = 2.5 \pm 0.2 \text{ V}$ or equivalent (includes jig and probe capacitance)
 $R_L = R_1 = 500 \Omega$ or equivalent
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

Figure 5. Test Circuit

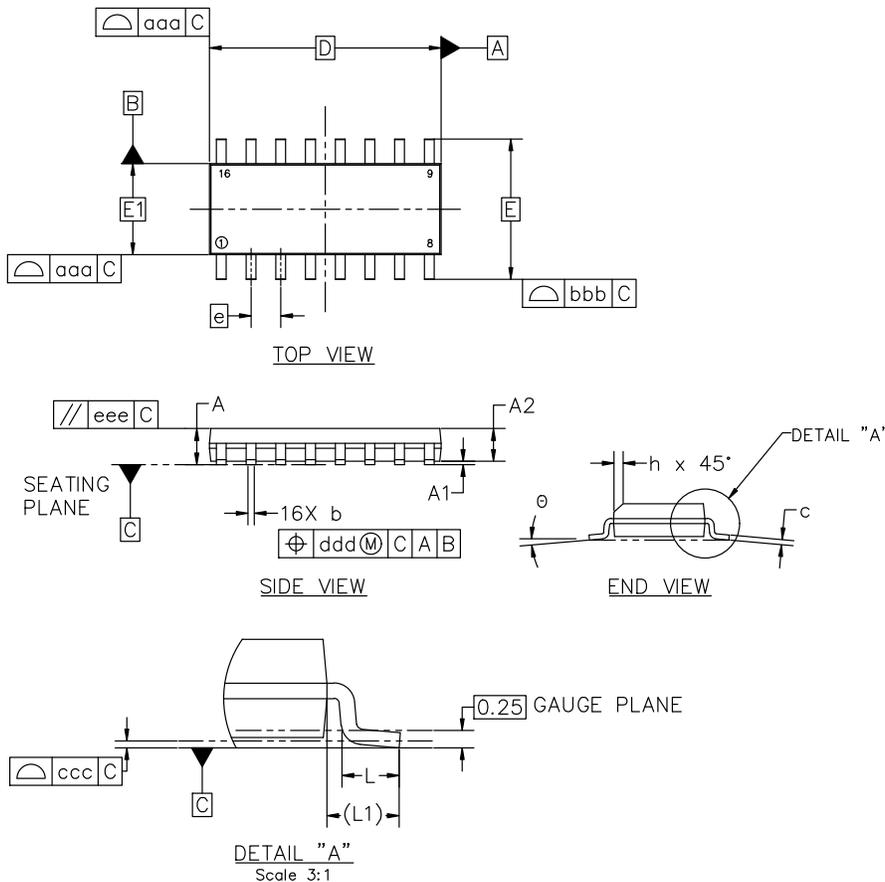


SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

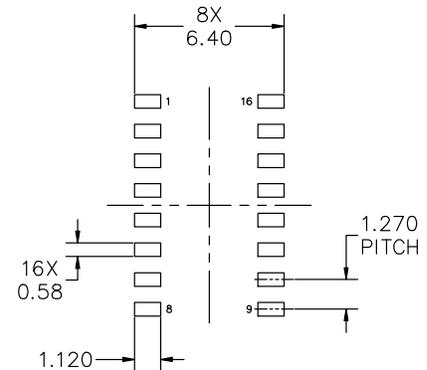
DATE 29 MAY 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

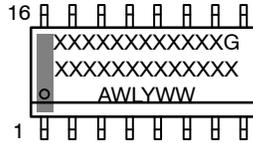
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SOIC-16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

**GENERIC
MARKING DIAGRAM***



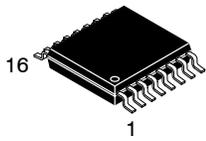
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

<p>STYLE 1:</p> <p>PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR</p>	<p>STYLE 2:</p> <p>PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE</p>	<p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4</p>	<p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1</p>
<p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1</p>	<p>STYLE 6:</p> <p>PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE</p>	<p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH</p>	

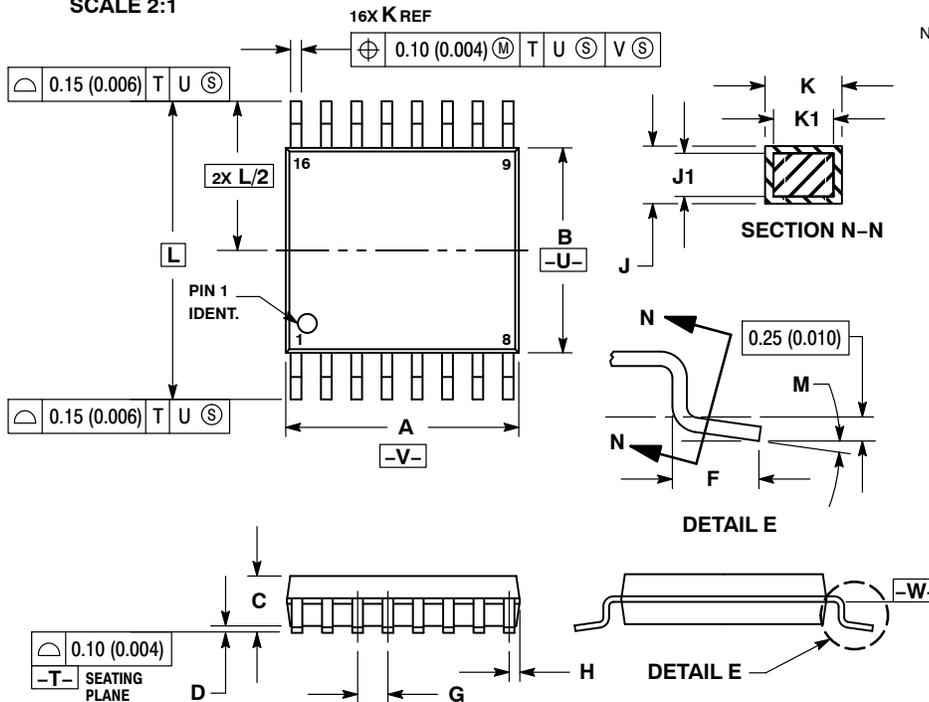
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TSSOP-16 WB
CASE 948F
ISSUE B

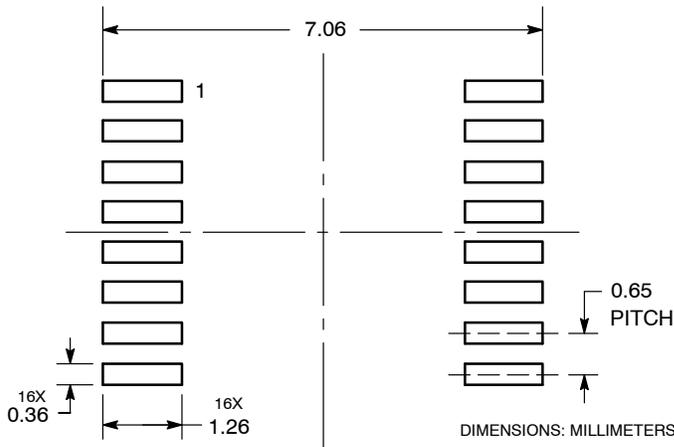
DATE 19 OCT 2006



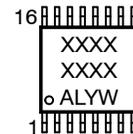
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED
SOLDERING FOOTPRINT*



GENERIC
MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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