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DATA SHEET
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Silicon Power Transistors

MJ21193 - PNP
MJ21194 - NPN

The MJ21193 (PNP) and MJ21194 (NPN) utilize Perforated Emitter technology and are specifically designed for high power audio output, disk head positioners and linear applications.

Features

- Total Harmonic Distortion Characterized
- High DC Current Gain
- Excellent Gain Linearity
- High SOA
- These Devices are Pb−Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	250	Vdc
Collector−Base Voltage	V_{CBO}	400	Vdc
Emitter−Base Voltage	V_{EBO}	5	Vdc
Collector−Emitter Voltage − 1.5 V	V_{CEX}	400	Vdc
Collector Current − Continuous	I_C	16	Adc
Collector Current − Peak (Note 1)	I_{CM}	30	Adc
Base Current − Continuous	I_B	5	Adc
Total Power Dissipation @ T_C = 25°C Derate Above 25°C	P_D	250 1.43	W W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	− 65 to +200	°C

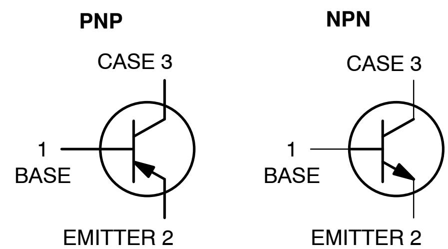
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.
1. Pulse Test: Pulse Width = 5 μs, Duty Cycle ≤ 10%. (continued)

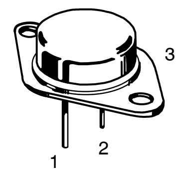
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction−to−Case	$R_{\theta JC}$	0.7	°C/W

16 AMP COMPLEMENTARY SILICON POWER TRANSISTORS 250 VOLTS, 250 WATTS

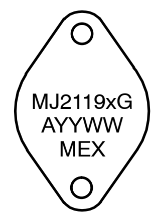
SCHEMATIC





TO−204AA (TO−3)
CASE 1−07
STYLE 1

MARKING DIAGRAM



MJ2119x	=	Device Code x = 3 or 4
G	=	Pb−Free Package
A	=	Assembly Location
YY	=	Year
WW	=	Work Week
MEX	=	Country of Origin

ORDERING INFORMATION

Device	Package	Shipping†
MJ21193G	TO−3 (Pb−Free)	100 Units / Tray
MJ21194G	TO−3 (Pb−Free)	100 Units / Tray

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

December, 2024 − Rev. 7
Publication Order Number:
MJ21193/D

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector−Emitter Sustaining Voltage (I_C = 100 mAdc, I_B = 0)	$V_{CEO(sus)}$	250	−	−	Vdc
Collector Cutoff Current (V_{CE} = 200 Vdc, I_B = 0)	I_{CEO}	−	−	100	μAdc
Emitter Cutoff Current (V_{CE} = 5 Vdc, I_C = 0)	I_{EBO}	−	−	100	μAdc
Collector Cutoff Current (V_{CE} = 250 Vdc, $V_{BE(off)}$ = 1.5 Vdc)	I_{CEX}	−		100	μAdc
SECOND BREAKDOWN					
Second Breakdown Collector Current with Base Forward Biased	$I_{S/b}$				Adc
(V_{CE} = 50 Vdc, t = 1 s (non−repetitive)		5	−	−	
(V_{CE} = 80 Vdc, t = 1 s (non−repetitive)		2.5	−	−	
ON CHARACTERISTICS					
DC Current Gain	h_{FE}			75	
(I_C = 8 Adc, V_{CE} = 5 Vdc)		25	−		
(I_C = 16 Adc, I_B = 5 Adc)		8	−		
Base−Emitter On Voltage (I_C = 8 Adc, V_{CE} = 5 Vdc)	$V_{BE(on)}$	−	−	2.2	Vdc
Collector−Emitter Saturation Voltage	$V_{CE(sat)}$				Vdc
(I_C = 8 Adc, I_B = 0.8 Adc)		−	−	1.4	
(I_C = 16 Adc, I_B = 3.2 Adc)		−	−	4	
DYNAMIC CHARACTERISTICS					
Total Harmonic Distortion at the Output	T_{HD}				%
V_{RMS} = 28.3 V, f = 1 kHz, P_{LOAD} = 100 W_{RMS} — h_{FE} unmatched		−	0.8	−	
(Matched pair h_{FE} = 50 @ 5 A/5 V) — h_{FE} matched		−	0.08	−	
Current Gain Bandwidth Product (I_C = 1 Adc, V_{CE} = 10 Vdc, f_{test} = 1 MHz)	f_T	4	−	−	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f_{test} = 1 MHz)	C_{ob}	−	−	500	pF

NOTE: Pulse Test: Pulse Width = 300 μs, Duty Cycle ≤2%

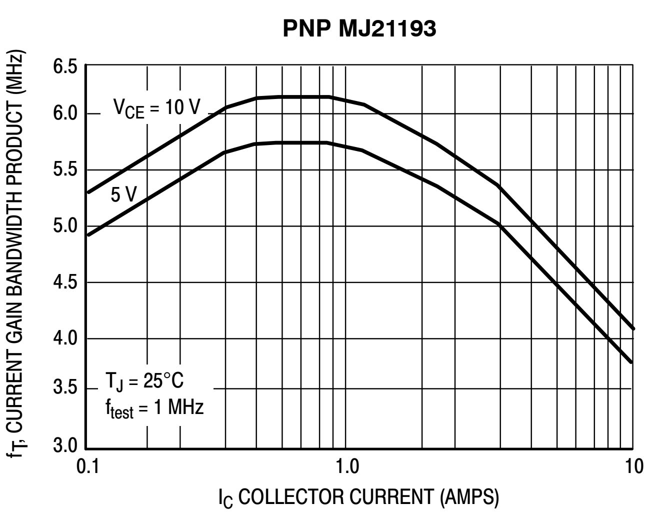


Figure 1. Typical Current Gain Bandwidth Product

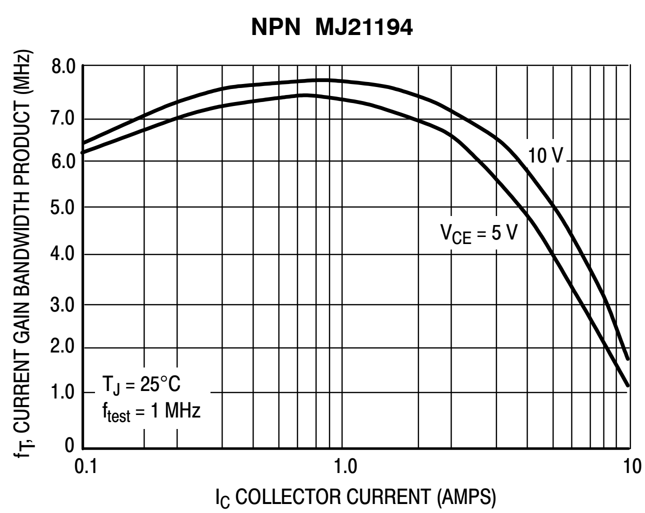


Figure 2. Typical Current Gain Bandwidth Product

TYPICAL CHARACTERISTICS

PNP MJ21193

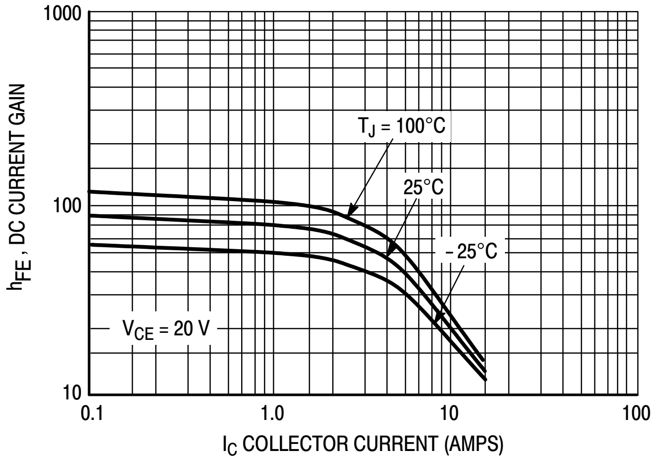


Figure 3. DC Current Gain, V_{CE} = 20 V

NPN MJ21194

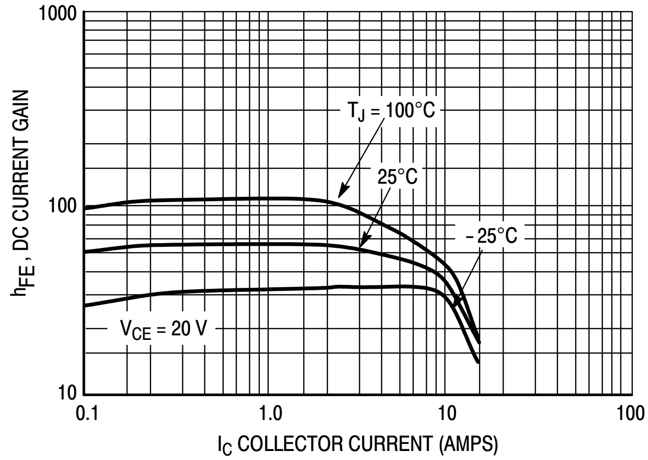


Figure 4. DC Current Gain, V_{CE} = 20 V

PNP MJ21193

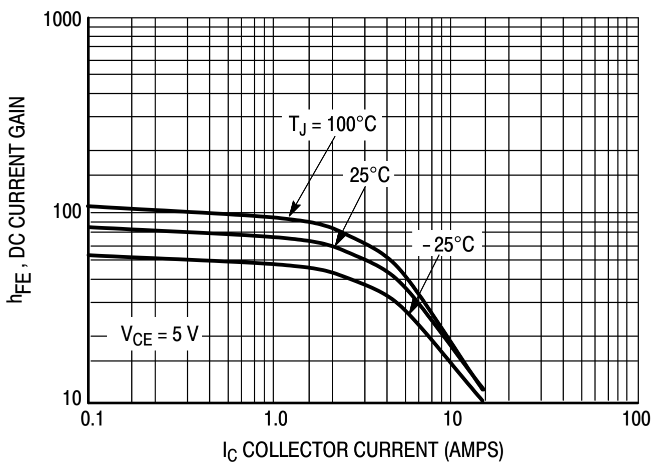


Figure 5. DC Current Gain, V_{CE} = 5 V

NPN MJ21194

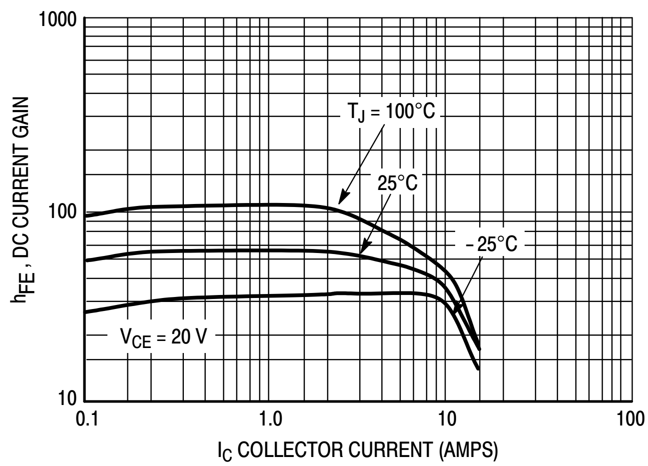


Figure 6. DC Current Gain, V_{CE} = 5 V

PNP MJ21193

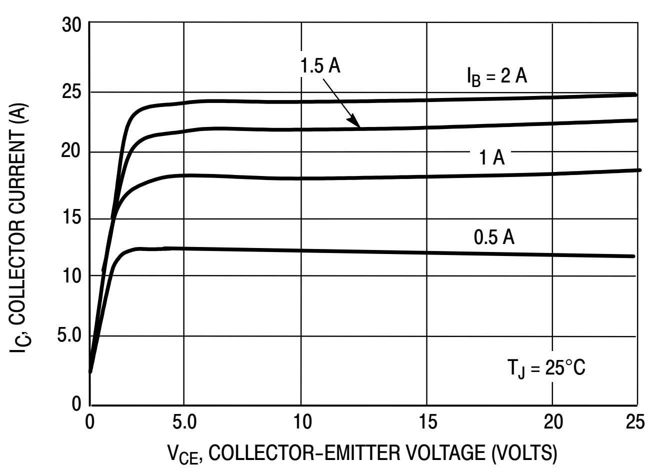


Figure 7. Typical Output Characteristics

NPN MJ21194

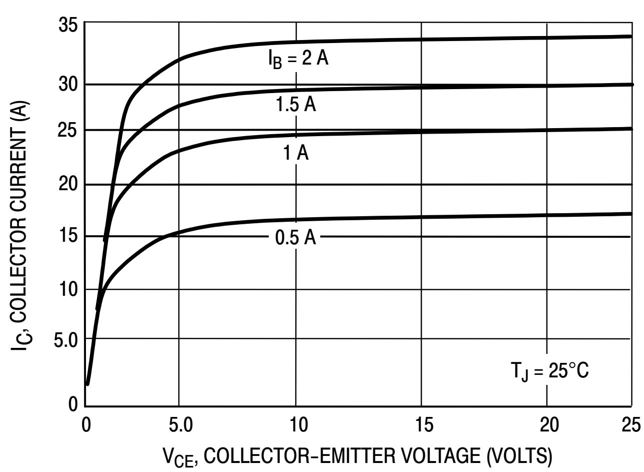


Figure 8. Typical Output Characteristics

TYPICAL CHARACTERISTICS

PNP MJ21193

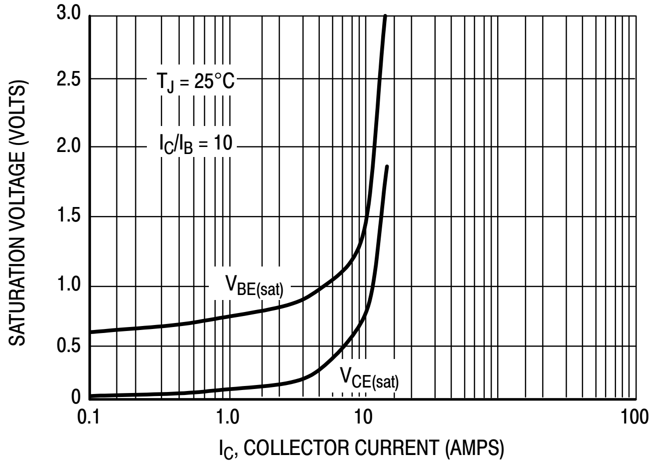


Figure 9. Typical Saturation Voltages

NPN MJ21194

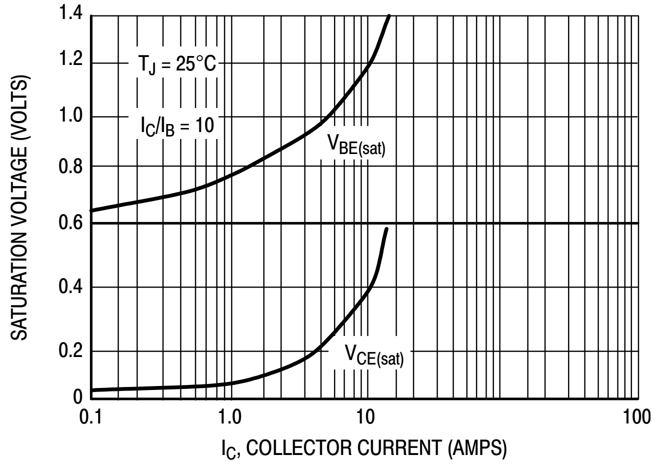


Figure 10. Typical Saturation Voltages

PNP MJ21193

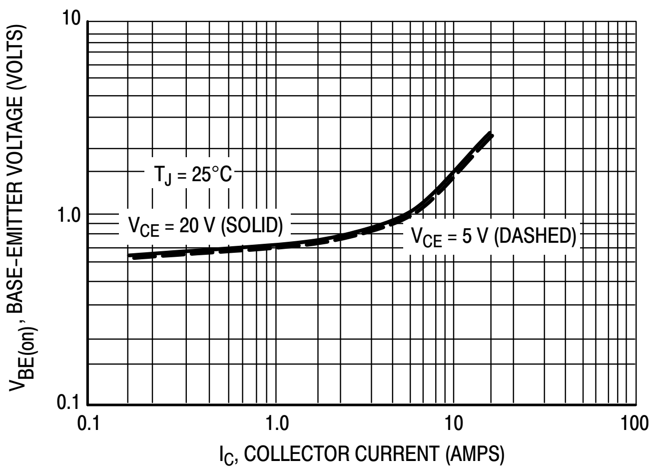


Figure 11. Typical Base−Emitter Voltage

NPN MJ21194

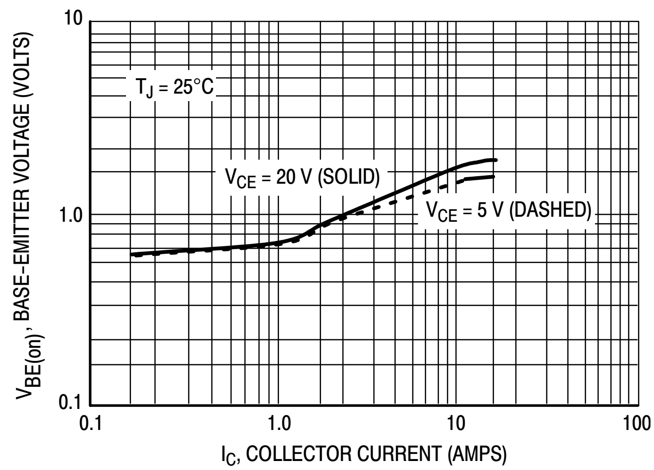


Figure 12. Typical Base−Emitter Voltage

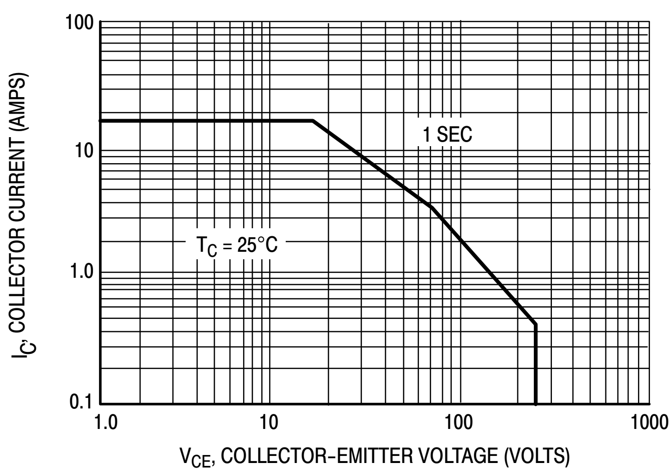


Figure 13. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor; average junction temperature and secondary breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 13 is based on $T_{J(pk)}$ = 200°C; T_C is variable depending on conditions. At high case temperatures, thermal limitations will reduce the power than can be handled to values less than the limitations imposed by second breakdown.

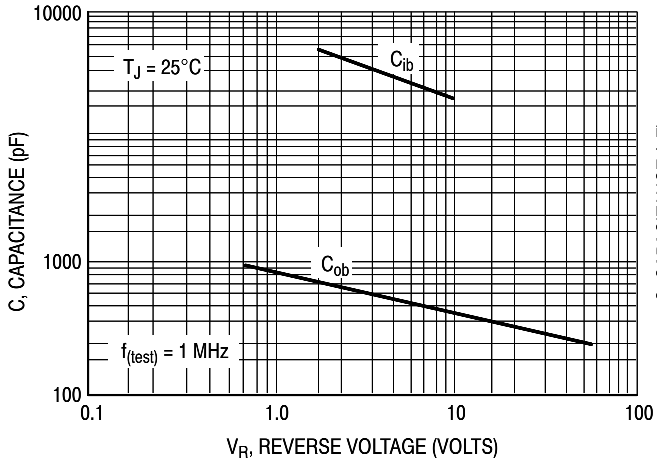


Figure 14. MJ21193 Typical Capacitance

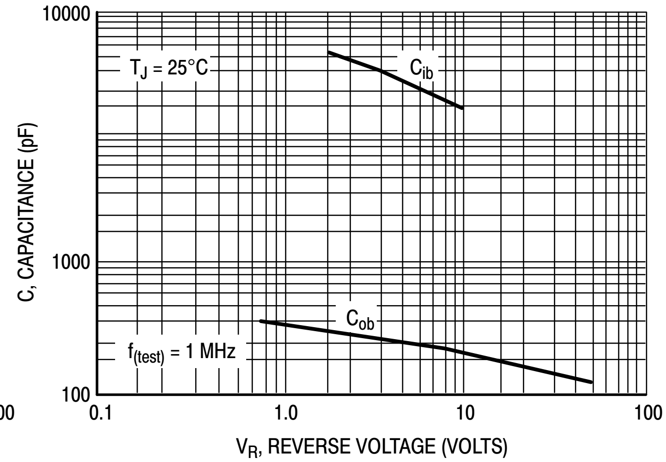


Figure 15. MJ21194 Typical Capacitance

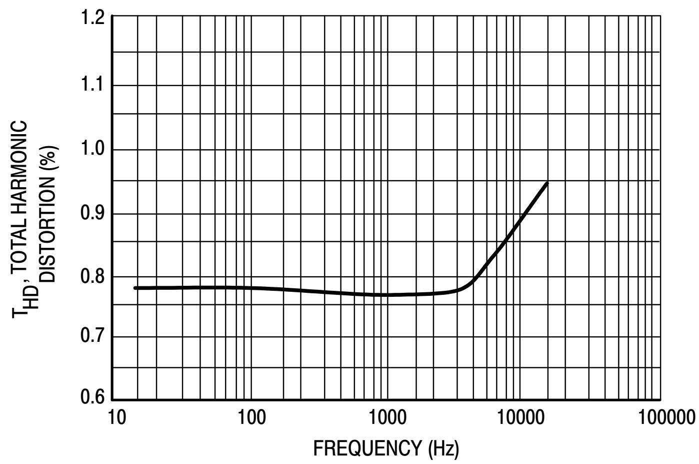


Figure 16. Typical Total Harmonic Distortion

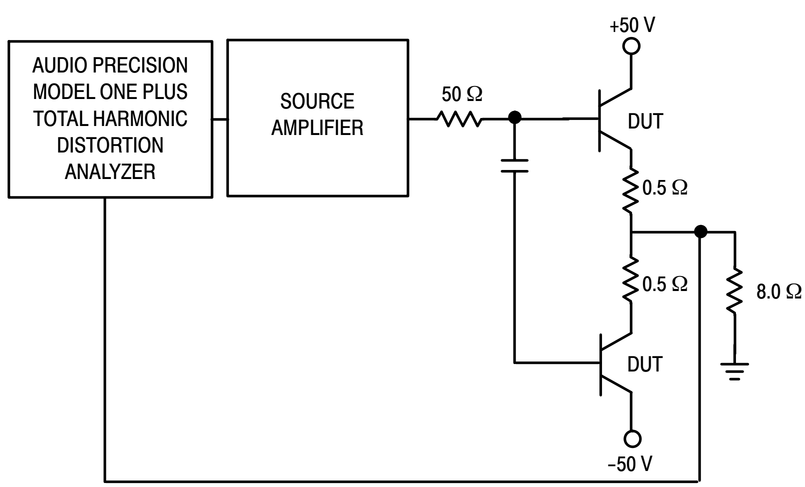
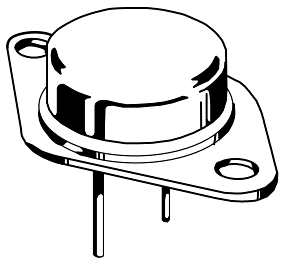


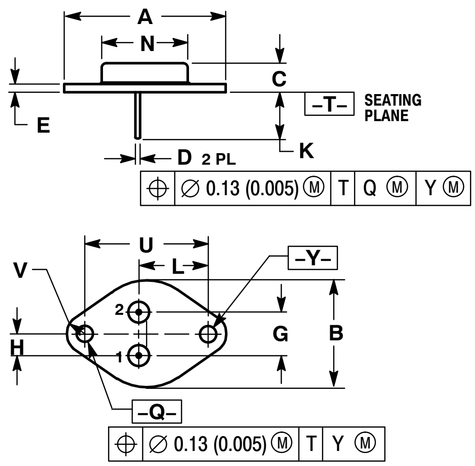
Figure 17. Total Harmonic Distortion Test Circuit



SCALE 1:1

TO−204 (TO−3)
CASE 1−07
ISSUE Z

DATE 10 MAR 2000



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

STYLE 2:
PIN 1. BASE
2. COLLECTOR
CASE: EMITTER

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE: DRAIN

STYLE 4:
PIN 1. GROUND
2. INPUT
CASE: OUTPUT

STYLE 5:
PIN 1. CATHODE
2. EXTERNAL TRIP/DELAY
CASE: ANODE

STYLE 6:
PIN 1. GATE
2. EMITTER
CASE: COLLECTOR

STYLE 7:
PIN 1. ANODE
2. OPEN
CASE: CATHODE

STYLE 8:
PIN 1. CATHODE #1
2. CATHODE #2
CASE: ANODE

STYLE 9:
PIN 1. ANODE #1
2. ANODE #2
CASE: CATHODE

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ADDITIONAL INFORMATION

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