# NPN Silicon Power Darlington Transistors

# MJE5740, MJE5742

The MJE5740 and MJE5742 Darlington transistors are designed for high−voltage power switching in inductive circuits.

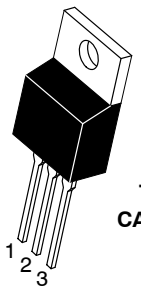
### Features

- These Devices are Pb−Free and are RoHS Compliant*

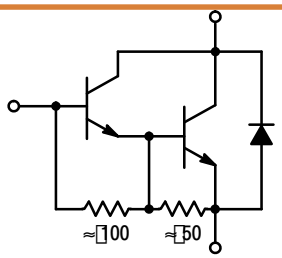
### Applications

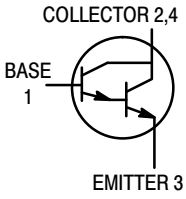
- Small Engine Ignition
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Motor Controls

**POWER DARLINGTON TRANSISTORS**
**8 AMPERES**
**300−400 VOLTS**
**80 WATTS**




**TO−220AB**
**CASE 221A−09**
**STYLE 1**




### MAXIMUM RATINGS

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{CEO(sus)}$ | Collector−Emitter Voltage<br>MJE5740<br>MJE5742 | <br>300<br>400 | Vdc |
| $V_{CEV}$ | Collector−Emitter Voltage<br>MJE5740<br>MJE5742 | <br>600<br>800 | Vdc |
| $V_{EB}$ | Emitter−Base Voltage | 8 | Vdc |
| $I_C$<br>$I_{CM}$ | Collector Current − Continuous<br>− Peak (Note 1) | 8<br>16 | Adc |
| $I_B$<br>$I_{BM}$ | Base Current − Continuous<br>− Peak (Note 1) | 2.5<br>5 | Adc |
| $P_D$ | Total Device Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | 2<br>0.016 | W<br>W/°C |
| $P_D$ | Total Device Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | 100<br>0.8 | W<br>W/°C |
| $T_J$, $T_{stg}$ | Operating and Storage Junction Temperature Range | −65 to +150 | °C |

### THERMAL CHARACTERISTICS

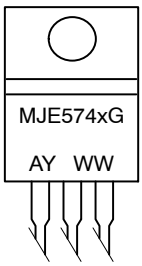
| Symbol | Characteristics | Max | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case | 1.25 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient | 62.5 | °C/W |
| $T_L$ | Maximum Lead Temperature for Soldering Purposes 1/8″ from Case for 5 Seconds | 275 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### MARKING DIAGRAM




| | | |
|---|---|---|
| MJE574x | = | Device Code<br>x = 0 or 2 |
| G | = | Pb−Free Package |
| A | = | Assembly Location |
| Y | = | Year |
| WW | = | Work Week |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Symbol | Characteristic | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{CEO(sus)}$ | Collector−Emitter Sustaining Voltage ($I_C$ = 50 mA, $I_B$ = 0) | MJE5740<br>MJE5742 | 300<br>400 | –<br>– | –<br>– | Vdc |
| $I_{CEV}$ | Collector Cutoff Current ($V_{CEV}$ = Rated Value, $V_{BE(off)}$ = 1.5 Vdc)<br>($V_{CEV}$ = Rated Value, $V_{BE(off)}$ = 1.5 Vdc, $T_C$ = 100°C) | | –<br>– | –<br>– | 1<br>5 | mAdc |
| $I_{EBO}$ | Emitter Cutoff Current ($V_{EB}$ = 8 Vdc, $I_C$ = 0) | | – | – | 75 | mAdc |
| **SECOND BREAKDOWN** | | | | | | |
| $I_{S/b}$ | Second Breakdown Collector Current with Base Forward Biased | | See Figure 6 | | | |
| RBSOA | Clamped Inductive SOA with Base Reverse Biased | | See Figure 7 | | | |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $h_{FE}$ | DC Current Gain ($I_C$ = 0.5 Adc, $V_{CE}$ = 5 Vdc)<br>($I_C$ = 4 Adc, $V_{CE}$ = 5 Vdc) | | 50<br>200 | 100<br>400 | –<br>– | – |
| $V_{CE(sat)}$ | Collector−Emitter Saturation Voltage ($I_C$ = 4 Adc, $I_B$ = 0.2 Adc)<br>($I_C$ = 8 Adc, $I_B$ = 0.4 Adc)<br>($I_C$ = 4 Adc, $I_B$ = 0.2 Adc, $T_C$ = 100°C) | | –<br>–<br>– | –<br>–<br>– | 2<br>3<br>2.2 | Vdc |
| $V_{BE(sat)}$ | Base−Emitter Saturation Voltage ($I_C$ = 4 Adc, $I_B$ = 0.2 Adc)<br>($I_C$ = 8 Adc, $I_B$ = 0.4 Adc)<br>($I_C$ = 4 Adc, $I_B$ = 0.2 Adc, $T_C$ = 100°C) | | –<br>–<br>– | –<br>–<br>– | 2.5<br>3.5<br>2.4 | Vdc |
| $V_f$ | Diode Forward Voltage (Note 3) ($I_F$ = 5 Adc) | | – | – | 2.5 | Vdc |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| **Typical Resistive Load** (Table 1) | | | | | | |
| $t_d$ | Delay Time | ($V_{CC}$ = 250 Vdc, $I_{C(pk)}$ = 6 A<br>$I_{B1}$ = $I_{B2}$ = 0.25 A, $t_p$ = 25 μs,<br>Duty Cycle ≤ 1%) | – | 0.04 | – | μs |
| $t_r$ | Rise Time | | – | 0.5 | – | μs |
| $t_s$ | Storage Time | | – | 8 | – | μs |
| $t_f$ | Fall Time | | – | 2 | – | μs |
| **Inductive Load, Clamped** (Table 1) | | | | | | |
| $t_{sv}$ | Voltage Storage Time | ($I_{C(pk)}$ = 6 A, $V_{CE(pk)}$ = 250 Vdc<br>$I_{B1}$ = 0.06 A, $V_{BE(off)}$ = 5 Vdc) | – | 4 | – | μs |
| $t_c$ | Crossover Time | | – | 2 | – | μs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: Pulse Width 300 μs, Duty Cycle = 2%.
3. The internal Collector−to−Emitter diode can eliminate the need for an external diode to clamp inductive loads. Tests have shown that the Forward Recovery Voltage ($V_f$) of this diode is comparable to that of typical fast recovery rectifiers.

## TYPICAL CHARACTERISTICS

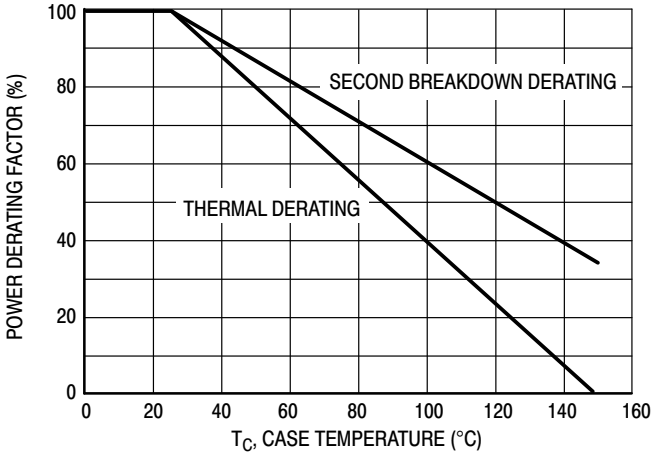



**Figure 1. Power Derating**

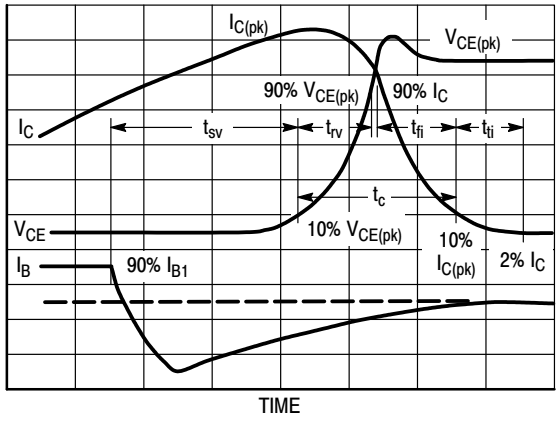



**Figure 2. Inductive Switching Measurements**

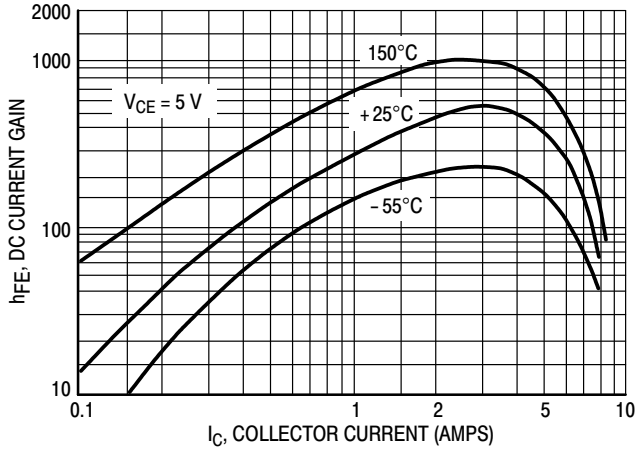



**Figure 3. DC Current Gain**

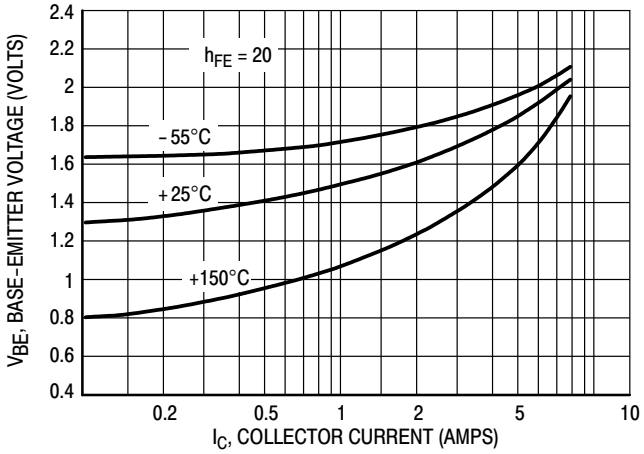



**Figure 4. Base−Emitter Voltage**

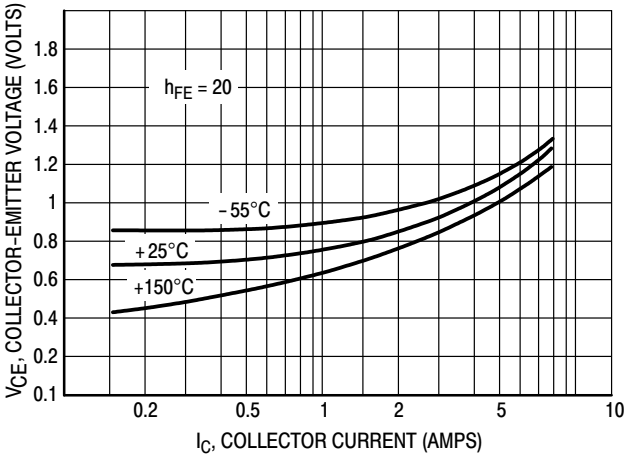
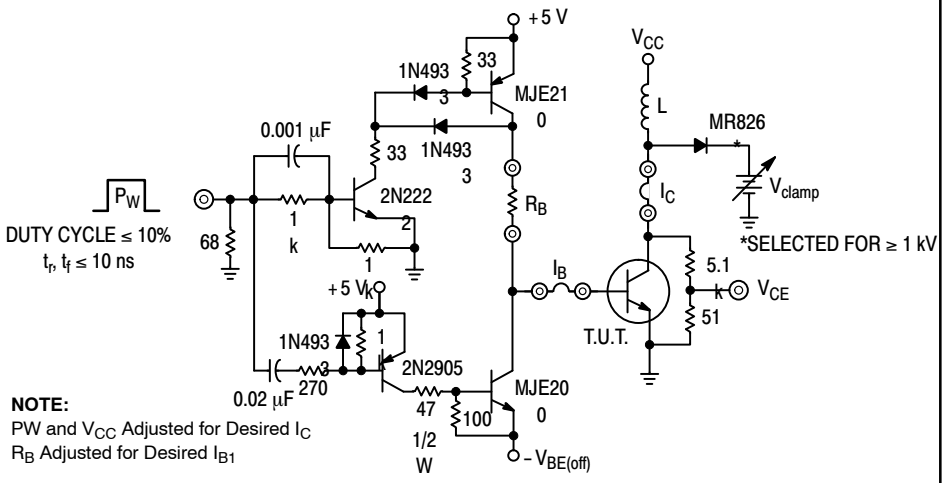
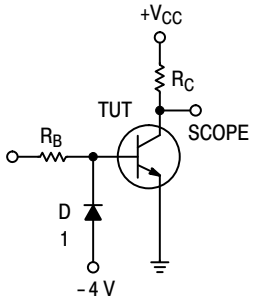
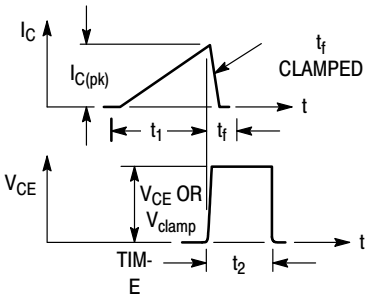
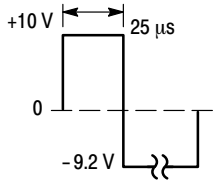



**Figure 5. Collector−Emitter Saturation Voltage**

**Table 1. Test Conditions for Dynamic Performance**

| | REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING | RESISTIVE SWITCHING |
|---|---|---|
| TEST CIRCUITS |  |  |
| CIRCUIT VALUES | COIL DATA:<br>FERROXCUBE CORE #6656<br>FULL BOBBIN (~16 TURNS) #16<br>GAP FOR 200 μH/20 A<br>$L_{coil}$ = 200 μH<br>$V_{CC}$ = 30 V<br>$V_{CE(pk)}$ = 250 Vdc<br>$I_{C(pk)}$ = 6 A | $V_{CC}$ = 250 V<br>D1 = 1N5820 OR EQUIV. |
| TEST WAVEFORMS | OUTPUT WAVEFORMS<br>  <br>$t_1$ ADJUSTED TO OBTAIN $I_C$<br>$t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$<br>$t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{clamp}}$<br>TEST EQUIPMENT<br>SCOPE-TEKTRONICS<br>475 OR EQUIVALENT |  <br>$t_r$, $t_f$ < 10 ns<br>DUTY CYCLE = 1%<br>$R_B$ AND $R_C$ ADJUSTED FOR DESIRED $I_B$ AND $I_C$ |

## SAFE OPERATING AREA INFORMATION

### FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_C = 25°C$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25°C$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 6 may be found at any case temperature by using the appropriate curve on Figure 1.

### REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn−off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage−current condition allowable during reverse biased turnoff. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 7 gives the complete RBSOA characteristics.

**The Safe Operating Area figures shown in Figures 6 and 7 are specified ratings for these devices under the test conditions shown.**

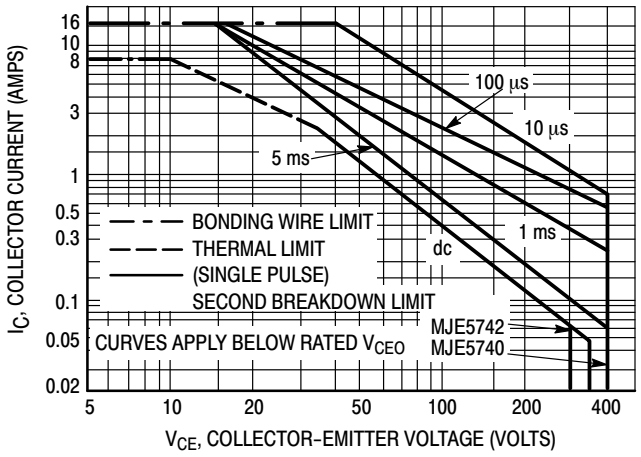



**Figure 6. Forward Bias Safe Operating Area**

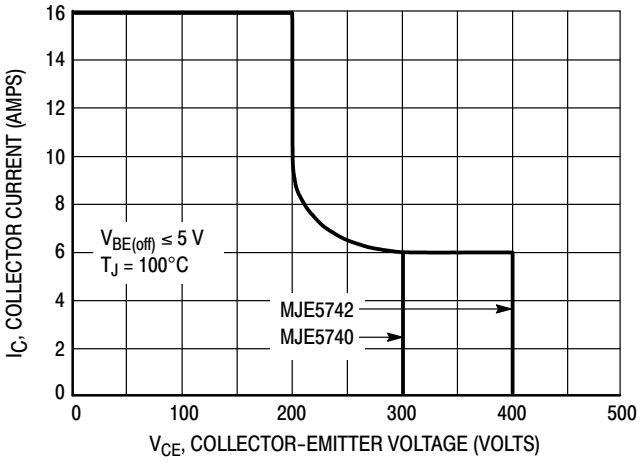



**Figure 7. Reverse Bias Safe Operating Area**

## RESISTIVE SWITCHING PERFORMANCE

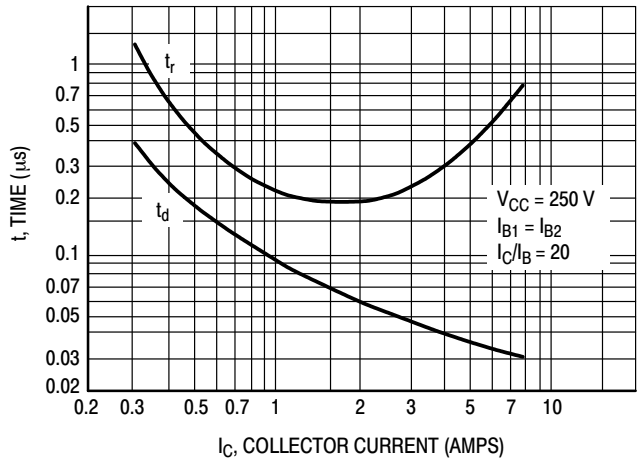



**Figure 8. Turn−On Time**

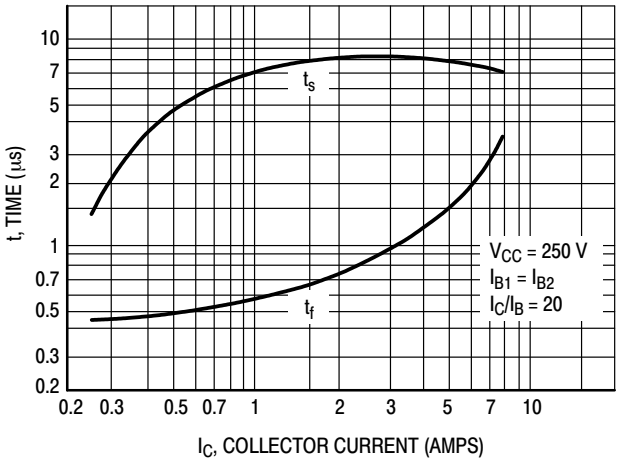



**Figure 9. Turn−Off Time**

## ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| MJE5742G | TO−220<br>(Pb−Free) | 50 Units / Rail |

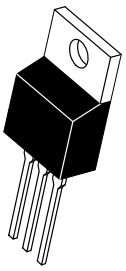
**DISCONTINUED** (Note 4)

| | | |
|---|---|---|
| MJE5740G | TO−220<br>(Pb−Free) | 50 Units / Rail |

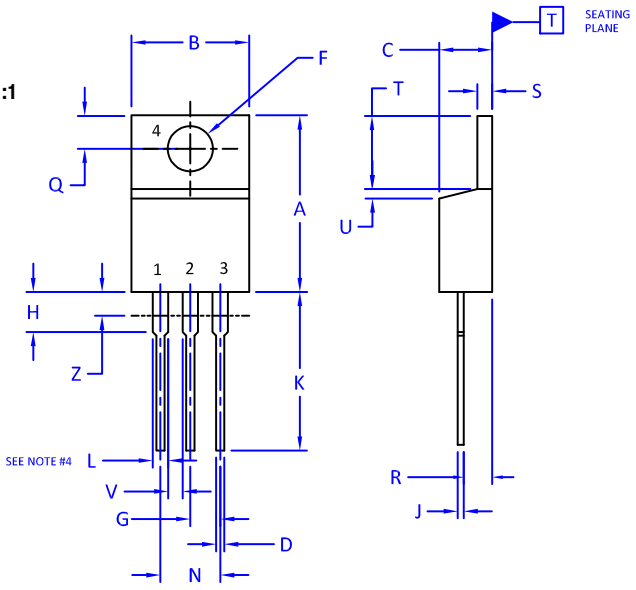
4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

**TO−220**
CASE 221A
ISSUE AK

DATE 13 JAN 2022



**SCALE 1:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN. | MAX. | MIN. | MAX. |
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.415 | 9.66 | 10.53 |
| C | 0.160 | 0.190 | 4.07 | 4.83 |
| D | 0.025 | 0.038 | 0.64 | 0.96 |
| F | 0.142 | 0.161 | 3.60 | 4.09 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.161 | 2.80 | 4.10 |
| J | 0.014 | 0.024 | 0.36 | 0.61 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.41 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | ---- | 1.15 | --- |
| Z | ---- | 0.080 | --- | 2.04 |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42148B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| **DESCRIPTION:** | **TO−220** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales