

Quad 2-Input NAND Gate

MM74HCT00

General Description

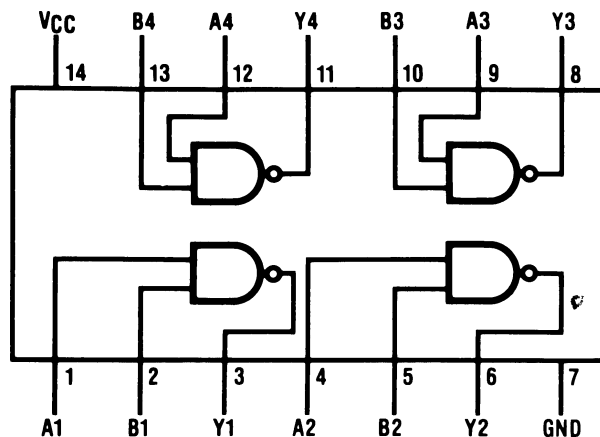
The MM74HCT00 is a NAND gates fabricated using advanced silicon-gate CMOS technology which provides the inherent benefits of CMOS—low quiescent power and wide power supply range. This device is input and output characteristic and pin-out compatible with standard 74LS logic families. All inputs are protected from static discharge damage by internal diodes to VCC and ground.

MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

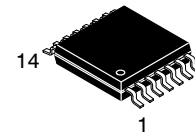
- TTL, LS Pin-out and Threshold Compatible
- Fast Switching: t_{PLH} , t_{PHL} = 14 ns (typ.)
- Low Power: 5 μ W at DC
- High Fan Out, 10 LS-TTL Loads
- This Device is Pb-Free and Halide Free

Connection Diagram



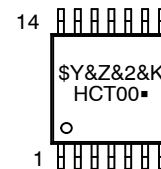
Top View

Figure 1. Pin Assignments for TSSOP



TSSOP-14,
CASE 948G

MARKING DIAGRAM

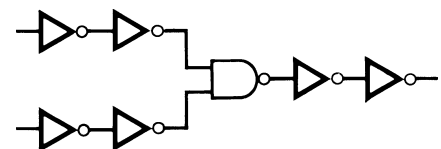


\$Y	= Logo
&Z	= Assembly Plant Code
&2	= 2-Digit Date Code (Year and Week)
&K	= 2-Digit Lot Run Traceability Code
HCT00	= Device Code

(Note: Microdot may be in either location)

LOGIC DIAGRAM

(1 of 4 gates)



ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

MM74HCT00

ABSOLUTE MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Rating	Unit
V_{CC}	Supply Voltage	-0.5 to +7.0	V
V_{IN}	DC Input Voltage	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage	-0.5 to V_{CC} +0.5	V
I_{IK}, I_{OK}	Clamp Diode Current	±20	mA
I_{OUT}	DC Output Current, per pin	±25	mA
I_{CC}	DC V_{CC} or GND Current, per pin	±50	mA
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
V_{IN}, V_{OUT}	DC Input or Output Voltage	0	V_{CC}	V
T_A	Operating Temperature Range	-55	+125	°C
t_r, t_f	Input Rise or Fall Times	–	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

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DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{ V} \pm 10\%$ (unless otherwise specified))

Symbol	Parameter	Conditions	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Unit
			Typ.	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		–	2.0	2.0	2.0	V
V _{IL}	Maximum LOW Level Input Voltage		–	0.8	0.8	0.8	V
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 20 μA	V _{CC}	V _{CC} – 0.1	V _{CC} – 0.1	V _{CC} – 0.1	V
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4.0 mA, V _{CC} = 4.5 V	4.2	3.98	3.84	3.7	
		V _{IN} = V _{IH} or V _{IL} , I _{OUT} = 4.8 mA, V _{CC} = 5.5 V	5.2	4.98	4.84	4.7	
V _{OL}	Maximum LOW Level Voltage	V _{IN} = V _{IH} I _{OUT} = 20 μA	0	0.1	0.1	0.1	V
		V _{IN} = V _{IH} I _{OUT} = 4.0 mA V _{CC} = 4.5 V	0.2	0.26	0.33	0.4	
		V _{IN} = V _{IH} I _{OUT} = 4.8 mA V _{CC} = 5.5 V	0.2	0.26	0.33	0.4	
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND, V _{IH} or V _{IL}	–	±0.05	±0.5	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND, I _{OUT} = 0 μA	–	1.0	10	40	μA
		V _{IN} = 2.4 V or 0.5 V (Note 2)	0.18	0.3	0.4	0.5	mA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. This is measured per input with all other inputs held at V_{CC} or ground.

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AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0\text{ V}$, $t_r = t_f = 6\text{ ns}$, $C_L = 15\text{ pF}$, $T_A = 25^\circ\text{C}$ (unless otherwise specified))

Symbol	Parameter	Conditions	Typ.	Guaranteed Limit	Unit
t_{PLH} , t_{PHL}	Maximum Propagation Delay		14	18	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

($V_{CC} = 5.0\text{ V} \pm 10\%$, $t_r = t_f = 6\text{ ns}$, $C_L = 50\text{ pF}$ (unless otherwise specified))

Symbol	Parameter	Conditions	T _A = 25°C		T _A = -40°C to 85°C	T _A = -55°C to 125°C	Unit
			Typ.	Guaranteed Limits			
t _{PLH} , t _{PHL}	Maximum Propagation Delay		18	23	29	35	ns
t _{THL} , t _{TLH}	Maximum Output Rise and Fall Time		8	15	19	22	ns
C _{PD}	Power Dissipation Capacitance	(Note 3)	30	–	–	–	pF
C _{IN}	Input Capacitance		5	10	10	10	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

ORDERING INFORMATION

Device	Package	Shipping [†]
MM74HCT00MTCX	TSSOP-14 WB, Case 948G (Pb-Free and Halide Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

NOTE: All packages are lead free per JEDEC: J-STD-020B standard.

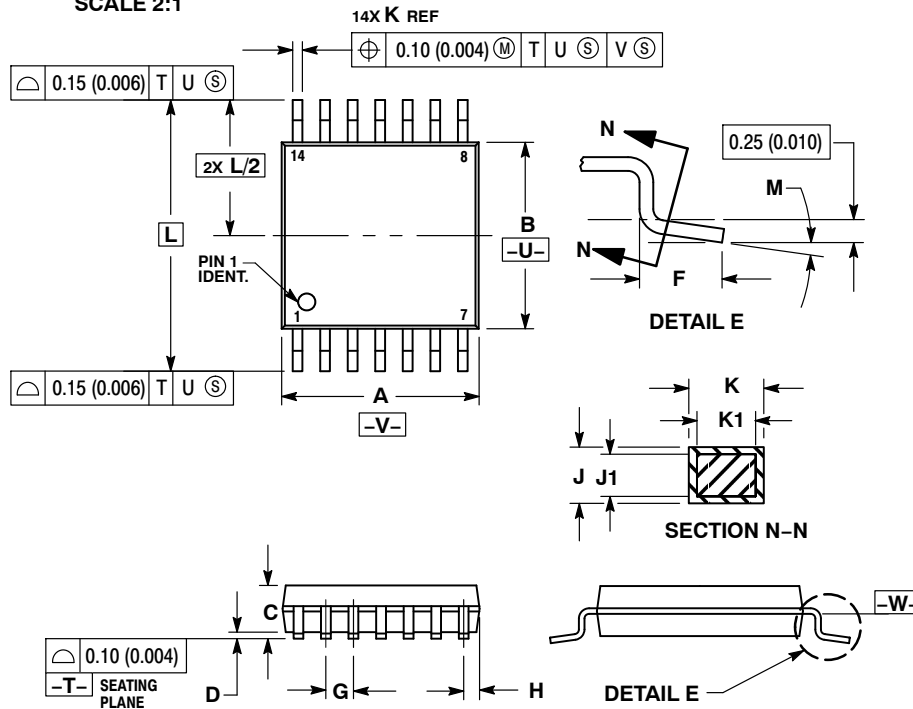
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1

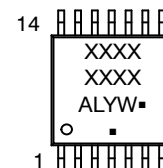


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

GENERIC MARKING DIAGRAM*



- A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

SOLDERING FOOTPRINT



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DESCRIPTION: TSSOP-14 WB

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