2 GHz – 26 GHz GaAs Distributed Self-Biased MMIC LNA

MMA042PP4

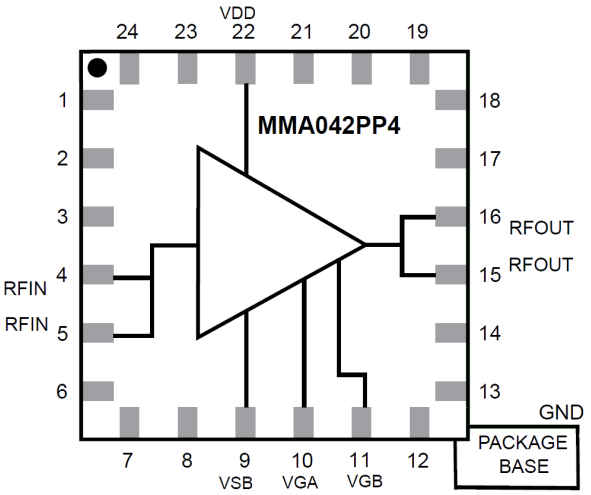
Product Overview

MMA042PP4 is a Gallium Arsenide (GaAs) Monolithic Microwave Integrated Circuit (MMIC) Pseudomorphic High-Electron Mobility Transistor (pHEMT) distributed amplifier that operates between 2 GHz and 26 GHz. It is ideal for test instrumentation, defense, and space applications. The amplifier provides a 2 dB positive gain slope with a typical gain of 18 dB, 2.5 dB noise figure, 18 dBm of output power at 1 dB gain compression, and 29 dBm output IP3 at 10 GHz. The MMA042PP4 amplifier features RF I/O's that are internally matched to 50Ω.

Key Features

- Frequency range: 2 GHz to 26 GHz
- High Gain: 18 dB with +2 dB upslope
- Low Noise figure: 2.5 dB
- High Output IP3: +29 dBm
- Maximum RF Input Power: +24 dBm
- Single Positive Supply: 5V thru 7V – Typical = +6V at 120 mA
- ESD Protection on RF and DC ports
- 50Ω matched input/output
- Analog gain adjustment [Temp Comp]
- QFN 4 mm × 4 mm Plastic Package

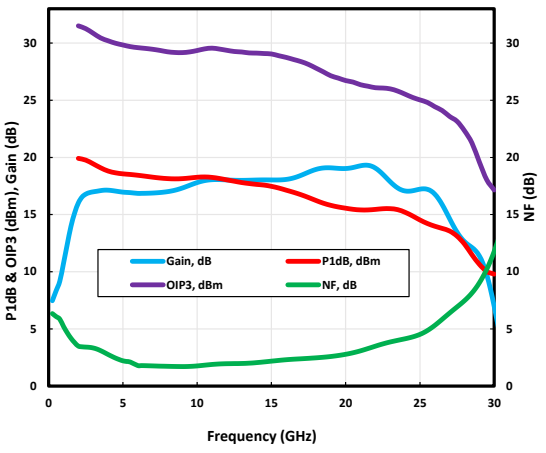
Functional Block Diagram



Applications

- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military, A&D, space, SATCOM
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

Gain, OIP3, and NF Performances



Performance Overview

Parameter	Typ.	Units
Operational frequency range	2 – 26	GHz
Gain	18	dB
OIP3	29	dBm
NF	2.5	dB
Current at +6V supply	120	mA

Export Classification: EAR–99

Table of Contents

1. Electrical Specifications

1.1 Typical Electrical Performance

Table 1-1. Typical Electrical Performance at 25 °C, V_{dd} = + 6V, I_{dd} = 120 mA (Unless otherwise mentioned)

Parameter	Frequency Range	Min	Typ.	Max	Units
Frequency range		2		26	GHz
Gain	2 GHz – 8 GHz	16	17		dB
	8 GHz – 16 GHz	17	18		
	16 GHz – 22 GHz	17	19		
	22 GHz – 26 GHz	16	18		
Gain flatness	2 GHz – 6 GHz		± 0.75		dB
	6 GHz –12 GHz		± 0.75		
	12 GHz – 22 GHz		± 0.75		
	22 GHz – 26 GHz		± 1.0		
Noise figure	2 GHz – 6 GHz		3.0	4	dB
	6 GHz – 12 GHz		2.5	3	
	12 GHz – 22 GHz		3	3.5	
	22 GHz – 26 GHz		4	5	
Input return loss	2 GHz – 8 GHz	11	12		dB
	8 GHz – 16 GHz	11	13		
	16 GHz – 22 GHz	10	12		
	22 GHz – 26 GHz	6	7.5		
Output return loss	2 GHz – 8 GHz	10	12		dB
	8 GHz – 16 GHz	10	12		
	16 GHz – 22 GHz	11	13		
	22 GHz – 26 GHz	7	8		
P1dB	2 GHz – 6 GHz	17	18		dBm
	6 GHz – 12 GHz	16	18		
	12 GHz – 22 GHz	14	16		
	22 GHz – 26 GHz	13	15		
P_{sat}(measured at 3 dB gain compression)	2 GHz – 6 GHz		21		dBm
	6 GHz – 12 GHz		20		
	12 GHz – 22 GHz		18		
	22 GHz – 26 GHz		17		
OIP3	2 GHz – 6 GHz	28	29		dBm
	6 GHz – 12 GHz	27	28		
	12 GHz – 22 GHz	25	26		
	22 GHz – 26 GHz	24	25		
V_{DD} (drain voltage supply)			+6		V
I_{DD} (drain current)			120		mA

1.2 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the MMA042PP4 device at 25 °C, unless otherwise specified. Exceeding one or any of the maximum ratings potentially could cause damage or latent defects to the device.

Table 1-2. Absolute Maximum Ratings

Parameter	Rating
Drain bias voltage (V_{DD})	8V
Gate bias voltage (V_G)	–2V to + 0.5V
RF input power (Pin)	24 dBm
Channel temperature	150 °C
V_{DD} Current (I_{DD})	200 mA
DC power dissipation (T = 85 °C)	1.6W
Thermal resistance	17 °C/W
Storage temperature	–65 °C to + 150 °C
Operating temperature	–55 °C to + 85 °C

ESD Sensitive Device

1.3 Typical Performance Curves

1.3.1 Typical Performances vs. Temperature

The graphs shown in Figures 1-1 through 1-30 represent the Typical Performance of MMA042PP4 device at specific bias conditions. All measurements were taken using board shown in Figure 3–3.

Figure 1-1. Gain vs. Temperature at 5V/100 mA

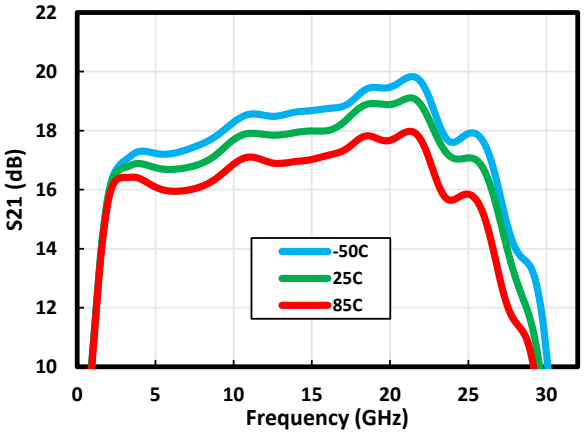


Figure 1-2. Gain vs. Temperature at 6V/120 mA

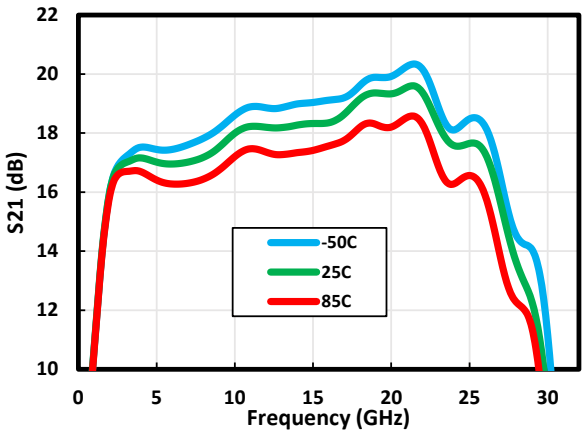


Figure 1-3. Gain vs. Temperature at 7V/130 mA

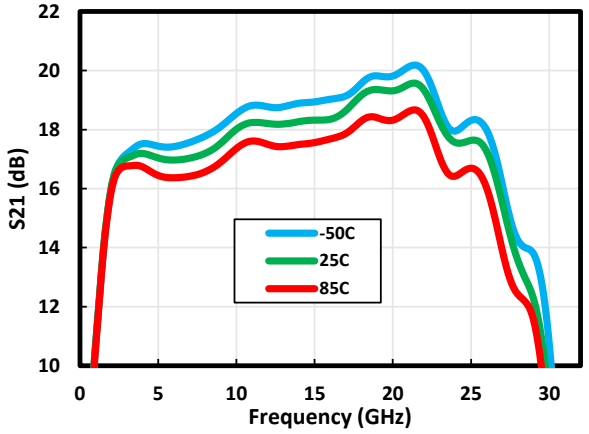


Figure 1-4. S11 vs. Temperature at 5V/100 mA

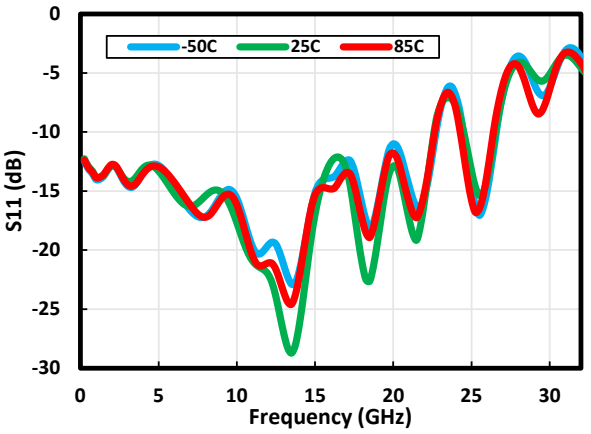


Figure 1-5. S11 vs. Temperature at 6V/120 mA

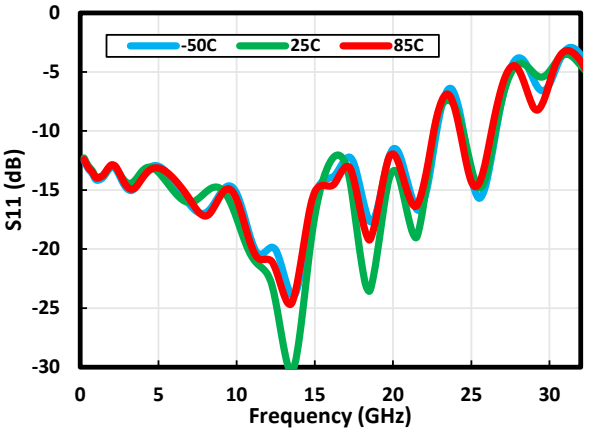


Figure 1-6. S11 vs. Temperature at 7V/130 mA

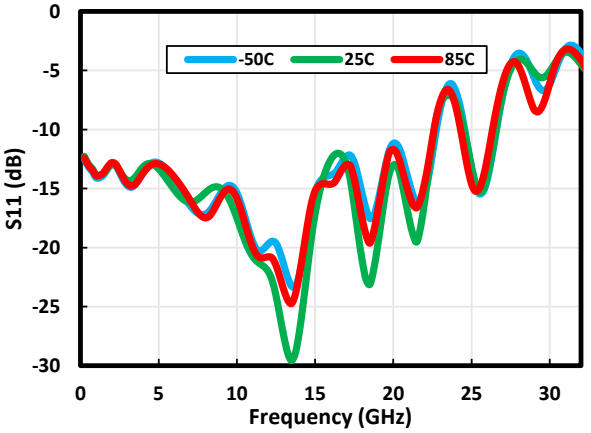


Figure 1-7. S22 vs. Temperature at 5V/100 mA

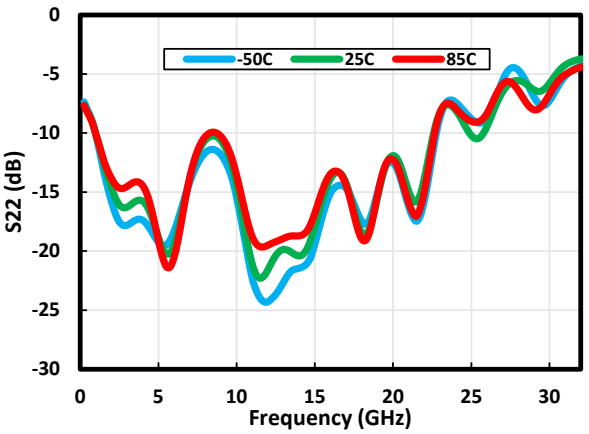


Figure 1-8. S22 vs. Temperature at 6V/120 mA

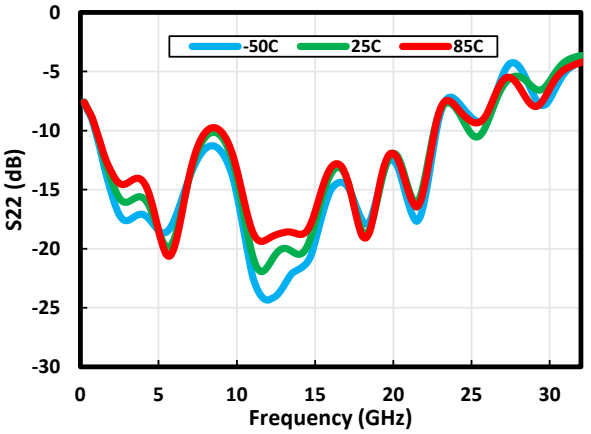


Figure 1-9. S22 vs. Temperature at 7V/130 mA

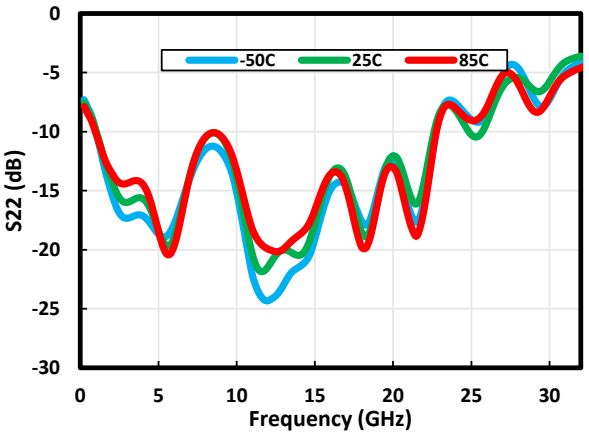


Figure 1-10. S12 vs. Temperature at 5V/100 mA

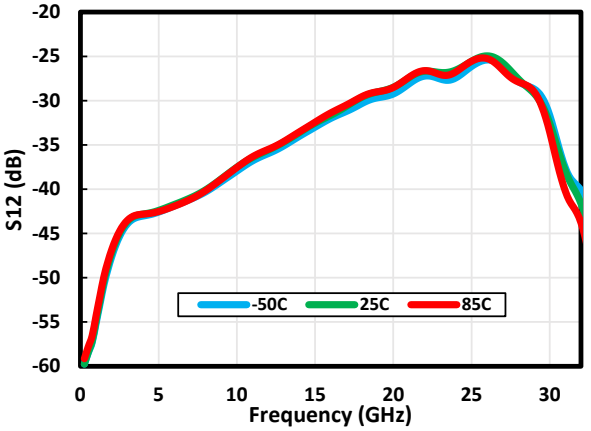


Figure 1-11. S12 vs. Temperature at 6V/120 mA

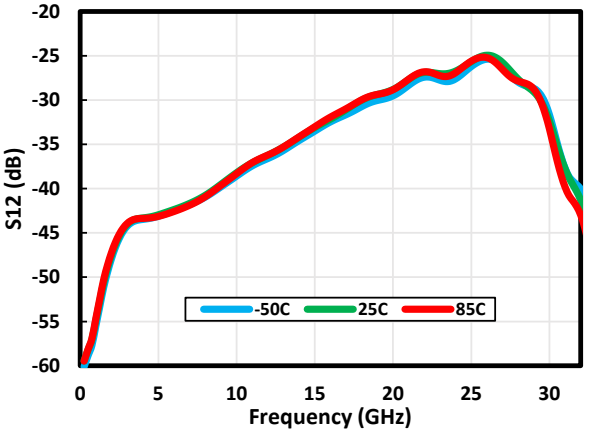


Figure 1-12. S12 vs. Temperature at 7V/130 mA

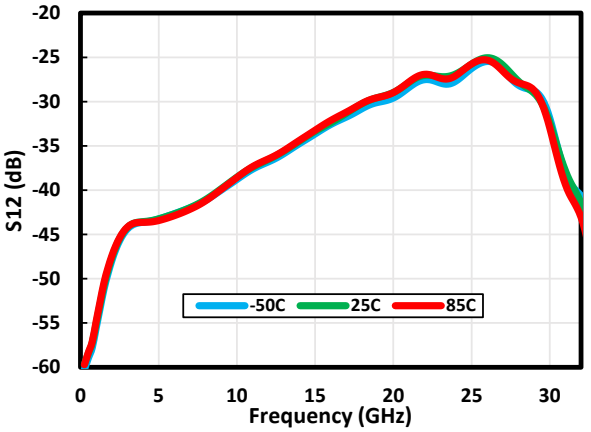


Figure 1-13. NF vs. Temperature at 5V/100 mA

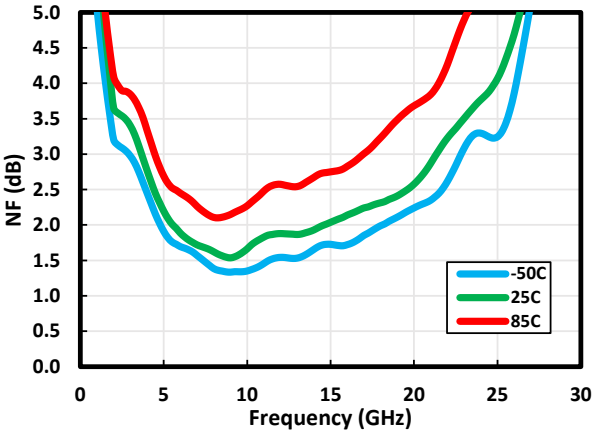


Figure 1-14. NF vs. Temperature at 6V/120 mA

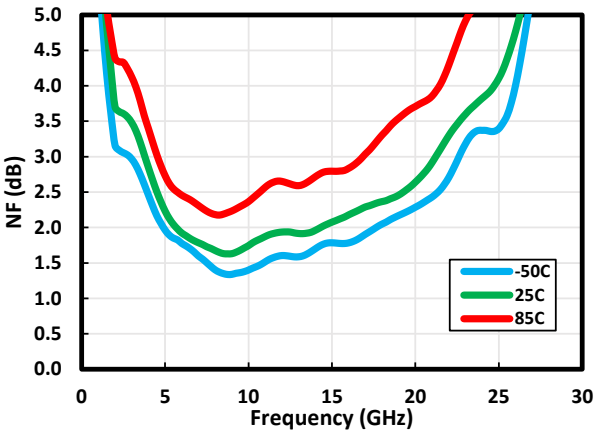


Figure 1-15. NF vs. Temperature at 7V/130 mA

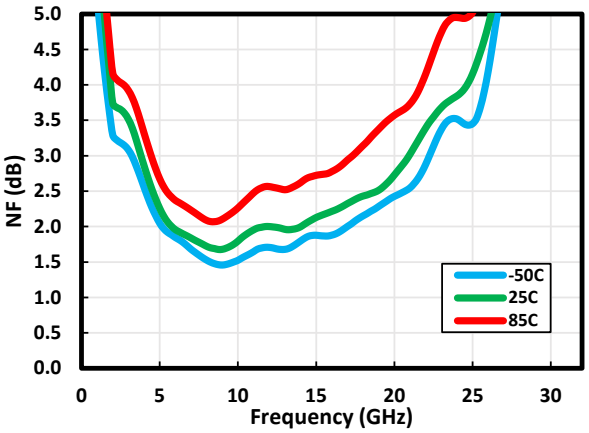


Figure 1-16. P1dB vs. Temperature at 5V/100 mA

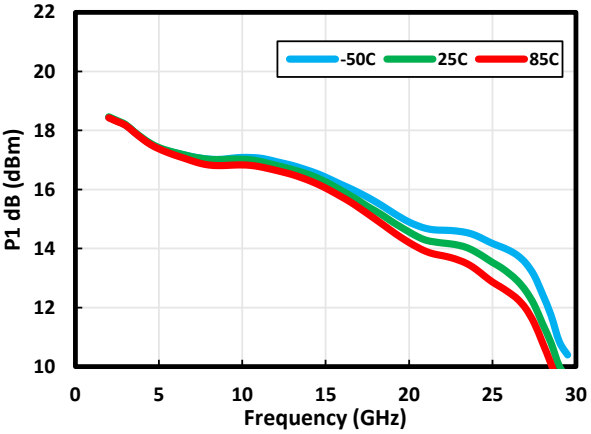


Figure 1-17. P1dB vs. Temperature at 6V/120 mA

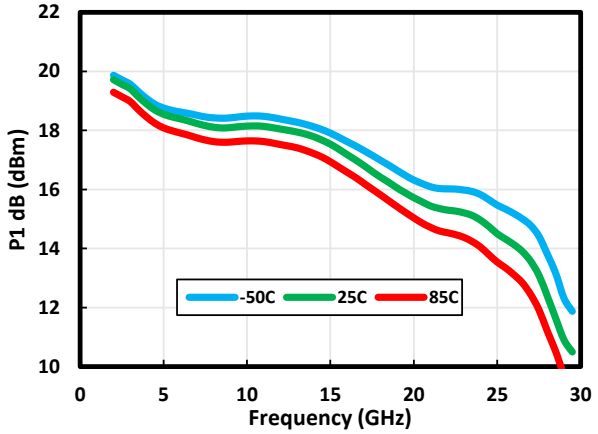


Figure 1-18. P1dB vs. Temperature at 7V/130 mA

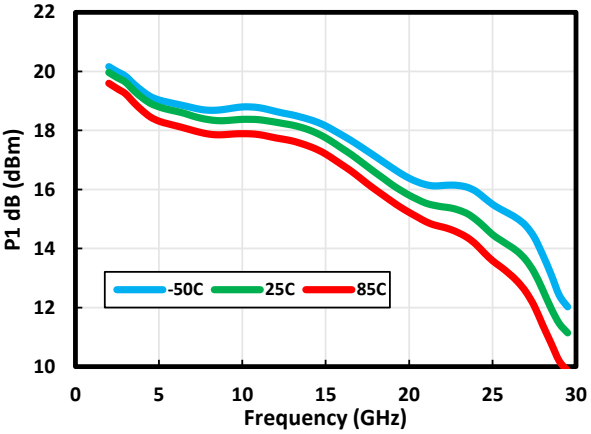


Figure 1-19. P_{sat} vs. Temperature at 5V/100 mA

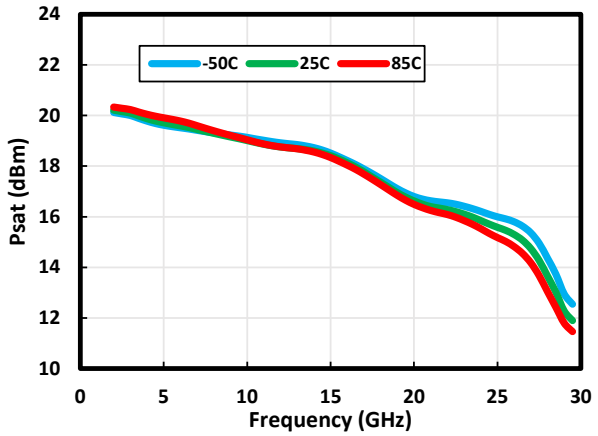


Figure 1-20. P_{sat} vs. Temperature at 6V/120 mA

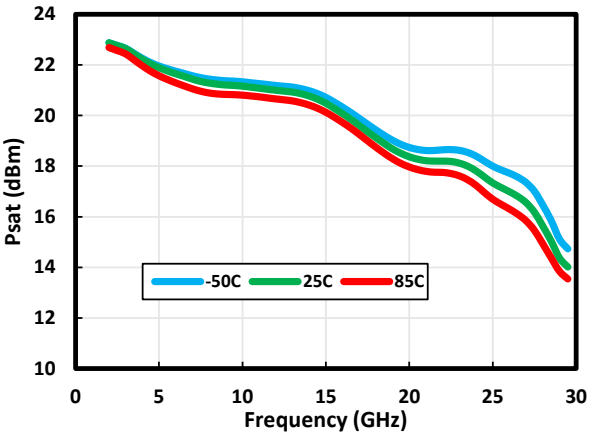


Figure 1-21. P_{sat} vs. Temperature at 7V/130 mA

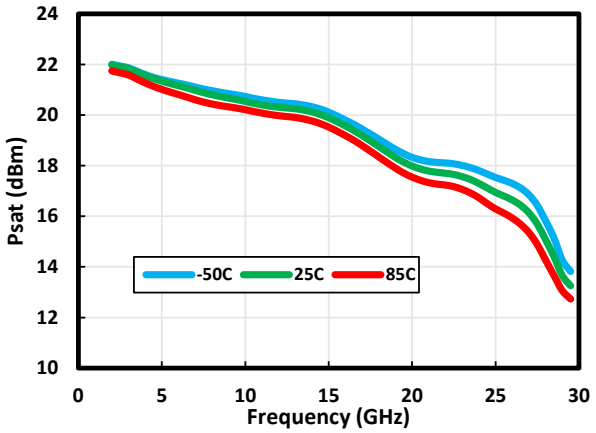


Figure 1-22. OIP3 vs. Temperature at 5V/100 mA

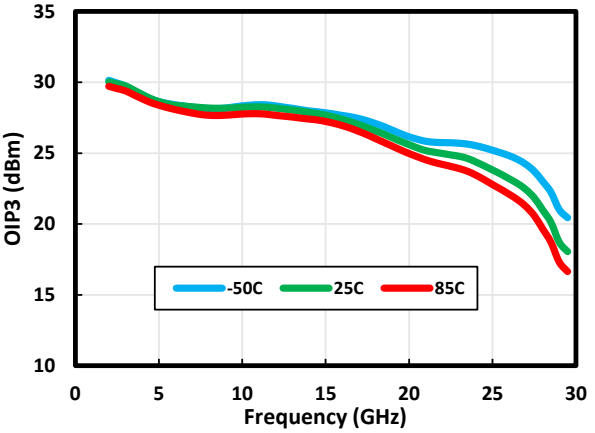


Figure 1-23. OIP3 vs. Temperature at 6V/120 mA

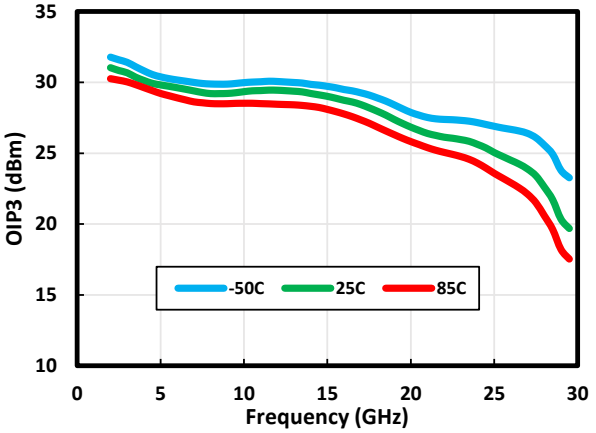


Figure 1-24. OIP3 vs. Temperature at 7V/130 mA

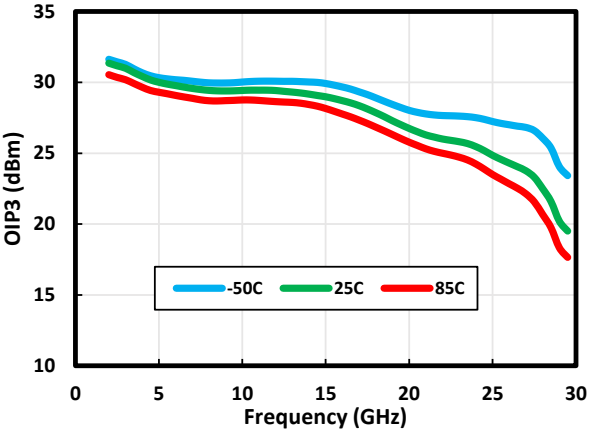


Figure 1-25. OIP2(low) vs. Temperature at 5V/100 mA

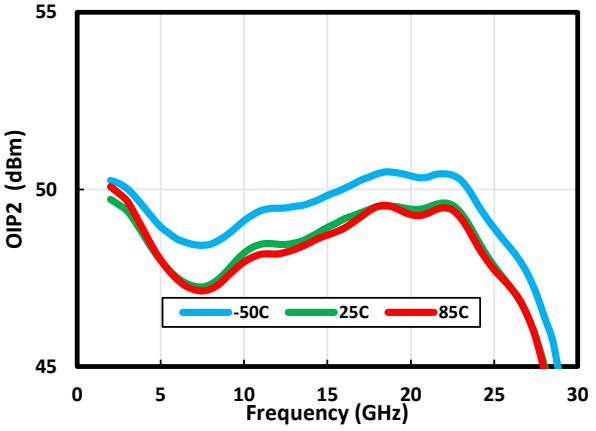


Figure 1-26. OIP2(low) vs. Temperature at 6V/120 mA

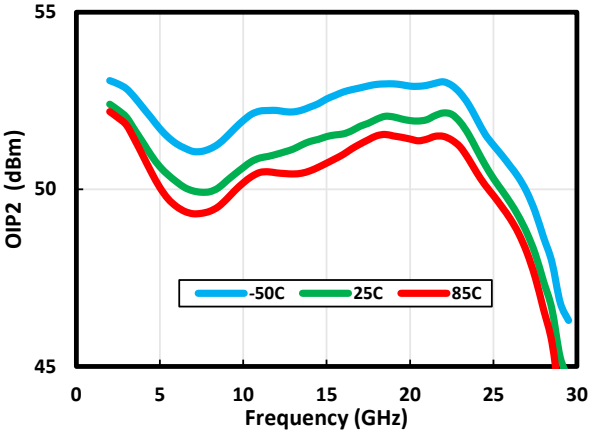


Figure 1-27. OIP2(low) vs. Temperature at 7V/140 mA

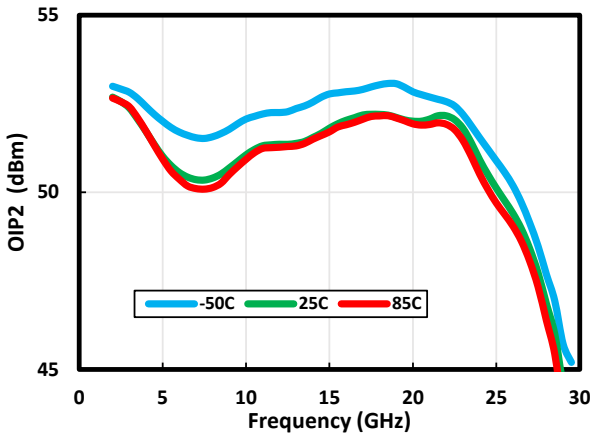


Figure 1-28. IM3 vs. Temperature at 5V/100mA, 10 dBm (per tone)

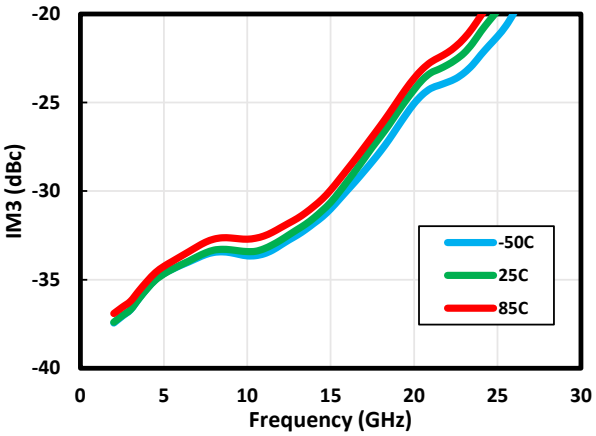


Figure 1-29. IM3 vs. Temperature at 6V/120 mA, 10 dBm (per tone)

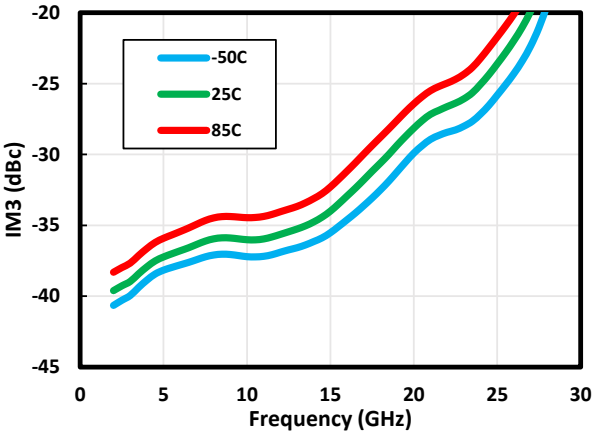
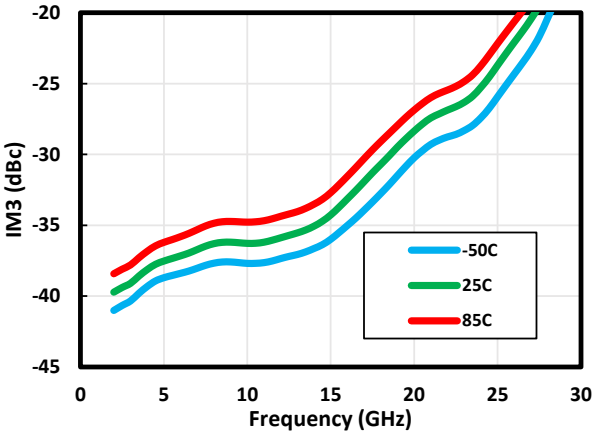


Figure 1-30. IM3 vs. Temperature at 7V/140 mA, 10 dBm (per tone)



1.3.2 Typical Performance vs. Bias

The graphs shown in Figures 1–31 through 1–43 represent the Typical Performance of MMA042PP4 device at specific bias conditions. All measurements were taken using board shown in Figure 3–3.

Figure 1-31. Gain vs. V_{DD} at 100 mA

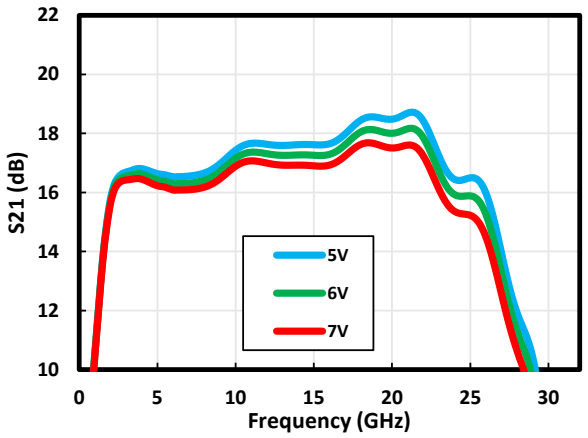


Figure 1-32. Gain vs. V_{DD} at 120 mA

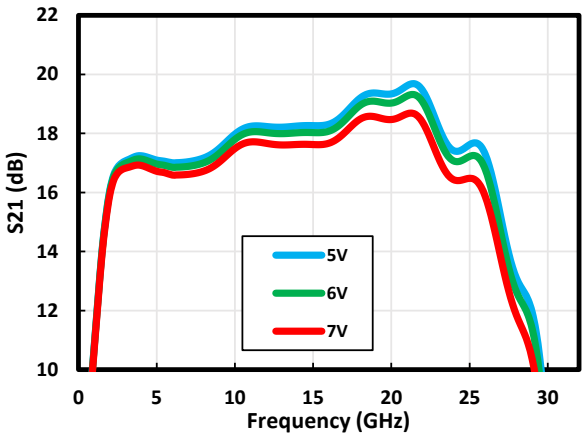


Figure 1-33. Gain vs. V_{DD} at 130 mA

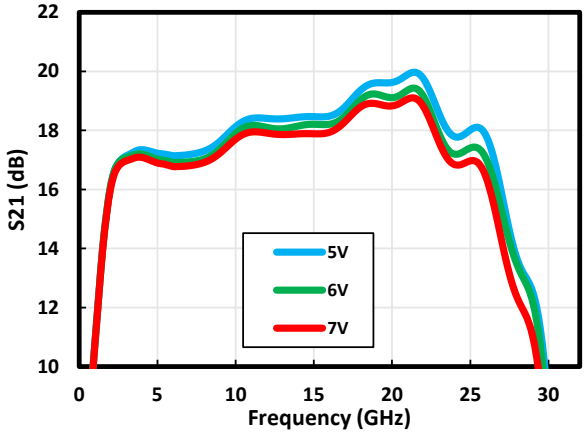


Figure 1-34. NF vs. V_{DD} at 100 mA

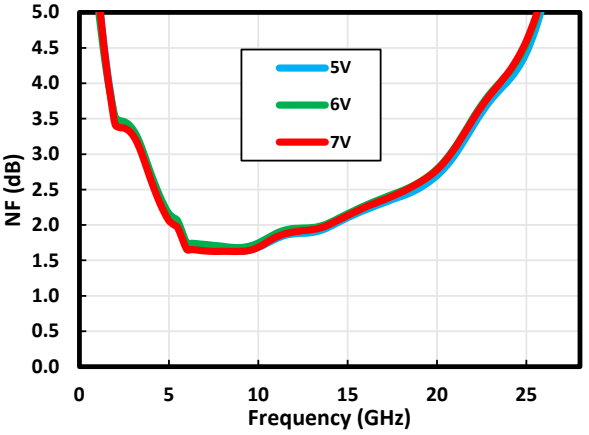


Figure 1-35. NF vs. V_{DD} at 120 mA

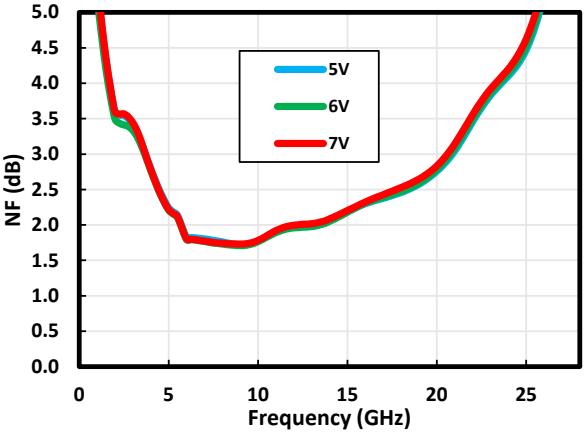


Figure 1-36. NF vs. V_{DD} at 130 mA

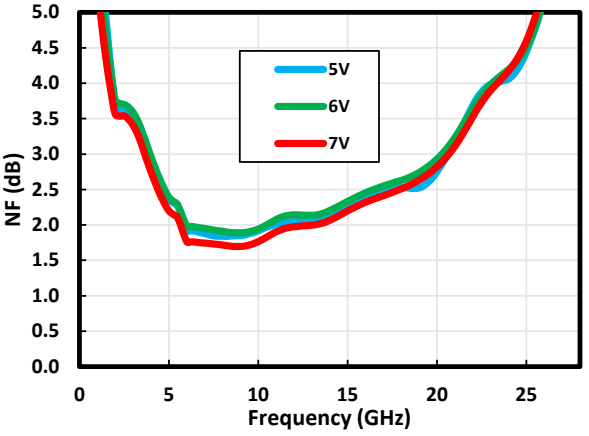


Figure 1-37. P1dB vs. V_{DD}/I_{DD}

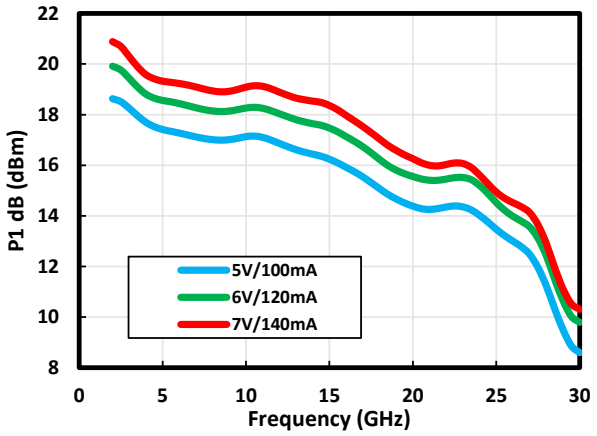


Figure 1-38. P_{sat} vs. V_{DD}/I_{DD}

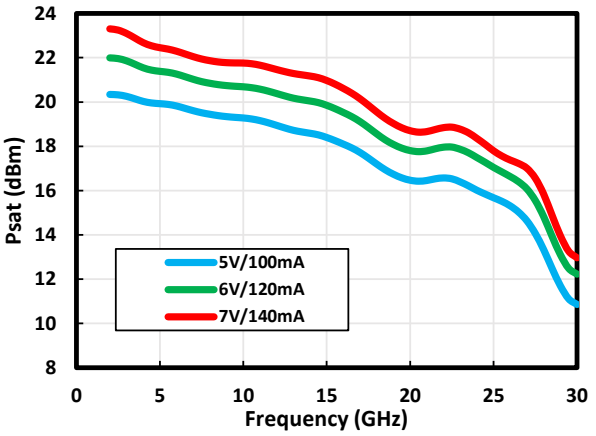


Figure 1-39. OIP3 vs. V_{DD}/I_{DD}

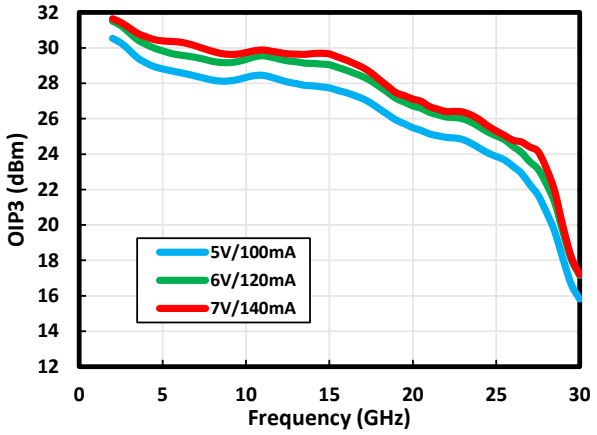


Figure 1-40. OIP2 Low at Δ = 250 MHz vs. V_{DD}/I_{DD}

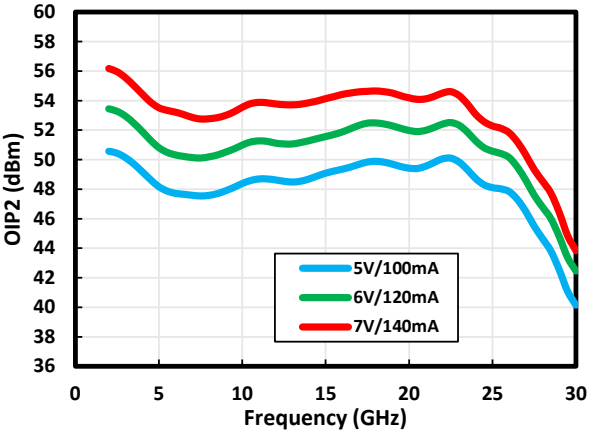


Figure 1-41. IM3 vs. V_{DD}/I_{DD}, 10 dBm (per tone)

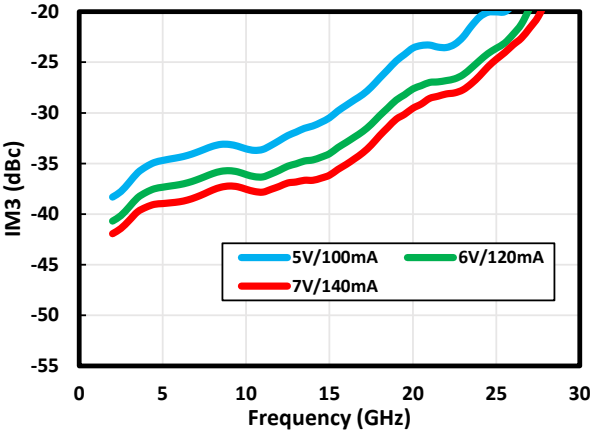


Figure 1-42. Gain vs. Input Bias Current at 6V/120 mA

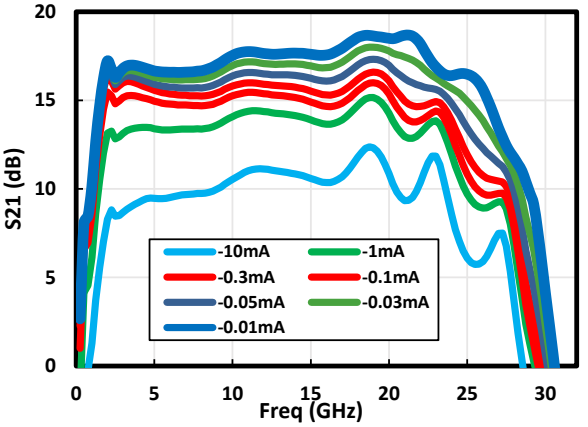
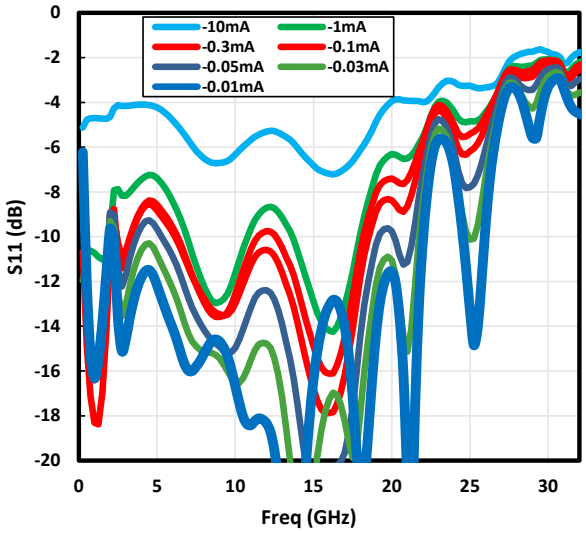


Figure 1-43. S11 vs. Input Bias Current at 6V/120 mA



1.3.3 Typical Performance vs. Output Power

The graphs shown in Figures 1–44 through 1–53 represent the Typical Performance of MMA042PP4 device at specific bias conditions. All measurements were taken using board shown in Figure 3–3.

Figure 1-44. IM2 vs. Power at 5V/100 mA

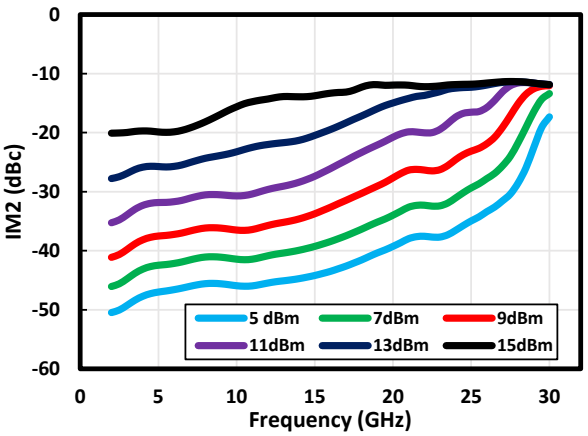


Figure 1-45. IM2 vs. Power at 6V/120 mA

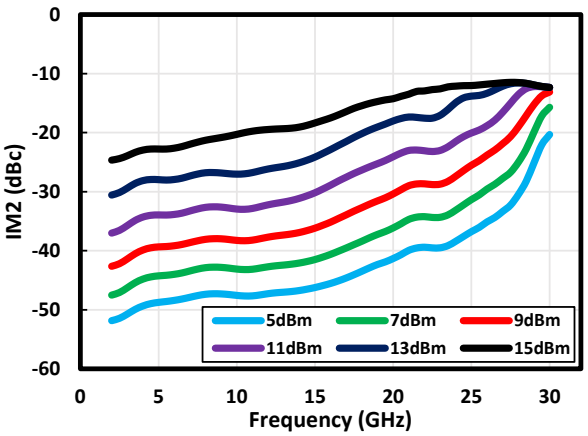


Figure 1-46. IM2 vs. Power at 7V/130 mA

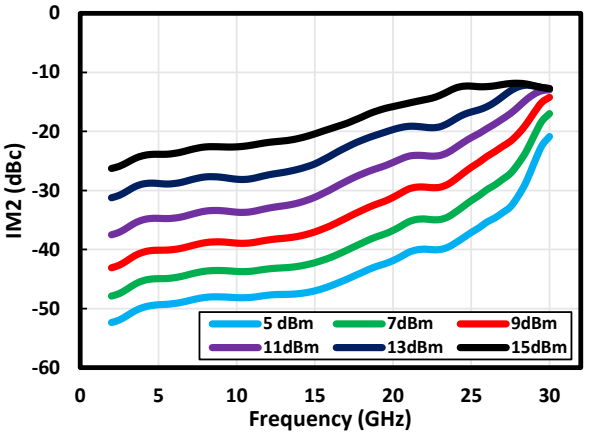


Figure 1-47. IM3 vs. Power at 5V/100 mA

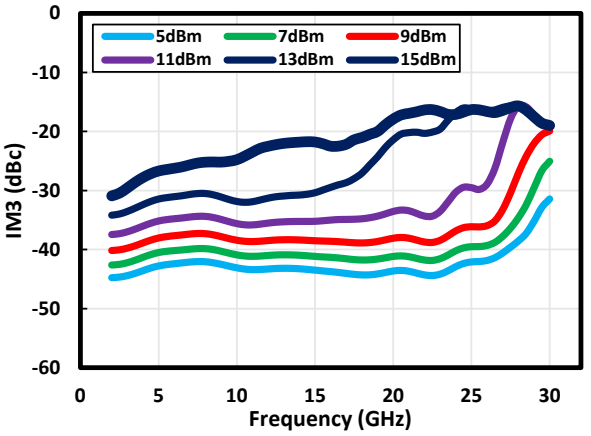


Figure 1-48. IM3 vs. Power at 6V/120 mA

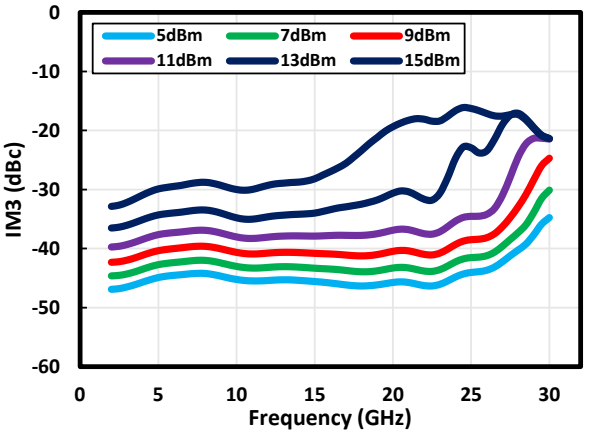


Figure 1-49. IM3 vs. Power at 7V/130 mA

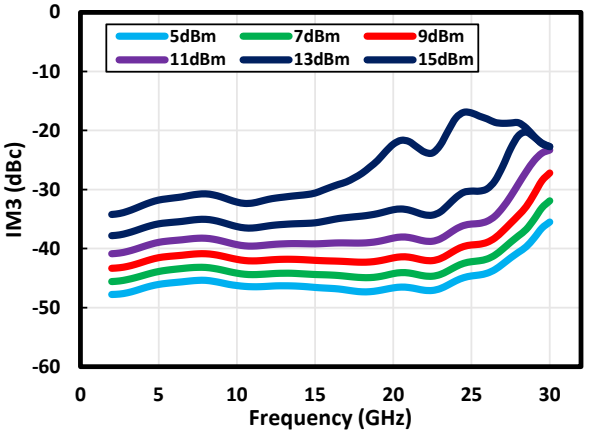


Figure 1-50. 2-nd Harmonic vs. Power at 5V/100 mA

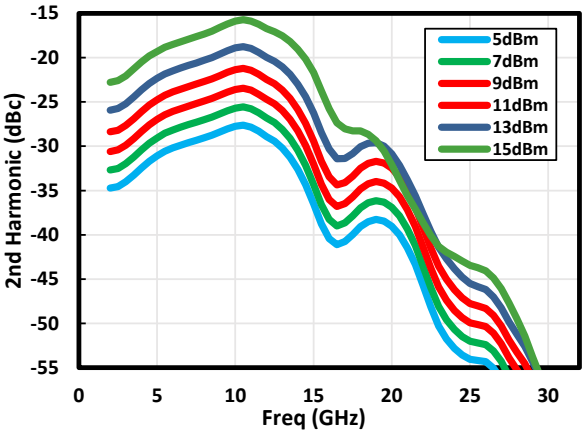


Figure 1-51. 2-nd Harmonic vs. Power at 6V/120 mA

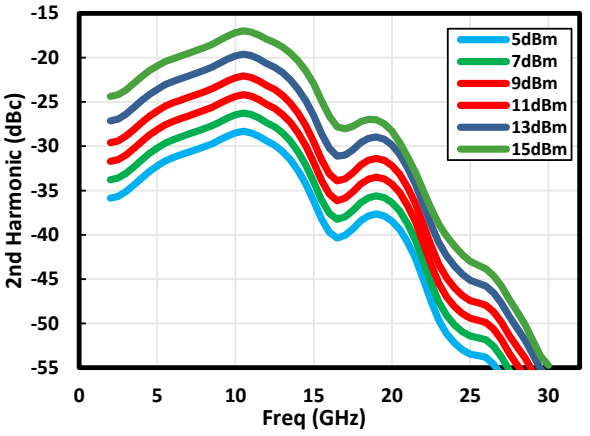


Figure 1-52. 2-nd Harmonic vs. Power at 7V/130 mA

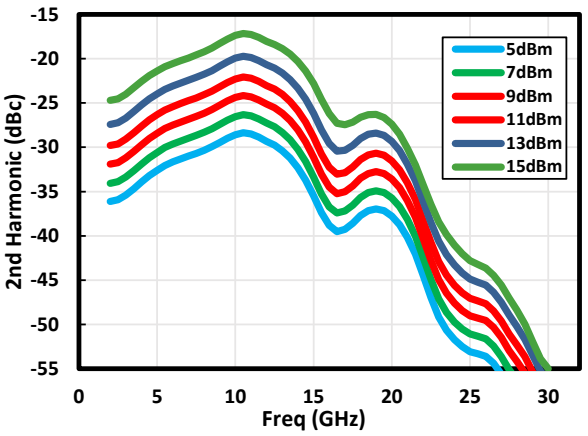
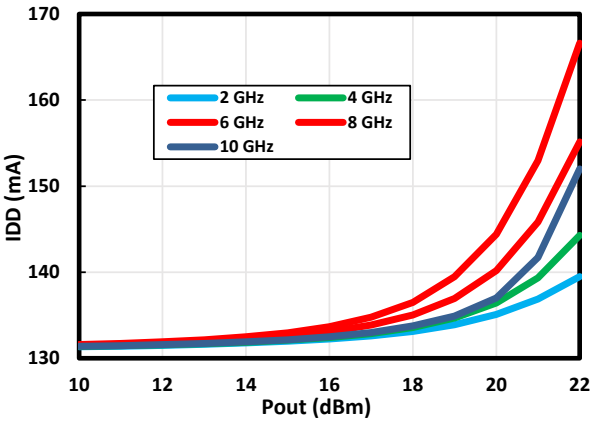


Figure 1-53. I_{DD} vs. P_{out} at 7V



2. Package Specifications

For additional packaging information, contact your Microchip sales representative.

Figure 2-1. Package Outline Drawing (mm)

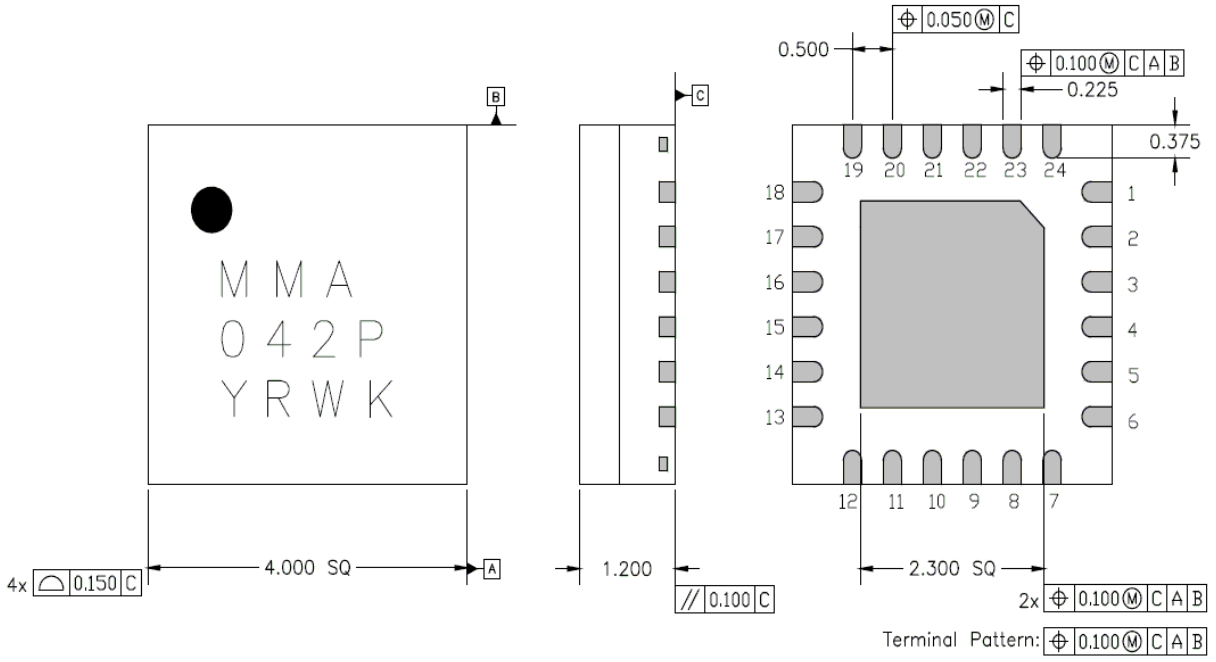


Table 2-1. Package Information

Material	Lead Frame
Plating	Ni: 0.50 µm min. Pd: 0.02 µm min. Au: 0.05 µm max.

Table 2-2. PIN Description

PIN Number	Pad Name	Pad Description
4, 5	RFIN	AC–coupled and matched to 50Ω
15, 16	RFOUT	AC–coupled and matched to 50Ω
22	VDD	VDD supply
9	VSB	Used to Set IDD through external optional resistor RSB, see Table 3-2
10, 11	VGA, VGB	Access to Gate 1 bias, connect to Ground either one for nominal operation.
3, 6, 14, 17	GND	RF/DC Ground Pins
1, 2, 7, 8, 12, 13, 18, 19, 20,21, 23, 24	N/C	Not connected pins (recommended to be grounded to RF ground on PCB)
Backside Paddle	RF/DC GND	Must be connected to RF/DC Ground

3. Application Circuit

Figure 3-1. Eval PCB Schematic

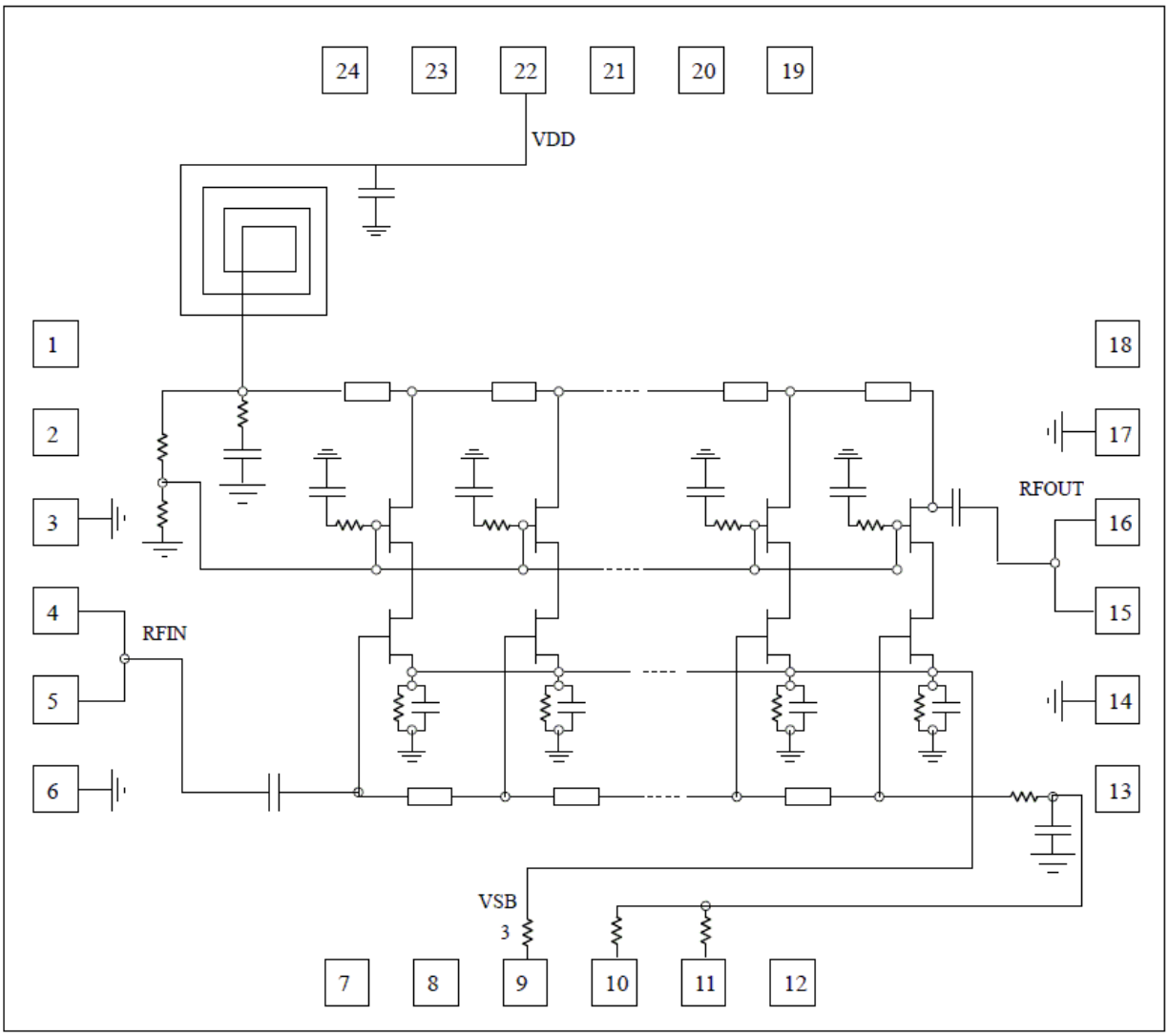


Figure 3-2. Evaluation Board Circuit

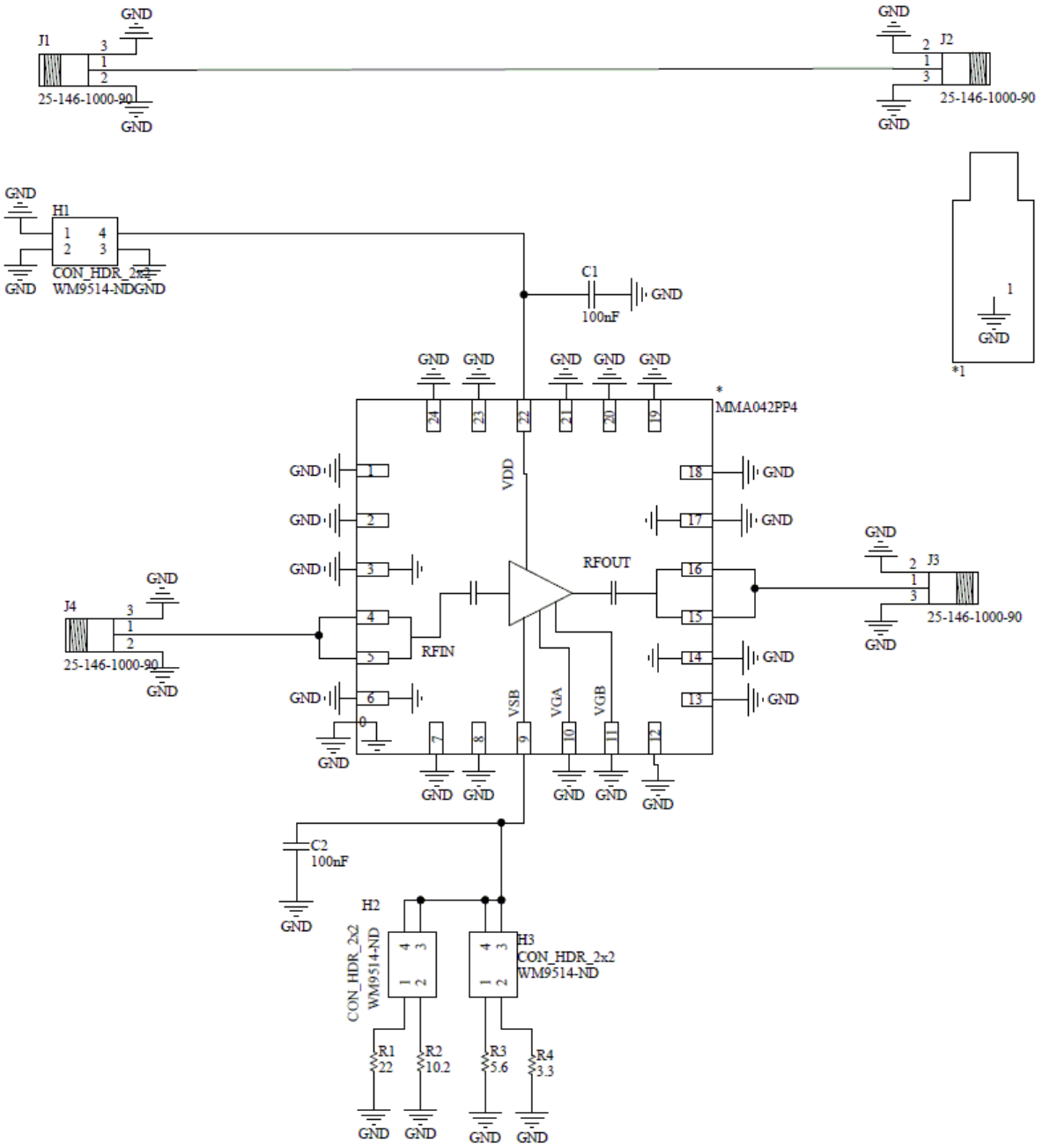


Figure 3-3. Evaluation Board MMA042PP4E

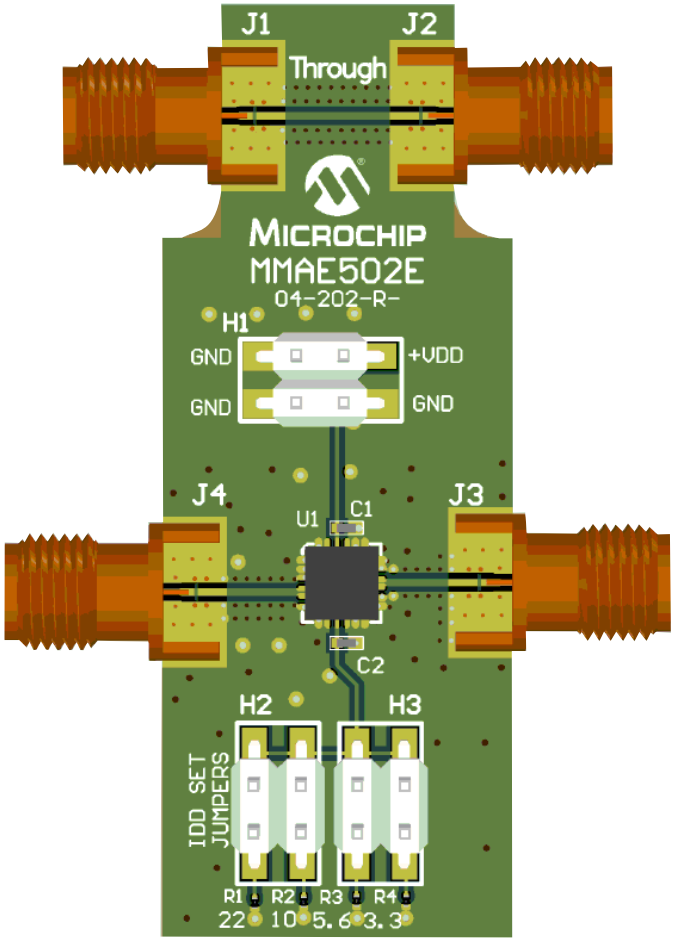


Table 3-1. List of Material for figure : Assembly Drawing

Designation	Part Number	Description
1		PCB backplate
C1...C2	0201X104K160GT	Cap 100 nF 16V ±10% X7R Au cer 0201
H1, H2, H3	15–91–2040	Header, 2-pin, dual row
J1, J2, J3, J4	25–146–1000–90	CONN 2.9MM FEMALE PCB EDGE MOUNT 0.12 PIN
R1	ERJ–1GEF22R0C	RES 22 OHM 1/20W 1% 0201 SMD
R2	ERJ–1GEF10R2C	RES 10 OHM 1/20W 1% 0201 SMD
R3	ERJ–1GEJ5R6C	Res 5.6–OHM 1/20W 5% 0201
R4	ERJ–1GEJ3R3C	RES 3.3–OHM 1/20W 5% 0201
U1	MMA042PP4	MMA042PP4 4X4 QFN

Table 3-2. Evaluation Board Jumper Settings for I_{DD} (mA)

State	Jumper Settings						
	R1	R2	R3	R4	I_{dd} at 5V	I_{dd} at 6V	I_{dd} at 7V
1	Open	Open	Open	Open	73	76	79
2	Short	Open	Open	Open	85	88	91
3	Open	Short	Open	Open	94	97	100
4	Short	Short	Open	Open	99	102	106
5	Open	Open	Short	Open	103	106	109
6	Short	Open	Short	Open	106	109	113
7	Open	Short	Short	Open	109	113	116
8	Short	Short	Short	Open	111	115	119
9	Open	Open	Open	Short	110	114	118
10	Short	Open	Open	Short	112	116	120
11	Open	Short	Open	Short	114	118	122
12	Short	Short	Open	Short	116	119	123
13	Open	Open	Short	Short	117	121	124
14	Short	Open	Short	Short	118	122	126
15	Open	Short	Short	Short	119	123	127
16	Short	Short	Short	Short	120	124	128

Table 3-3. RSB Values[1] vs. Drain Current at 5, 6, 7V

RSB (Ohm)	IDD (mA) at 5V	IDD (mA) at 6V	IDD (mA) at 7V
0	130	131	136
1	122	125	129
2	116	120	123
3	112	115	119
4	108	112	116
5	106	109	113
6	103	107	110
7	101	104	108
8	100	103	106
9	98	101	105
10	96	100	103
11	95	98	102
12	94	97	101
13	93	97	100
14	92	96	99
15	92	95	98
16	91	94	97
17	90	94	97
18	90	93	96
19	89	92	96
20	89	92	95

Note:

1. R_{SB}–Bias defining resistor connecting between Pin 9 and ground on Figure 3-3.

4. Ordering, Shipping, and Handling

4.1 Handling Recommendations

Gallium Arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

4.2 Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package
MMA042PP4	4 mm × 4 mm, 24L Plastic QFN
MMA042AA	Die, refer to corresponding MMA042AA datasheet.
MMA042PP4E	Evaluation board for MMA042PP4

4.3 Packing Information

Standard Format
Tape and Reel

Note: Contact your Microchip sales representative for the minimum quantity order

5. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 5-1. Revision History

Revision	Date	Description
B	06/2024	Updated with new data throughout, updated plots.
A	05/2022	Document created.

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